Application Note

Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions

Paul Grohe

ABSTRACT

The TL331, LM339, LM393, and the next generation B-versions (TL331B, LM339B, LM2901B, LM393B and LM2903B) are a popular and long-lived family of standard comparators due to their flexibility, availability, and cost-effectiveness. It is important to understand how these comparators are different than most other comparators before using them in your design. The information in this application guide will help promote first time design successes. The front page of the B data sheets contains a table showing the differences in specifications between the various classic devices and the new B device.

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Trademarks

1 Devices Covered in Application Note

This application note covers all comparators devices listed in Table 1-1 including the next generation B-versions which have improved specifications. All of these comparators contain a unique input stage that was revolutionary when released in the early 1970's. Unlike other comparators of that time, it supported ground level input voltages useful for single supply designs.

1.1 Base Part Numbers

The base part numbering is unconventional, as the numbering was assigned in order of product development. The LMx39/LM2901 quad was released first, followed by the LMx93/LM2903 dual, then followed by the TL331 (TI) and LM397 (National) singles several years later. The "-Q1" suffix denotes AEC-Q100 qualified devices. The “-N” in a part name denotes devices acquired from the National Semiconductor acquisition that matched an existing Texas Instruments (TI) base part number. There are no current orderable part number duplicates because National Semiconductor and TI used different package suffixes. Likewise, the next generation versions have the suffix "B" added which indicates improved specifications. We will refer to all the devices listed below as the "LM339 Family" throughout this document.

Table 1-1. Base Part Number, Channel Count, and Temperature Range

Temperature Range	Single	Dual	Quad
–55°C to 125°C	TL331-EP	LM193, LM193-MIL, LM193-N, LM193QML, LM193QML-SP, LM293-EP	LM139, LM139-MIL, LM139-N, LM139-SP, LM139A, LM139A-MIL, LM139AQML, LM139AQML-SP, LM239A-EP
–40°C to 125°C	TL331B	LM2903, LM2903V, LM2903AV, LM2903B	LM239A-EP, LM2901, LM2901AV, LM2901V, LM2901B
–40°C to 105°C	TL331K	See –40°C to 125°C	See –40°C to 125°C
–40°C to 85°C	LM397	LM393B, LM2903-N	LM339B, LM2901-N, LM2901EP, LM3302
–25°C to 85°C	TL331I	LM293, LM293-N, LM293A	LM239, LM239-N, LM239A
0°C to 70°C	See –25°C to 85°C	LM393, LM393-N, LM393A	LM339, LM339-N, LM339A , LM339-MIL
Automotive Q1 (–40°C to 125°C)	TL331B-Q1,TL331-Q1	LM2903B-Q1, LM2903-Q1	LM239A-Q1, LM2901-Q1, LM2901AV-Q1, LM2901V-Q1, LM2901B, LM2901B-Q1
Automotive Q0 (–40°C to 150°C)	-	LM2903-Q1 (E Version)	-

1.2 Input Voltage Offset Grades

There are also grade options for V_{IO} (also known as V_{os}) tolerance. An “A” in the part number suffix will have better V_{IO} specifications compared to the same part number without an A.

Table 1-2. Maximum Input Offset Error at 25°C for Each Base Part Number with V_{IO} Grade Options

Single		Dual		Quad	
Part Number	V_{IO} Max 25°C	Part Number	V_{IO} Max 25°C	Part Number	V_{IO} Max 25°C
LM397	7 mV	LM193	5 mV	LM139	5 mV
TL331	5 mV	LM193-MIL	5 mV	LM139-MIL	5 mV
TL331-EP	5 mV	LM193-N	5 mV	LM139-N	2 mV, 5 mV
TL331-Q1	5 mV	LM193QML	5 mV	LM139-SP	2 mV
TL331B	4 mV	LM193QML-SP	5 mV	LM139A	2 mV
TL331B-Q1	4 mV	LM2903	7 mV	LM139A-MIL	2 mV
TL391B	4 mV	LM2903-N	7 mV	LM139AQML	2 mV
TL391B-Q1	4 mV	LM2903-Q1	2 mV, 7 mV	LM139AQML-SP	2 mV
		LM2903V	2 mV, 7 mV	LM239	9 mV
		LM293	5 mV	LM239-N	5 mV
		LM293-EP	5 mV	LM239A	3 mV
		LM293-N	5 mV	LM239A-EP	2.5 mV
		LM293A	2 mV	LM239A-Q1	2.5 mV
		LM393	5 mV	LM2901	7 mV
		LM393-N	5 mV	LM2901-N	7 mV
		LM393A	2 mV	LM2901-Q1	7 mV
		LM393B, LM2903B	2.5 mV	LM2901AV	2 mV
				LM2901AV-Q1	2 mV
				LM2901EP	7 mV
				LM2901V	7 mV
				LM2901V-Q1	7 mV
				LM3302	20 mV
				LM339	9 mV
				LM339-MIL	5 mV
				LM339-N	2 mV, 5 mV
				LM339A	3 mV
				LM339B	5.5 mV
				LM2901B	5.5 mV
				LM2901B-Q1	5.5 mV

1.3 Maximum Supply Voltage

The default maximum recommended supply voltage is 30 V. Devices having a V in the suffix, denotes maximum voltage up to 32 V.

The new B versions, such as the TL331B, LM393B, LM339B, LM2901B and LM2903B have maximum voltage up to 38 V.

1.4 High Reliability Options

There are many high reliability options for the single, dual, and quad comparators.

Single comparator product list: TL331-EP.

Dual comparator product list: LM193QML-SP, LM193QML, LM293A-EP, LM293-N, LM2904-EP, LM139AQML and LM139JAN.

Quad comparator product list: LM139-SP, LM139AQML-SP, LM139-MIL, LM139A-MIL, LM139AQML and LM139JAN.

The qualifications and ratings of these devices are not covered in this application note. Please consult the individual device data sheets.

2 The New TL331B, TL391B, LM339B, LM393B, LM2901B and LM2903B B Versions

In late 2019, TI introduced a new, updated B design based on a new high-voltage junction-isolated process to replace the classic LM339 design that has existed since the early 1970's. This update allowed for improvements in many specifications and smaller package options.

The new B devices were designed to have equal to, or better-than, performance than the classic devices so that they can easily drop-in replace the classic devices. The front page of the B data sheets contains a convenient table showing the differences in specifications between the various classic devices and the new B device. An example a comparison table is shown in Comparison Table for the LM393B and LM2903B Dual Family.

Comparison Table for the LM393B and LM2903B Dual Family

Specification	LM393B	LM2903B	LM393 LM393A	LM2903	LM2903V LM2903AV	LM193	LM293 LM293A	Units
Supply Voltage	2 to 36	2 to 36	2 to 30	2 to 30	2 to 32	2 to 30	2 to 30	V
Total Supply Current (5 V to 36 V max)	0.6 to 0.8	0.6 to 0.8	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	mA
Temperature Range	−40 to 85	−40 to 125	0 to 70	−40 to 125	−40 to 125	−55 to 125	−25 to 85	°C
ESD (HBM)	2000	2000	1000	1000	1000	1000	1000	V
Offset Voltage (Max over temp)	± 4	± 4	± 9 ± 4	± 15	± 15 ± 4	± 9	± 9 ± 4	mV
Input Bias Current (typ / max)	3.5 / 25	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 100	25 / 250	nA
Response Time (typ)	1	1	1.3	1.3	1.3	1.3	1.3	µsec

As shown in the Comparison Table for the LM393B and LM2903B Dual Family example above, improvements in the B devices can be seen in wider supply voltage range, lower offset voltage, much lower bias current, faster propagation delay and lower supply current. Similar improvements were made to the Single TL331B and Quad LM339B/2901B.

2.1 PCN to Change Classic Die to a New Die Design

In March 2021, Product Change Notifications (PCN's) #20210318001 (Single and Dual) and #20231016006 (Quad) were issued to notify customers that the classic die is to be replaced with a new die based on the B device die. These PCN notices contain a list of the devices planned to change. These PCN's are sent to customers from their distributors.

The existing electrical specification limits, part markings and orderable part numbers for the classic devices remain the same. Some of the electrical table typical numbers and graphs can change to reflect any major differences between the old die and new die. The new die devices have passed, or exceeded, all the qualifications of the classic die. A qualification summary is available within the associated PCN.

For known differences, please see Differences between the classic and B version.

TI recommends that any new or updated designs specify the new B devices to immediately spot any possible compatibility issues. Eventually, all die will be based on the B die.

These high volume device families are assembled at multiple assembly sites, and not all of these assembly sites are converting to the new die at the same time. Therefore, as of this writing, **it is possible to receive a mix of classic die and new die for a given high volume orderable part number** (LM2903DR for example). The mix will be between sealed containers (bag or reel) and not mixed within a single rail or reel. The reel or bag information will provide the necessary die information.

Only the Native TI Commercial and Automotive devices are affected by the PCN's. At this time, there are no plans to PCN the Ex-National Semiconductor (the "-N") versions. The Military (/883, -MIL), QML, Space and Rad Hard families using the ex-National die will continue with their existing die. Some Native TI Military devices may be be affected by a PCN. These will be listed in the associated PCN.

To determine which die is used, the chip site and fab site location fields on the box label or bag label are viewed.

2.1.1 Determine Die Used for Single TL331 and Dual LM293, LM393, and LM2903

The Single TL331 and Dual LMx39/2903 use a different fab location than the quad LMx39/2901. This requires looking at the 21L label fields.

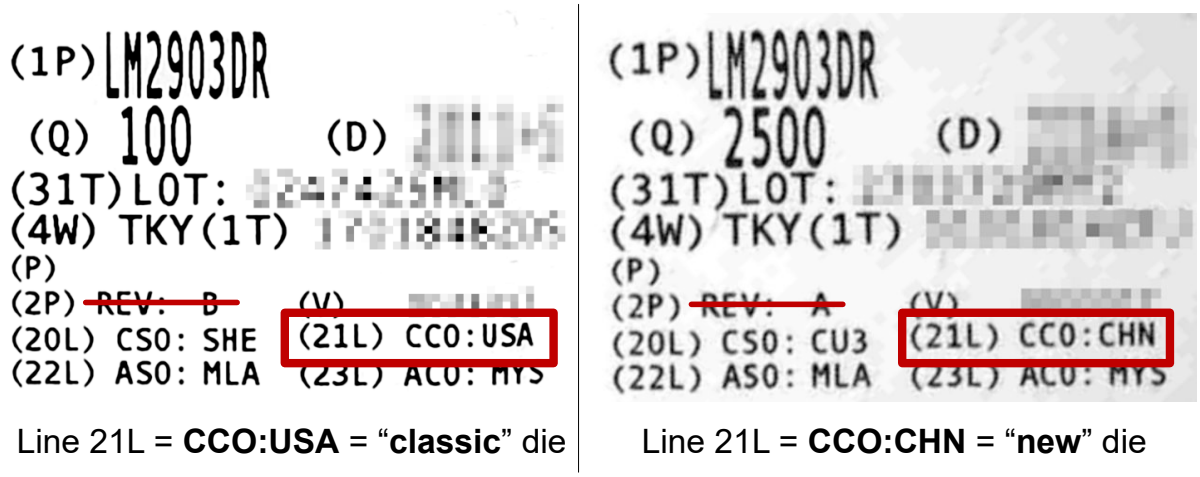


Figure 2-1. Packing Label Examples - Single TL331 and Dual LM293 / LM393 / LM2903

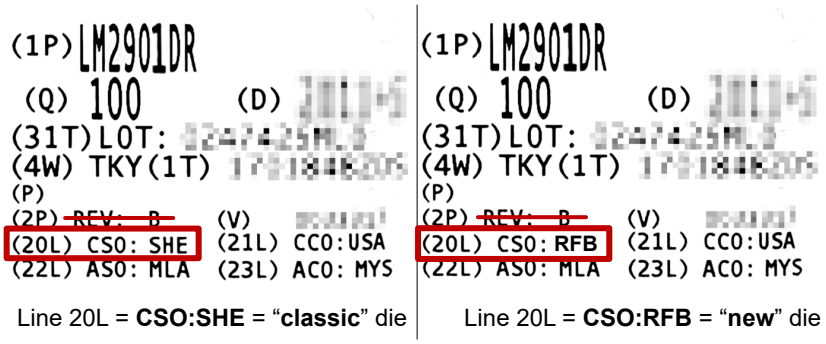
For the single and dual, if the Chip Country of Origin (21L) CCO: field says USA, then this is the classic die.

For the single and dual, if the Chip Country of Origin (21L) CCO: field says CHN, then this is the new die.

Please ignore the *(2P) REV: x* field (crossed out above) to determine which die is used. This field is the revision of the particular die used and does not represent which core die design is used. This has caused some confusion in the past.

2.1.2 Determine Die Used for Quad LM139, LM239, LM339, and LM2901

Because the classic and new quad die are both fabricated in the USA, attention must be paid to the particular fab site location (20L) fields.



Line 20L = **CSO:SHE** = "**classic**" die

Line 20L = **CSO:RFB** = "**new**" die

Figure 2-2. Packing Label Examples - Quad LM139 / LM239 / LM339 / LM2901

For the quad LM339 or LM2901, if the Chip Site of Origin (20L) CCO: field says SHE, then this is the classic (SFAB) die.

For the quad LM339 or LM2901, if the Chip Site of Origin (20L) CCO: field says RFB, then this is the new (RFAB) die.

Please ignore the*(2P) REV: x* field (crossed out above) to determine which die is used. This field is the revision of the particular die used and does not represent which core die design is used. This has caused some confusion in the past.

2.1.3 Device PCN Summary

Device PCN Summary summarizes the differences between the pre-PCN and post-PCN behavior.

Table 2-1. Device PCN Summary

Device Family (Including -Q1)	Chip Site Origin Packing Label Field (20L) CSO : _ _ _	Chip Country Origin Packing Label Field (21L) CCO : _ _ _	Die Process	Both Inputs Above Input Range Ouptut Behavior
LM139/239/339 (Pre PCN)	SHE	USA	JI1	Low
LM139/239/339 (Post PCN)	RFB	USA	TIB	High
LM339B	RFB	USA	TIB	High
LM2901 (Pre PCN)	SHE	USA	JI1	Low
LM2901 (Post PCN)	RFB	USA	TIB	High
LM2901B	RFB	USA	TIB	High
LM193/239/393 (Pre PCN)	SHE	USA	JI1	Low
LM193/239/393 (Post PCN)	RFB	USA	JI3	High
LM393B	CU3	CHN	JI3	High
LM2903 (Pre PCN)	SHE	USA	JI1	Low
LM2903 (Post PCN)	CU3	CHN	JI3	High
LM2903B	CU3	CHN	JI3	High
TL331 (Pre PCN)	SHE	USA	JI1	Low
TL331 (Post PCN)	CU3	CHN	JI3	High
TL331B	CU3	CHN	JI3	High

2.2 Changes to Package Top Markings

In early 2022, TI made changes to the device top markings company-wide, and not just specific to the LM339 family. This change was covered in PCN# 20211123004 for most of the LM339 family.

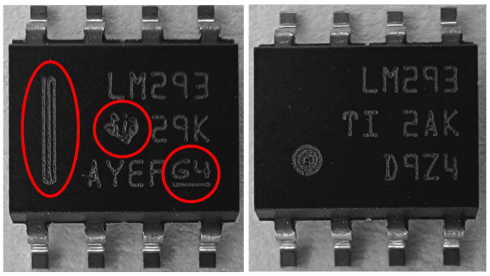


Figure 2-3. Package Marking Change Comparison

The left photo is the previous *bar* style marking, and the right photo is the new *dot* style marking.

The package marking changes are:

1. The pin 1 *bar* marking was changed to a single dot.
2. The TI logo graphic was replaced with the letters `TI`.
3. The underscored *E Category* marking (commonly G4 or E4) was eliminated.
4. The font was changed to a more Optical Character Recognition (OCRA) friendly font.

These label changes are gradually being applied across TI, and is possible to get a mix of the two device marking styles in large orders. **The marking changes do not directly indicate which die is used, and it is still possible to get a *classic* die with the new top marking style**.

3 Input Considerations

3.1 Input Stage Schematic – The Classic LM339 Family

The simplified classic LM339 Family comparator internal schematic is shown in Figure 3-1. Minus a few devices in the biasing circuitry, the schematic is a fairly true representation of the actual internal circuit.

The input stage consists of the PNP Darlington Input Pairs Q1+Q2, and Q3+Q4, the bias mirror Q10 to provide the operating tail currents, and the active load of Q5 and Q6. The output stage is comprised of Q7, Q12 and output transistor Q8. Diodes D1 through D4 protect the input devices when the inputs are taken above V+.

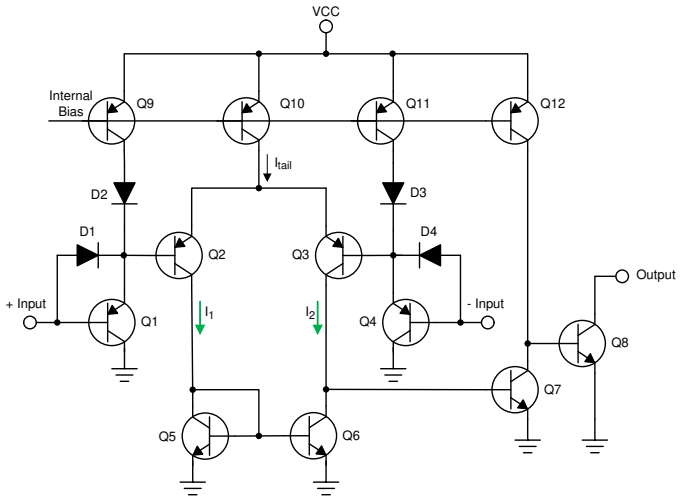


Figure 3-1. Simplified Input Stage Schematic with All Current Source Connections

The schematic also contains additional current source lines (Q9, D2, Q11, and D3) not drawn in the simplified schematic found in the data sheets. All PNP emitters in the Darlington input stage have current source connections. These current sources ensure a consistent input bias current that does not vary with the differential

input voltage. This consistent current provides a high effective input to input resistance. Without these secondary current sources, the input bias current could vary from zero to twice the normal bias current as the differential input voltage is varied.

3.2 Input Stage Schematic - New B Devices

For the new B devices, to improve propagation delay and output drive capability, an additional gain stage consisting of Q13 and Q14 was added to the classic LM339 design.

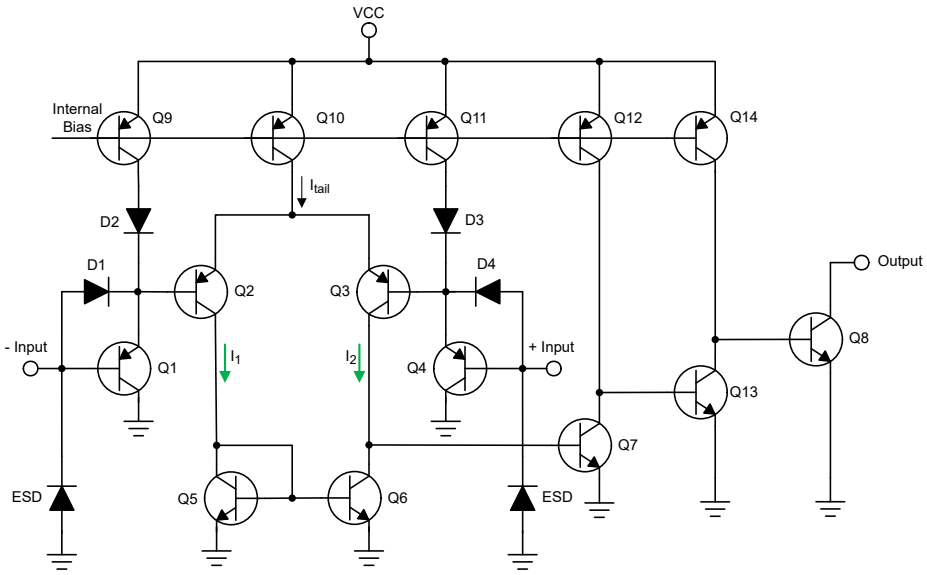


Figure 3-2. Simplified B Internal Schematic

While this additional stage did improve the specifications, the extra stage does add an inversion to the signal path (note that the inputs are now reversed). One effect of this inversion was that Section 3.7.1 behavior is inverted, causing the B devices output go high.

Dedicated ESD protection structures were also added for more robust ESD performance.

3.3 Differences Between the Classic and B Die Devices

While effort was made to make the new B devices drop-in compatible with the classic devices, there can be differences when operated outside of the data sheet specifications.

One major difference is the Section 3.7.1 behavior is inverted. The B version output can go high when both inputs are above VCM.

Because the new B design is slightly faster with lower typical offset voltages, it tends to be more sensitive to noise spikes, ringing and glitches that the older, slower classic design may have ignored. Marginal system designs with excessive ground noise, very noisy input signals, noisy supplies or poor supply bypassing may now show false or multiple triggers. TI recommends proper supply bypassing (100nF minimum) directly between the supply pins. Input signals should be filtered to minimize high frequency noise and transients.

Due to the internal smaller device geometry and tighter junction spacing, the newer B devices tend to be slightly more sensitive to negative input voltages (voltages below the GND pin) and negative supply transients. Please see Section 3.8 for more information to protect against negative inputs.

3.4 Input Voltage Range

The data sheet specified input voltage range indicates the allowable minimum and maximum voltages to be applied to the inputs for normal specified operation. When operated outside the specified input range, parametric changes will occur, particularly offset voltage, bias current and propagation delay.

The specified LM339 Family input voltage range (V_{ICR}) is 0 V (relative to the negative supply pin) to V_{CC} – 1.5 V at room temperature. However, the actual upper input voltage range reduces by -4 mV/°C at cold temperatures. Therefore the specified LM339 Family full temperature range common mode range is 0 V to V_{CC} – 2 V to account for this reduction. The V_{CC} – 2 V range is strongly recommended for use in all designs.

3.5 Input Voltage Range vs. Common Mode Voltage Range

The phrases Common Mode Voltage Range and Input Voltage Range tend to be used interchangeably, but there is an important difference when discussing comparators. The common definition of Common Mode Voltage (CMVR or CMR) is the average of the inverting (-IN) and non-inverting (+IN) input voltages. This definition is acceptable for operational amplifiers where the inputs are kept to less than a millivolt of each other due to negative feedback, but comparator inputs are rarely kept at the same potential and can see several volts of differential voltage under normal operation. If the average value is used, there can be an instance where one input voltage slightly exceeds the input range specification, and the average of the two inputs can still reside within the input range, even though that one input is violating the input range. The average gives a false impression of meeting the input voltage range requirement.

Note

The input voltage limits must be considered **per input** and **NOT** the average of the two input voltages. If, for example, the calculated input voltage limit is 3.5 V, then neither input can exceed 3.5 V.

3.6 Reason for Input Range Headroom Limitation

The LM339 family was the first truly single-supply, ground sensing comparator, but it is not a Rail to Rail input device and can only sense up to about 1.5 V below V_{CC}. The input stage requires some headroom to the V_{CC} supply to provide the needed tail current and biasing to the input devices Q1 through Q4. Assuming a 5 V supply, Figure 3-3 shows the necessary voltage drops from the supply voltage down to the input terminal.

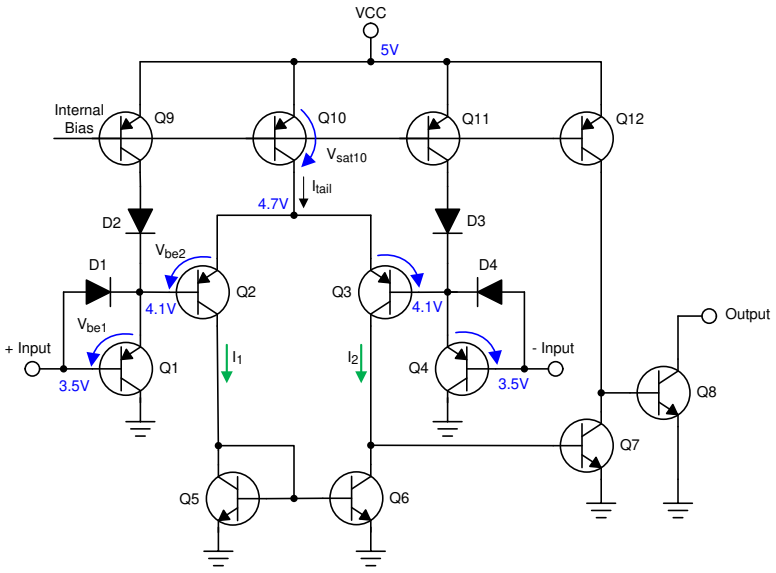


Figure 3-3. Headroom Taken Up by VBE's and VSAT of Input Stage

The DC biasing current flows down from V_{CC} , through the Q10 current source, through the input pair Q2 and Q1, and *out* of the input pin towards ground through the input source resistance.

The required headroom can be analyzed by Counting VBE's, starting at the V_{CC} rail and down to the input pin. Starting at V_{CC}, about 250-300mV is dropped across the current source Q10 collector-emitter junction (V_{SAT10}). Another 600mV is dropped across each of the Base-Emitter junctions of Q2 (V_{BE2}) and Q1 (V_{BE1}). By adding all the drops together (V_{SAT10} + V_{BE1} + V_{BE2}), it can be seen that there needs to be at least a 1.5 V headroom between the input pin and V_{CC} for the input stage to bias properly.

If an input is brought above the input limit, that input transistor starts to turn off, and the tail current for that device (I_1 or I_2) is also cut off.

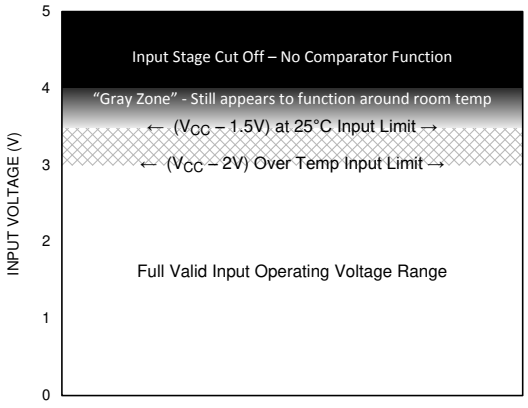


Figure 3-4. Visual Representation of Input Voltage Range With a 5 V Supply

Figure 3-4 shows a visual representation of the input voltage range with a single +5 V supply.

Between 0 V and 3 V (V_{CC} - 2V), the device is fully operational and will function per data sheet specifications over the full specified temperature range. The V_{CC} - 2V limit is the recommended upper input range limit to be utilized for all designs.

The input range from 0 to 3.5 V (V_{CC} - 1.5V) is valid at 25°C and above. The range between 3 V and 3.5 V will vary over temperature due to the V_{BE}'s of the transistors changing at -2.1mV/°C. This results in the input voltage range changing at -4.2mV/°C over temperature (note the negative sign!), necessitating the V_{CC} - 2 V over temperature specification. Using the V_{CC} - 1.5 V limit can cause *It worked fine on the bench, but it fails at cold* complaints. Do not make this mistake!

The range between 3.5 V and 4 V is the gray zone, where the device appears to still function at 25°C and above, but critical specifications are deteriorating, such as offset voltage, bias current and particularly propagation delay as the input stage is gradually starved. These effects may not be immediately apparent. Operating at low temperatures *can* cause failures. Operation within this zone must be avoided.

Between 4 V and 5 V, and even up to 36 V, the input stage is cut off and input bias current falls to near zero. The actual cut-off threshold depends on temperature. Comparator operation ceases. DO NOT operate in this area!

3.7 Input Voltage Range Feature

A nice feature of the LM339 family (and ONLY applies to the LM339 family devices listed in Table 1-2) is that only one input needs to be within the valid input voltage range for a valid output. The other input can be above the input voltage range or, even above V_{CC} and the output will be in the expected state.

Note

The following feature was originally intended to reassure users of *expected* behavior during fault conditions or transient conditions. It is described here only because it has been mentioned in the data sheets over the years. **TI strongly advises to stay within the specified input voltage range limits and not to rely on the following feature as part of normal operating conditions. The device will not meet full data sheet specifications in this mode**.

This occurs because as long as *one* of the inputs is still within the valid input voltage range, that input pairs tail current (I_1 or I_2) is still flowing, signaling the correct output polarity to the active loads Q5 and Q6.

While this is a nice feature, it does come at a cost. When operating outside the specified input voltage limits, performance deteriorates and will no longer meet the data sheet specifications. Critical specifications such as offset voltage, bias current and propagation delay will be adversely affected. TI still recommends to stay within the data sheet input voltage range specifications.

3.7.1 Both Inputs Above Input Range Behavior

If both inputs exceed the upper input voltage range (Vin > Vcc - 1.5V), both I_1 and I_2 are cut off, so Q7 remains off, which allows the base of Q8 to be pulled-up and saturate, pulling the output low.

For the classic devices, when the inputs exceed the upper input range, the output goes Low. Because of the Section 3.2 in the B devices, adding an inversion, the B devices output will go high.

Because the inputs have no internal clamp or ESD diodes to V_{CC}, the input voltage can go up to a maximum of 36 V. If the inputs exceed about V_{CC}-1V, the input will block current flow due to the reverse biased base-emitter junctions in the input PNP transistors and associated blocking diodes D2 or D4. Current flow is blocked even if V_{CC} equals 0 V. If either input or both inputs exceed the maximum 36 V V_{CC} rating, junction breakdown can occur. This can lead to permanent device damage per the table notes in the respective device's data sheet *Absolute Maximum Ratings* table.

If either input is lower than –0.3 V with respect to the negative supply, excessive input current can flow in the substrate and the output can display phase reversal, also called inversion. See the Negative Input Voltages in the following section for further information.

3.8 Negative Input Voltages

The LM339 family does not like negative input voltage on any I/O pins, and this is mentioned several times in the data sheets. The LM339 family is built using a junction-isolated die process, wherein all the individual on-die devices are electrically separated from the substrate by a reversed PN junction. This can be thought of as a reversed diode under every circuit node to a common die substrate. These junctions are commonly referred to as the Body Diode or Substrate Diode. For this junction isolation to function properly, the substrate ***must*** be maintained at the most negative potential. The die substrate is electrically tied to the GND pin, and thus the GND pin must be at the most negative circuit potential for proper operation.

If any pin is brought more negative than the GND pin (substrate), these various substrate junctions and parasitic transistors will start to conduct. Reverse currents now flow in paths that were not designed for current flow and this can cause parasitic devices to appear, leading to malfunctions, or worse, latch-up if the input current is high enough.

Figure 3-5 shows the input current of the input pin with a +5 V supply, sweeping the input from -1 V to +7 V. Noticeable nanoamp currents will start to flow when the input is at -0.3 V, and will increase to several tens of milliamps as the diodes start to conduct.

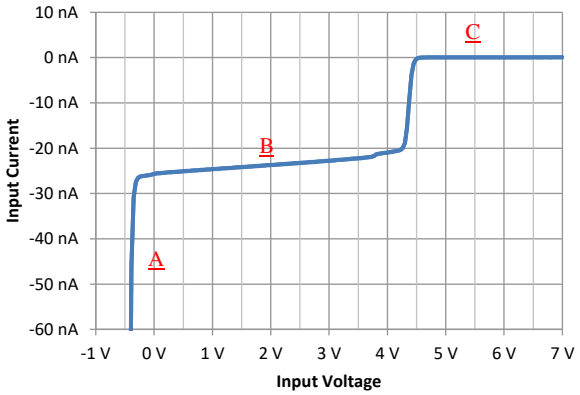


Figure 3-5. Classic Input Pin I/V Curve with 5 V Supply

Section A shows the substrate diode knee starting to conduct at -400mV, with the subsequent increase in reverse current as the negative input voltage is increased.

Section B shows the normal operating Input Bias Current from 0 V up to 3.5 V. The gray zone can be seen as the current heads up towards zero after 4 V.

Section C shows the near zero (picoamp) bias currents as the input devices are reversed and cut off and no base current flows.

When the LM339 Family was originally designed in the early 70's, Electrostatic Discharge (ESD) damage was not as prevalent due to the high breakdown voltages of these older processes, so dedicated ESD protection structures were not included in the LM339 family. Without dedicated ESD structures, there is not a defined current path for reverse currents back to the GND pin. The new B devices do have dedicated ESD structures added to the inputs and output pins for more robust ESD performance.

3.8.1 Maximum Input Current

A commonly misinterpreted specification is the *Maximum Input Current* or *Input Current* specification as listed in the Absolute Maximum Table. For this family, the specification can be as high as 50 mA (typically listed as -50 mA).

This current is actually the maximum current that can be passed through the reverse biased substrate diode without damage, though the specification does not imply proper operation at that time. This current is seen when a negative voltage is applied to the input attempting to pull the input below the GND pin (-0.5 V to -1 V). This specification sets a limit on the current as mentioned in the previous section on Negative Input Voltages. At 50 mA, improper operation and malfunctions are possible. TI still recommends keeping the current to below 10mA or less.

This specification does NOT relate to a maximum input bias current. When the input voltage is within proper specified operating range (0 V to Vcc-2 V), the input current can be within the Electrical Specification Tables for maximum bias current (<500nA) and must never approach the milliamp range under normal operation.

3.8.2 Phase Reversal or Inversion

Under certain conditions, the polarity of the output can become incorrect. This scenario, called phase reversal or inversion, occurs when the input of the comparator violates the negative common-mode voltage range. As explained previously, exceeding the positive common mode range tends to result in predictable behavior. But a negative input voltage, relative to the GND pin, can come from unexpected sources, such as switching noise or ground bounce from DC to DC converters. Negative input voltages can also arise from AC capacitor coupled inputs that create a bipolar voltage at the input.

An input voltage of less than –0.3 V can cause parasitic device conduction (Figure 3-5, point A) that results in incorrect output behavior. Operation in this region is not defined in the data sheet as it violates the -0.3V absolute maximum specification for input voltage. The input current turns on internal parasitic NPN transistors that steal current from other internal nodes causing output phase reversal.

Do not try to determine phase reversal performance empirically as different units can have different performance across lots and processes. Negative input voltages must be avoided, assuming a single supply configuration, unless the application can accept either the V_{OL} or V_{OH} level during the duration of the negative input.

3.8.3 Protecting Inputs from Negative Voltages

3.8.3.1 Simple Resistor and Diode Clamp

In cases where a negative input voltage cannot be avoided, such as ringing from inductive sources of bipolar outputs or from direct coupled sensors, a current limiting resistor in series with the input can limit the current to a safe level, as shown in Figure 3-6. The diode must be a Schottky type for lowest forward voltage.

The resistor must be calculated to limit the current to 1mA or less at the highest expected voltage. A rule of thumb is 1kΩ per volt of expected over-voltage. So if the maximum expected negative voltage is -5V, the resistor must be at least 5kΩ or greater. This resistance can be part of the divider or other resistive input network. A similar resistance can be added to the other input for bias current cancellation. The size of the resistor is a compromise between minimum clamp current, bias current error and minimum added delay for AC signals.

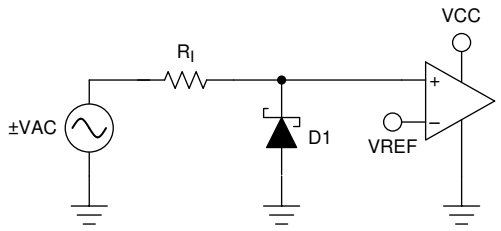


Figure 3-6. Series Resistor And Diode Negative Voltage Protection

If the resistor value is too high, interaction with the comparator input bias current and leakage currents of the diode can cause shifts in the threshold points. High resistor values can also cause delays in AC signals due to the time constant of the input and stray capacitance and the resistor.

If the resistor value is too low, the forward voltage of the diode will increase due to the higher clamp current, as well as load-down the source while clamping. Lower values are better for AC signals due to the lower delay.

The disadvantage of this simple clamp approach is that the forward voltage of the diode can exceed the -300mV input limit, even when using low forward voltage Schottky type diode.

If large negative input voltages are expected, such as zero crossing detectors or input signals with inductive ringing, which require clamping the negative portion of the input signal, then a low ratio voltage divider must then be used. See Section 3.8.3.2.1.

3.8.3.2 Voltage Divider with Clamp

A very common circuit to measure a bipolar high voltage is a resistor divider with a clamping diode is shown in Figure 3-7. The problem is that the diode does not start clamping the negative until -600mV, well past the -300mV negative input voltage limit.

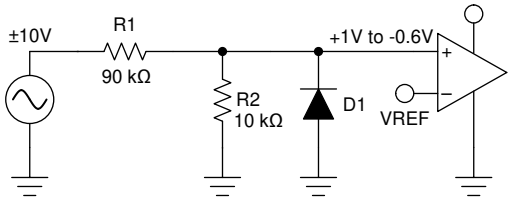


Figure 3-7. Commonly Used Two-Resistor Voltage Divider with Clamping Diode

3.8.3.2.1 Split Voltage Divider with Clamp

To improve upon the voltage divider described above, it is possible to split the upper voltage divider resistor and apply the clamp diode at a higher tap voltage, as shown in Figure 3-8. The idea is that two bottom resistors (R1B and R2) further divide down the diode clamped voltage to bring the clamped voltage to a safe level at the input.

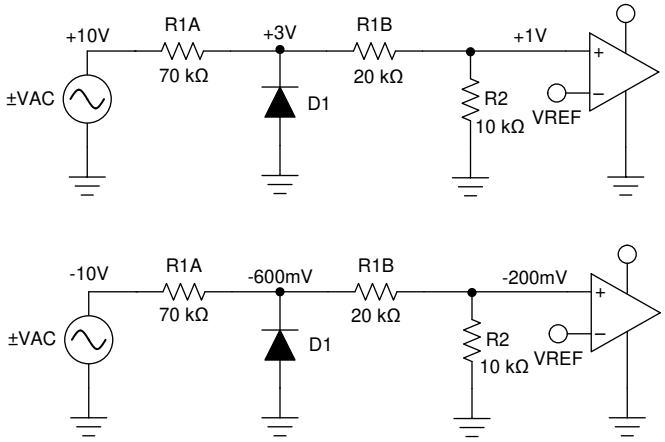


Figure 3-8. Split Voltage Divider Negative Voltage Protection

The upper common voltage divider resistor R1 is split into two resistors, R1A and R1B, providing a higher voltage tap sample point for the clamp diode. The clamp diode ensures that the tap voltage does not exceed -600mV as the input voltage moves further negative.

With a positive input voltage, the diode is reverse biased and does not conduct, effectively removing it from the circuit (except for some small leakage current). The voltage divider R1A + R1B combine create the upper R1 voltage divider resistor against R2.

When the input voltage is negative, the diode clamps the node between R1A and R1B to -600mV. R1B and R2 then create a 3x voltage divider, which results in a safer -200mV on the input. Note that R1A will then have the full input voltage across it and needs to be sized appropriately.

The design procedure is fairly simple. The full divider is calculated as a normal two resistor voltage divider, deriving the needed R1 and R2 values. The desired secondary negative R1B divider is then calculated from the existing R2 and required portion of R1.

3.9 Power-Up Behavior

At power-up, while the comparator supply (Vcc) is below the minimum supply voltage (< 2V), there can be transitions on the output depending on the supply voltage and input voltages applied at that point-in-time. This can cause problems with designs that require a known start-up state, such as a latching circuit or oscillator. Some existing designs can have inadvertently relied on this behavior.

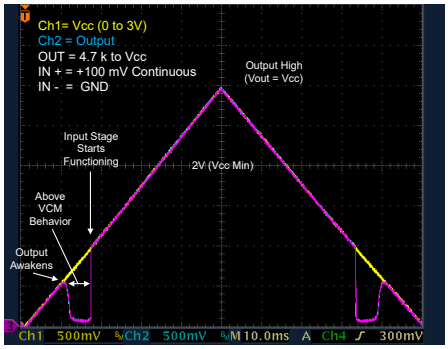


Figure 3-9. Start-up for Classic die, Output set HIGH

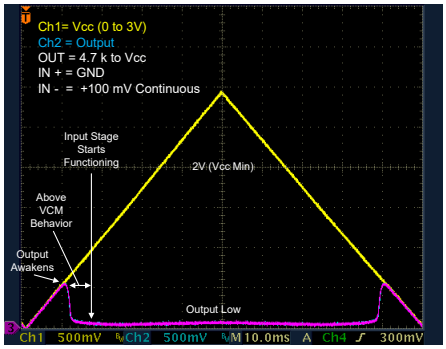


Figure 3-10. Start-up Behavior for Classic die, Output set LOW

Starting from Vcc = 0 V up until approximately 0.55 V, the output is high-impedance as there is not yet enough supply voltage to bias the output driver current source (Q12) and the output transistor (Q8) base-emitter junctions. The output tracks the pull-up supply through the pull-up resistor.

When the supply reaches the range of 0.55 V, the output stage now has *just* enough bias to become active, but the input stage still does not have enough voltage to operate. This is show as Output Awakens in Figure 3-9 and Figure 3-10.

With the output stage functioning and the input stage still inoperative (cut-off), the output behavior in this region is similar to when Section 3.7. This is shown as *Out Of VCM Behavior* in Figure 3-9 and Figure 3-10. The "classic" die output will go low, and theb version will remain high-impedance (high).

When the V_{CC} supply reaches the range of 1 V, there is just enough supply voltage to weakly bias the input stage. At this point, the output can start responding to input signals, but proper output is still not ensured. This is shown as *Input Stage Starts Functioning* in Figure 3-9 and Figure 3-10.

Once the supply reaches 2 V, the input and output stage are fully biased, but the input voltage range is essentially zero (Vcc-2V). The inputs can properly respond to input voltages around zero volts. The input voltage range will now increase proportionally with the increasing supply voltage.

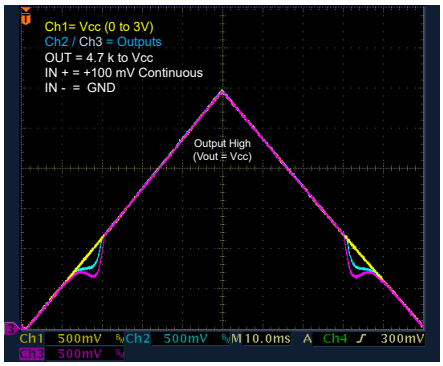


Figure 3-11. Start-up for B die, Output set high

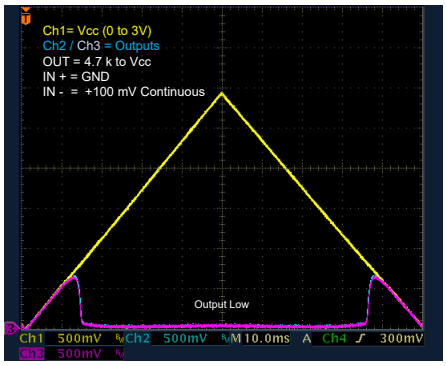


Figure 3-12. Start-up for B die, Output set low

For the B device, shown in Figure 3-11 and Figure 3-12, the behavior is similar, but the output goes high during the out of VCM range. Due to differences in the B process, the output awakens is a little higher at 0.7 V, and the input stage starts functioning at 1.2 V.

For circuits with a slow supply start-up ramp, it is a good idea to keep the operating threshold voltages low to make sure they are within the proper operating range as quickly as possible.

Similar effects can occur during power-down, but in reverse sequence. The remedies can be similar to power-up.

One way to make sure that the comparator is operational during power-down is to add a diode in series with the comparator circuit power supply (including any reference dividers), along with a large comparator bypass capacitor for storage. This way, when the main supply drops, the diode isolates the comparator from the main supply and *holds up* the comparator circuit supply allowing it to still function until the capacitor discharges. Since the LM339 family is an open collector output, the supply current is constant regardless of output state. Thought will be needed as to the pull-up and any reference divider voltage source sequence during power down.

3.10 Capacitors and Hysteresis

It is common to see designers add small value capacitors added to the inputs to provide filtering, either for EMI filtering or to filter or clean up the input signals.

One common oversight is to add a capacitor (C_F) to the non-inverting (IN+) node while utilizing hysteresis (positive feedback), as shown in Figure 3-13

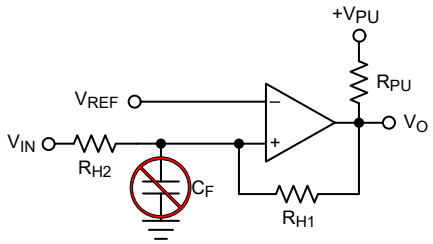


Figure 3-13. Example of Adding a Capacitor to IN+ While Using Hysteresis

Ideally, the hysteresis feedback through R_{H1} shifts the threshold slightly on the very first transition of the output, muting further transitions. Adding the capacitor C_F delays the hysteresis feedback, possibly allowing multiple transitions (bursting) before and after the transition, or even completely negating the hysteresis feedback action completely. Adding a large capacitor to the output can also have a similar effect (and may be asymmetrical due to the asymmetrical rise and fall times of a open-collector output).

Adding a capacitor to the inverting input is acceptable. The capacitor can be added to the non-inverting (IN+) node when hysteresis is not being used (no R_{H1}). If filtering is still required when using hysteresis, the capacitor needs to be placed to the left of R_{FB2}.

3.11 Output to Input Cross-Talk

To prevent oscillations and false-triggering, the output and input traces need to be kept separated when the source impedance is greater than 25kΩ, The fast output edge rates (< 200ns) can couple through the stray capacitance back into the high-impedance input, particularly at high output voltage swings (>10 V). This is important for the dual LMx93 where the inverting input is next to the output pin. The input and output traces must be run at right angles to each-other and never in parallel.

4 Output Stage Considerations

4.1 Output V_{OL} and I_{OL}

A critical graph for the output is the Output voltage vs Output Current graph, shown in Figure 4-1. From this graph, the output Low voltage can be determined from the expected sinking load current.

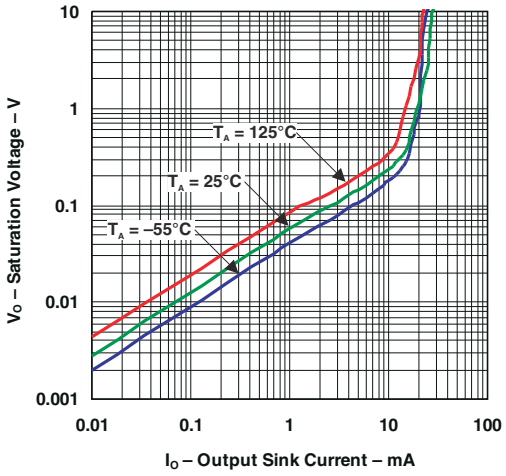


Figure 4-1. Typical Output Low (Saturation) Voltage vs Output Sinking Current

The graph also shows the current limit, where the output voltage sharply inflects upwards in the 10-20mA region. This region must be avoided as the specified minimum short circuit current is only 6mA (typically 12-16mA) and can vary across devices, lots and temperature. TI recommends sinking currents of less than 5mA.

This graph must also be used to determine the pull-up resistor value needed for a desired output low voltage.

For example, if a 3.3kΩ resistor is used on a 3.3 V pull-up voltage, the resulting current is 1mA when sinking. From the graph, 1mA will result in a worst-case (125°C) V_{OL} voltage of 90mV. However, if a 330 ohm pull-up resistor is used, the output low voltage is now 350mV, and is also uncomfortably close to the current limit.

4.2 Pull-Up Resistor Selection

An open collector output requires a pull-up resistor for the output to go High. An often overlooked design item is the pull-up resistor value. If the pull-up resistor value is too low, the output low pull-up current is excessive, which results in the output low voltage (V_{OL}) increasing, causing excessive output power dissipation and increased overall system supply currents. What is suitable for a 3.3 V pull-up voltage may not be suitable for a 24 V pull-up voltage!

If the pull-up resistor value is too high, this will result in a larger risetime. The risetime will vary with capacitive load as the risetime is dependent on the time constant of the pull-up resistor and the load capacitance. The result is an exponential risetime instead of a square edge and can effect the overall propagation delay. Falltime is not dependent on the pull-up resistor as the output transistor immediately shorts the output, quickly discharging the load capacitance through a low impedance.

The equation to determine risetime (10-90%), with 5k and 15pF example:

$$risetime = 2.2 * (R_{PULLUP} * C_{LOAD}) = 2.2 * (5k * 15pF) = 165ns \quad (1)$$

If risetime is not critical, a higher resistor value can be used to further save system power.

TI recommends a pull-up resistor sink current in the range of 100uA to 1mA for the best compromise of output swing and risetime. For example, With a 5 V pull-up voltage and 1mA current, the resistor value would be $V_{PULL-UP}$ / 1mA = 5kΩ. A 4.7k or 5.1k resistor would suffice, as the exact value is not critical. The proper pull-up resistor can be derived from the output saturation curve shown in Figure 4-1 above. With multiple

channel devices, be sure to include the power dissipation of each channel in the total package power dissipation calculation.

4.3 Short Circuit Sinking Current

The NPN output transistor has rudimentary self-current limiting. The current limiting protects the device from immediate damage. Device overheating can occur during prolonged shorts to VCC, especially when the VCC voltage is higher than 5 V. Note that power dissipation in the Comparator is $((V_{CC} – V_{OUT}) \times I_{OUT})$. The current limit magnitude decreases as die temperature increases.

The Comparator has no over-temperature shutdown circuitry. Therefore, excessive power dispassion can lead to very high die temperature. The data sheet absolute maximum ratings table warns that shorts to V_{CC} , for even very short periods, can lead to excessive heat dissipation and eventual destruction. Note that the power dissipation for each channel must be included in the total device dissipation calculation.

4.4 Pulling Output Up Above VCC

The output may be pulled-up to 36 V, independent of the supply voltage (even V_{CC} = 0 V!). Caution must be taken to ensure the output does not exceed the +36 V to -0.3 V limit. If the output is run off-board or past EMI producing devices, protection devices such as Zeners or TVS' must be used.

4.5 Negative Voltages Applied to Output

Similar to the inputs, any negative voltages applied to the output can cause similar effects as described in Section 3.8 above. Watch for inductive kick-back when driving inductive loads such as relays, transformers or long cables.

4.6 Adding Large Filter Capacitors To Output

Commonly designers will add large capacitors (100pF to >10uF) directly from the output to ground in an attempt to filter the output to reduce noise on the output or reset timing circuits. TI discourages this practice as it can cause several problems.

A charged capacitor can source peak currents of several amps. When the output goes low, the output must then short the charged capacitor, which causes the output to go into current limit. Long-term, this can stress the output. If discharging a capacitor with the output is desired, as in a timing application, a series current limiting resistor must be used to keep the peak current below 10mA or less. Adding the series resistor, with the appropriate adjustment to the capacitor value, will provide a more controlled discharge as it will swamp out the slight device variations in the short circuit current. If a series resistor is unacceptable, then a suitable external discrete pass transistor or MOSFET must be used.

Of course, adding the output capacitor increases the propagation delay by directly affecting the risetime and falltime.

Adding a large output capacitor will affect any added hysteresis feedback by adding a delay and slowing the output edges, resulting in bursting or outright cancellation of the hysteresis.

Instead, TI recommends filtering the input signal and using hysteresis instead of brute-force filtering of the output with a capacitor. These techniques can maintain the proper propagation delay while minimizing chatter or false triggers on noisy signals. Please see *AN-74 LM139/LM239/LM339 A Quad of Independently Functioning Comparators*, application note for more information about adding hysteresis to filter noise.

5 Power Supply Considerations

5.1 Supply Bypassing

The supply must be free of noise and transients to avoid false transitions. The recommended supply bypass capacitor is a 0.1uF ceramic capacitor. The capacitor must be placed as close to the supply pins as possible to a solid ground. Because the output is open-collector, the supply pin only supplies current for the comparator quiescent current, so load transient currents are minimal. Further bypassing must be at the pull-up resistor if it is located remotely. The GND pin must be returned to a solid ground as it will contain fast output load transients.

5.1.1 Low V_{CC} Guidance

The minimum V_{CC} for some devices in this family is 2 V. For lower supply voltages, such as those in the range of 2 V to 3 V, pay careful attention to the input voltage range. Note that the input range is especially limited at the device's lowest operating temperature, particularly the -40°C and -55°C devices. At a 2 V supply, the input voltage range limit is *at* 0 V over temperature. For supply voltages below 5 V, TI recommends devices optimized for low voltage operation, such as the TL331LV, LM393LV, LM339LV or TLV70x1 families of low voltage comparators.

5.1.2 Split Supply use

The LM339 Family may be used with split (±V) supplies, where the GND pin becomes V_{EE} or V- (the most negative supply voltage), provided that the difference between the supplies (V_{CC} - V_{EE}) does not exceed the specified maximum supply voltage (36 V). Do note that the output will now be swinging to the negative V_{EE} supply and not to common ground, so level shifting or external pass device may be necessary for ground referenced logic levels. Be mindful of the limited positive input voltage range at low split supply voltages. A +5 V/-5 V split supply will only have a -5 V to +2 V input range!

6 General Comparator Usage

6.1 Unused Comparator Connections

6.1.1 Do Not Connect Inputs Directly to Ground

For both used and unused comparators, the inputs must not be connected directly to ground or any other low impedance node. Always add some resistance to limit the current to less than 10 mA, regardless of any possible fault condition. All the input pins have a diode from the input to the device's GND, or V–, pin. In dual supply applications, the GND pin will be negative. However, during power up, power down, or supply faults, the GND pin may become positive. If this occurs then a grounded input pin will have potentially damaging current flow due to the input diode. Even if the GND pin is also grounded, such as in single supply applications, there is a possibility that the input ground will be negative relative to the op amp's internal ground node. Ground differences occur when there is poor layout or high current transients, $\Delta I/\Delta t$. Adding 1-kΩ to 10-kΩ series resistors to the input pin is acceptable in most applications.

6.1.2 Unused Comparator Input Connections

Occasionally applications will not need all the comparators in a dual or quad package. The unused channels must be connected in a way that is safe for the unused comparator and doesn't affect the used comparators. The best connection method puts the comparator into the normal operation range and no inputs are connected directly to low impedance nodes. The output of the comparator must be left open and not connected.

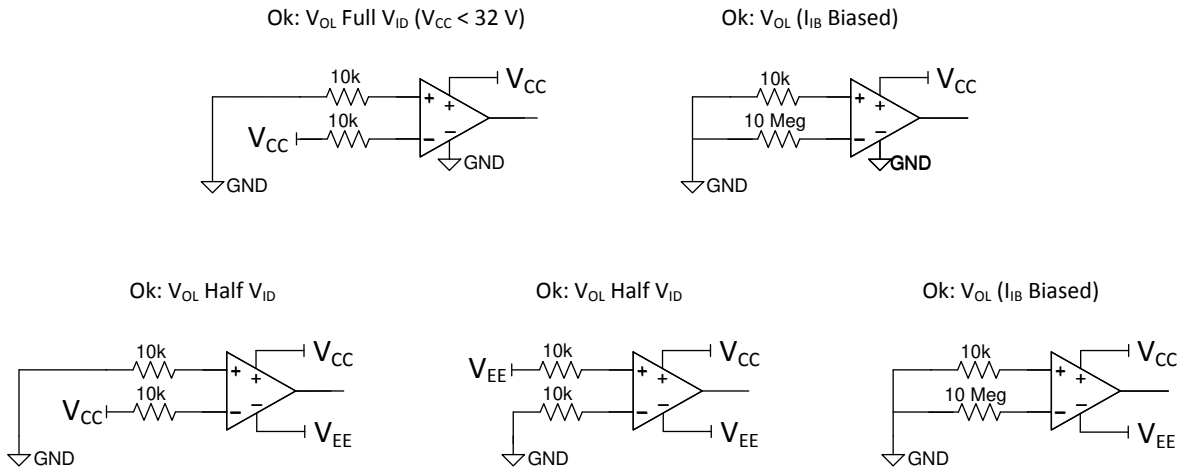


Figure 6-1. Best Connections Practices for Single and Dual Supplies

Increasing the input resistor to 10 MΩ would ensure linear operation as the input bias current (I_b), which flows out of the input pin towards ground, would raise the non-inverting input voltage beyond the input offset voltage

range. V_{OL} Full V_{ID} is better suited for lower voltage applications as there is no reason to apply a large input voltage difference even though the comparator allows it. The V_{OL} (I_{IB} Biased) method uses the input bias current to raise the voltage on the inverting input. If used, place the 10-MΩ resistor close to the inverting input pin to reduce noise pickup. No inputs may be connected directly to low impedance nodes such as ground, V_{CC} or V_{EE}. V_{OH} alternatives are also acceptable; just swap the input pins.

The next set of connections in Figure 6-2 is not recommended, but these configurations are not considered harmful methods of terminating unused channels. The V_{OH} alternatives that swap the inputs are also not recommended methods of terminating unused channels.

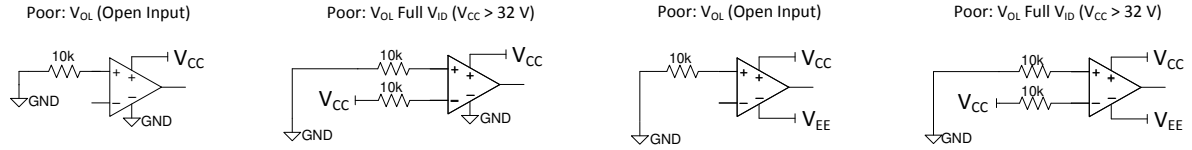


Figure 6-2. Less Than Acceptable Connection Practices for Single and Dual Supplies

The last set of connections, shown in Figure 6-3, demonstrates improper setups that could cause output noise chatter or device damage if the GND pin were to ever become positive relative to the input pin.

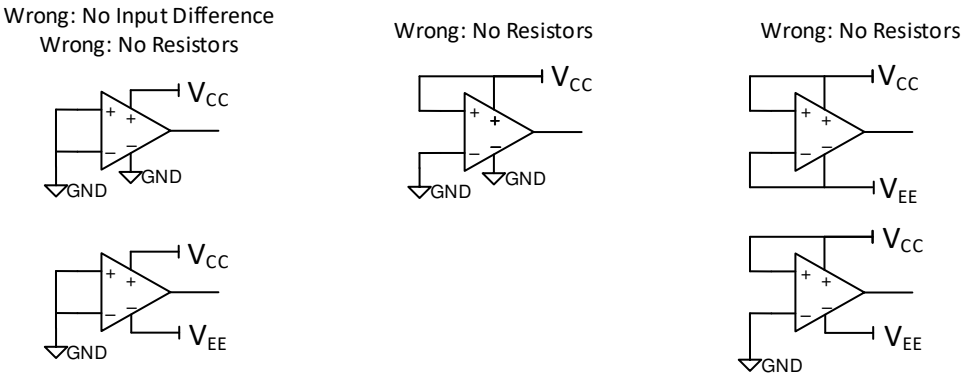


Figure 6-3. Potentially Harmful Connection Practices for Single and Dual Supplies

6.1.3 Leave Outputs Floating

TI recommends leaving the unused output pin floating. While it is possible to ground the output, as it cannot source current, there are leakage currents to V+ that can occur at high temperatures and high voltages, just as previously discussed for the inputs. To avoid any issues with these currents or other transient conditions, it is just best to let the outputs float.

6.1.4 Prototyping

If the board is a breadboard or prototype, not hard-wiring the inputs and leaving the outputs floating allows the future use of the unused channels if they are needed for fixes or expansion. The resistors can be removed and wires soldered to the pads or pins for breadboarding. This is true of all the multi-channel comparators, amplifiers and logic gates.

7 PSPICE and TINA TI Models

PSPICE models are available for both the classic and new "B" devices. The models are located in the respective product folders under the *Design & Development -> Design tools & simulation* tab. The core model is the same for the TINA and PSPICE model.

The models model typical behavior at room temperature, and since most of the family have similar typical at room, the model can be used for any device in the family.

There is an older, simple transistor-level model for the classic devices, and a newer model for the B devices.

Note

The newer B model has a feature that forces the output to one-half of the comparator supply voltage (Vcc/2), regardless of pull-up voltage, when the input range or supply range is violated. This is purposely designed to alert the user that there is a problem. The actual device will not do this and will react as described in the previous sections. The B model does not model the "one input within range" functionality, and instead will force the Vcc/2 output error if either input range is violated.

8 Conclusion

The LM339, LM393 and their variants are among the most popular, cost effective and long-lived standard comparators. Using this app note to understand their pros, cons and how they differ from more modern comparators will increase the likelihood of a successful design. Although most analog designers will continue to use these devices, improvements in op amp design, process technology and our understanding of comparator applications over the past four decades have led to the development of better and easier to use comparators.

9 Related Documentation

9.1 Related Links

The following lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

- Texas Instruments, *LMx39 (TI version) Core*, data sheet.
- Texas Instruments, *LMx39-N (National version) Core*, data sheet.
- Texas Instruments, *LMx93 Data Sheet (TI Version) Core*, data sheet.
- Texas Instruments, *LMx93-N (National Version) Core*, data sheet.
- Texas Instruments, *TL331 Core*, data sheet.
- Texas Instruments, *LM397*, data sheet.
- Texas Instruments, *AN-74 – A Quad of Independently Functioning Comparators*, application note.
- Texas Instruments, *TI Precision Labs – Op Amps: Comparator Applications (Comparators section)*.
- Texas Instruments, *Analog Engineers Circuit Cookbook: Amplifiers (Comparators Applications section).*
- Texas Instruments, *Comparator Input Types*

10 Revision History

Changes from Revision C (April 2023) to Revision D (December 2023) **Page**

- Added Quad to PCN Information section, Re-ordered sections....5
- Added Determine Die Used for Single and Dual section....5
- Added Determine Die Type for Quads....6
- Added Device PCN Summary table....6
- Added Changes To Part Markings section....7
- Updated input range behavior into separate sections....11
- Deleted mention of clamp for LM339B....11
- Added Maximum Input Current section....12
- Added Power-up behavior section....14
- Added Capacitors and Hysteresis section....15
- Added PSPICE model section....21

Changes from Revision B (August 2021) to Revision C (April 2023) **Page**

- Added *New TL331B, TL391B, LM339B, LM393B, LM2901B and LM2903B B versions* topic....4
- Added PCN information....5
- Added description of B input stage....8
- Added *Differences Between the Classic and B Die Devices* 8

Changes from Revision A (March 2020) to Revision B (August 2021) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document....2

Changes from Revision * (April 2019) to Revision A (February 2020) **Page**

- Added LM393B and LM2903B 1

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