LMG1210 Optimizing GaN RF Power Amplifiers

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1 Introduction

The advantages of using GaN FETs outweigh Silicon MOSFETs for many emerging high-speed applications topologies based on DC/DC buck converters, such as RF power amplifiers (RFPA), radio transmitters in telecommunication base stations, and wireless data transmission. The transmitter in a RFPA can waste a lot of power as heat whether idling or in operation, so different power modulation techniques are employed to allow the power amplifier to follow the optimal power level that the signal needs for amplification. With power levels up to hundreds of watts, linear amplifiers produce about 50% efficiency. However, using GaN FETs with a class D topology, switching amplifiers now have a peak efficiency above 90%. This increase in efficiency allows baseband stations to save money on electricity and maintenance and 5G users to save battery life and talk time. One of the most important aspects of RFPA circuit design is choosing a high-performance gate driver. A GaN FET and high-performance GaN driver can deliver high-performance RF power when considering the gate drive circuit's PCB layout and minimal dead-time among the driver's propagation delay variation and other variables to distortion-free RF signal amplification. LMG1210 has the ability to improve the performance of a RFPA by switching up to 50 MHz with 5-V gate drive, enabling tight layout for high-performance GaN, obtaining precise dead-time minimization for maximizing efficiency at full load, and more.

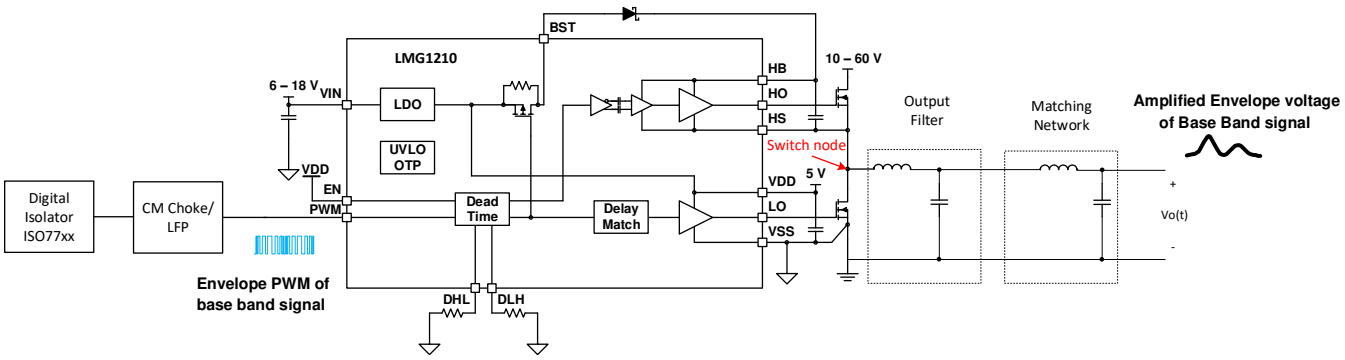

Figure 1. LMG1210 Driving Class D Envelope Amplifier for RFPA

1.1 Class D, LMG1210, and RFPA

Class D amplifiers were originally used in audio applications to provide sufficient power to a low-impedance, forever changing load modulated to resemble the analog audio waveform. Since the signals are similar in shape just faster in speed, class D amplifiers are used because they can theoretically achieve 100% efficiency, disregarding all layout and FET parasitics. Class D amps operate with FETs in saturation to achieve a near ideal square switch node waveform. By driving the FET fast with high-peak source and sink current GaN can help with the high slew rates of high-frequency, peak-power signals. The input of the LMG1210 can be driven with a single PWM pin signal to drive the dead-time of the half bridge as short as possible. With one PWM input, two HO and LO output signals can be generated, as found in Figure 13 from the *LMG1210 200-V, 1.5-A, 3-A Half-Bridge MOSFET and GaN FET Driver with Adjustable Dead Time for Applications up to 50 MHz Data Sheet*. The PWM pin input signal can be modulated to the shape of the RF input with an envelope detector to filter out the DC. The DC envelope of the RF input is analyzed and recreated in the form of pulse width modulation (PWM), shown in blue in Figure 1. This PWM signal represents a modulated form of the envelope of the input signal. The switching frequencies needed for sufficient bandwidth are so high that ground bounce can occur due to common source

inductance and layout parasitics that can negatively affect the input signal and controller. So separate digital isolators and input filters can be used on each input to help remove noise or ground bounce that reaches the input side. This PWM signal is accepted by the PWM pin of the LMG1210, and is transferred to the switch node using HO. The DC voltage is pulsed by LMG1210 and GaN to the switch node and filtered output. When filtered out, the output voltage is just above the envelope voltage, so minimal power is lost as heat as opposed to using a fixed supply as shown in Figure 3. This technique can be thought of as chopping up the DC power supply at a duty cycle that modulates the RF power to match the envelope of the input signal. The output filter removes any switching harmonics, and the matching network creates the interface between the transmission line and the antenna for optimal efficiency at the resonant frequency of the system.

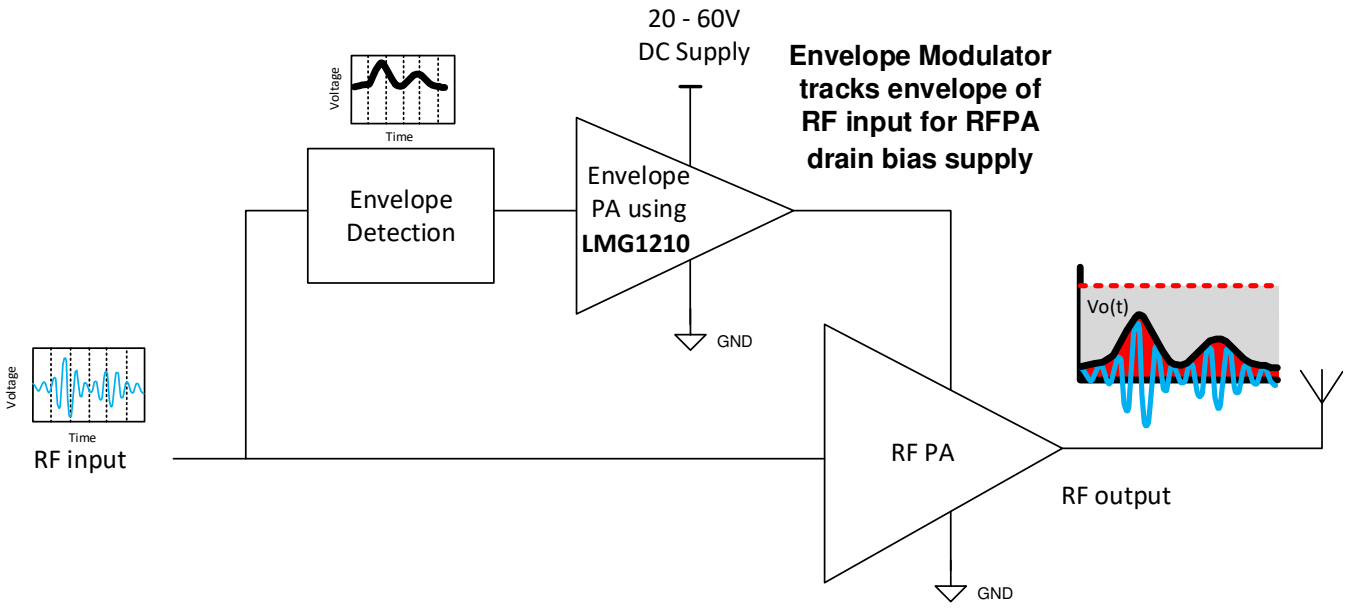

Figure 2. RFPA Envelope Tracking

1.2 RFPA Envelope Tracking with LMG1210

The RFPA needs a mechanism like Envelope Tracking (ET) to separate the power from the signal. Operating the amplifier in the red region of the plot in Figure 3 eliminates the unused power when using a fixed supply. The RF input found in Figure 1 consists of a low-voltage AC waveform, similar to an audio signal with much higher frequency. A DC filter reads the shape of the signal, and an envelope detection modulator creates a PWM representation of the envelope. The LMG1210 steps in to switch the power required with as little delay to make sure the amplification is happening at the right time as efficiently as possible with minimal dead-time. In PWM mode, the max propagation delay of the LMG1210 of 11 ns turning off and 11 ns plus the dead-time to turn on allows low distortion of the switch node waveform. The output of the RFPA to the antenna, if done correctly, looks like the plot above the RF output found in Figure 2. The need of the RFPA for a high-bandwidth (BW) solution up to 100 MHz per channel for 5G-LTE, as well as high efficiency to amplify high-power RF frequency signals. To achieve 100-MHz BW per channel, multiple phases are needed and, to achieve higher power multiple, FETs are paralleled. Since 4G allows for 20-MHz BW per channel and 5G allows for 100-MHz BW per channel 5G offers higher bandwidth and data speeds. With a 5G multi-carrier system, the RFPA may require higher peak power to prevent clipping the signal, which means higher slew rates on the switch node for higher peak to average power ratio (PAPR) RF output signal frequencies. In a multi-carrier architecture wireless data transmission, where there are multiple channels combined, a frequency division multiplexing technique is performed to increase wireless data speeds. When the different frequency carriers are out of phase with each other, their peaks add up and produce a high PAPR, which is expressed in dB. 5G signals can have above 10-dB PAPR signals, which require low impedance outputs to achieve the high power slew rates to prevent clipping.

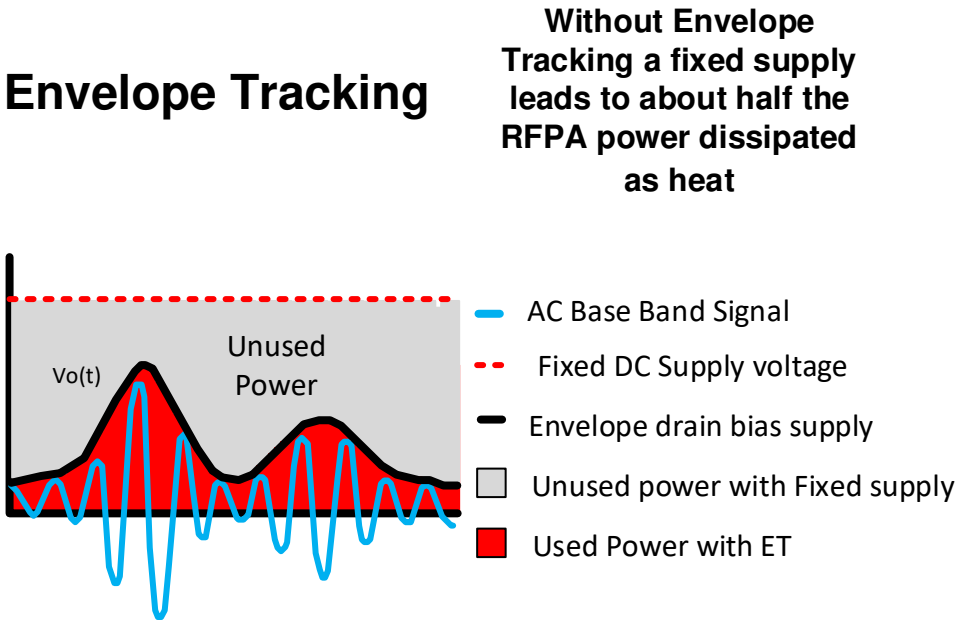

Figure 3. Envelope Tracking versus Using a Fixed Supply

1.2.1 Optimal RFPA Layout Recommendations with LMG1210

The placement and routing for the RFPA supply is very important to achieve high performance with GaN. For a very high-frequency parallel or multi-phase half bridge layout design, the FETs and driver connection and placement must be symmetrical. The FETs placed a similar distance from the driver to prevent one FET turning on nanoseconds before the other. A good layout can also help prevent the following:

- Ground bounce
- Gate overshoot
- Thermal problems
- EMI noise
- Better matching networks

The key to a good layout is to place the component in such a way that allows the shortest and widest connection possible. For the lowest inductance connection, that means putting the gate driver and all the FETs in the power stage on the top layer in the smallest area. Knowing the high current loops on the schematic, as well as PCB, can help to achieve higher power and efficiency when using parallel FETs and multiple phases. Paralleling FETs divides the current per FET, increasing the power capability and increasing the efficiency by reducing conduction loss with lower R_{dson}. Multiple phases are good for the matching network to efficiently couple RFPA output from the antenna, as well as decrease the output impedance to increase the BW. From the perspective of the output, for maximum RF power transfer efficiency to the antenna, the impedance of the load must match the impedance of the source to minimize power loss from reflections.

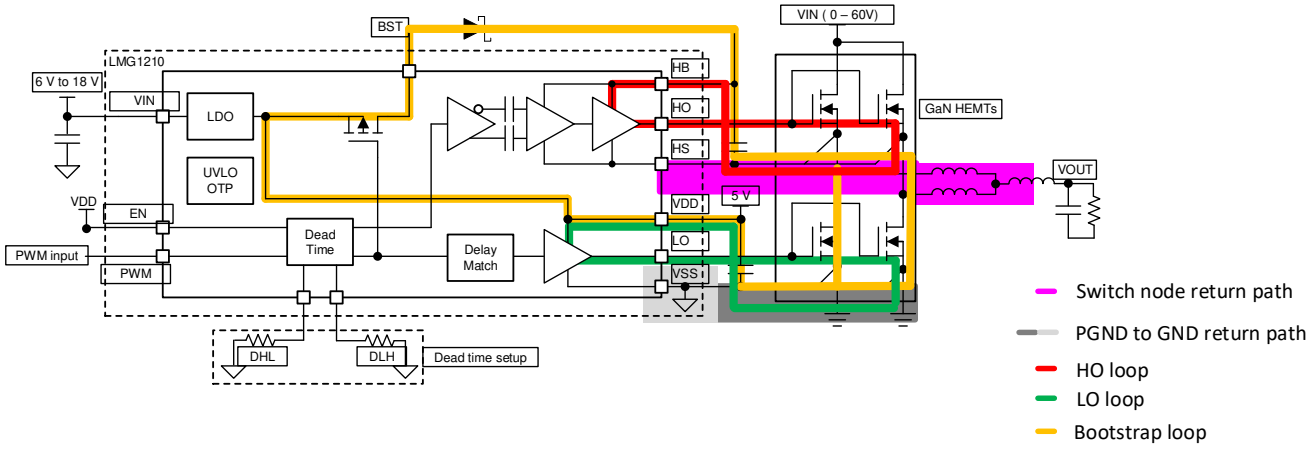

Figure 4. TIDA-01634 Essential Gate Loops Colored System Block Diagram

SW-HS and PGND-GND Source Return Connection

Figure 4 shows a schematic view of the important gate loops in the *TI Designs: TIDA-01634 Multi-MHz GaN Power Stage Reference Design for High-Speed DC/DC Converters*. Figure 9, Figure 7, and Figure 4 show the layout in further color-coded gate loop detail. For more layout details on the TIDA-01634, see the FETs Paralleling section from *Multi-MHz GaN Power Stage Reference Design for High-Speed DC/DC Converters Design Guide*. The switch node is colored pink. The wide pad represents a low-inductance plane. The other planes are PGND (dark gray) and GND (light gray) as well as the power input and output planes. The other colors represent the gate loops. The large HB-HS charge path is orange, the HO-HS loop is red, and the LO-GND loop is green. The switch node (SW) connection to the LMG1210 HS pin is the most over-looked layout connection for the gate driver. The switch node waveform shows how the HO and LO with dead-time perform together. The switch node waveform can diagnose how much dead-time can be minimized, if thermal problems are too slow, and if noise issues are too fast. Parasitic inductance and capacitance connected to the switch node rings at the resonant frequency, especially when the converter current reaches peak di/dt. For topologies that combine multiple half bridges together at the switch node, there may need to be inductance to connect each switch node to balance oscillations to achieve the same amount of current through each half bridge. As peak current at high frequency follows the path of least impedance through parallel FETs, the additional switch node inductance connecting the inductor smooths the current peaks out so they better align.

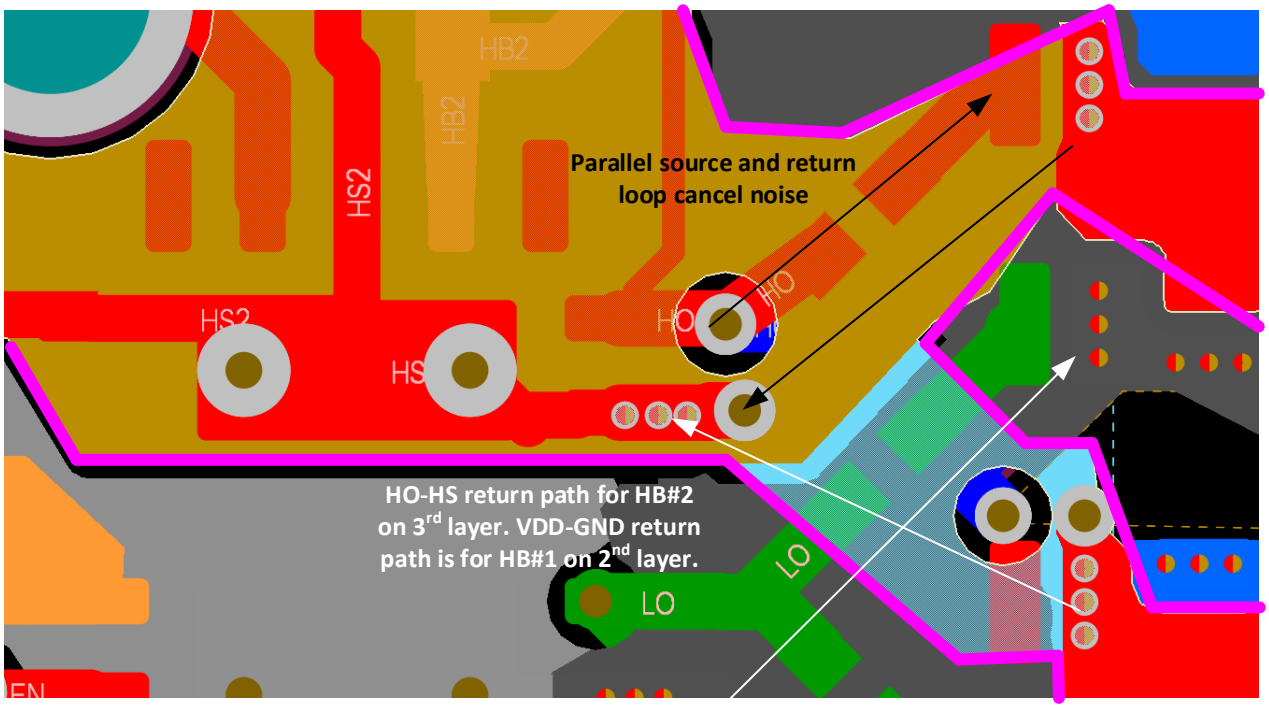

Figure 5. Gate Drive Loop Layout for High-Side FET

The most over-looked layout connection as mentioned is the shared source return (pink HS plane) back to the driver, which completes the loop and can be found in Figure 5. In this case, the switch node (HS) is outlined pink, the power ground (PGND) is dark gray, and the driver ground (GND) is light gray. The HS plane and PGND plane must connect to the driver pins at one point. In this case, they are connected with three in-pad vias. To keep the return loops as short as possible, micro-vias or in-pad vias are used. Using a plane and taking advantage of the vertical current path rather than lateral on the adjacent layer is essential to making a low-inductance connection for high-frequency switching. If the vias are not placed close to the driver pin and FET pin, the common source inductance can cause gate voltage to fall as the switch node experiences high dv/dt. If the gate voltage falls close to UVLO, the GaN does not drive to saturation, which causes the following:

- Power loss
- Non-linearity
- Oscillations
- EMI

Figure 5 also shows how to use the middle layers to route the VIN, HS, and PGND planes, weaving them for low inductance connections to the FETs as shown in Figure 7. The mid-layer planes can require the HS and PGND planes to overlap each other. The most difficult part of routing parallel FETs is avoiding overlapping the HS and PGND planes, and must be limited to less than about 100 square mils. Overlapping planes adds parasitic layout capacitance to the switch node, which slows down dv/dt as well as couples damaging oscillations to the input and output.

HO-HS and LO-GND Loops

Since the placement of the FETs are close to the driver, the connections from the gate output to the gate of the FET must be around 100 mil short and as wide as possible to keep loops low-inductance. Gate resistors can be used to limit overshoot but slow down the maximum operating frequency. The turn-on gate resistor is used to avoid overshoot, since the maximum GaN gate voltage is 6 V, as well as oscillations and excessive switch node dv/dt since the maximum CMTI for LMG1210 is 300 V/ns. These connections must be equal trace length to limit part-to-part or gate-to-gate delay variation. Symmetry achieved with careful placement helps set up easy routing. The HO-HS loop is red in Figure 4 and the LO-GND loop is green at a 45° angle to achieve equal gate trace length, as shown in Figure 6. The second

HO gate on the bottom half-bridge is routed on the bottom layer to keep equal gate lengths, as shown in Figure 6. In this case, the current flow on the input of FET gate is the opposite of the ground current return, which offsets the magnetic field and reduces PCB stray inductance, as shown in Figure 5. FET selection is important to achieving a good gate loop. The output trace may need a via to reach the source. When using vias on the output gate loop, the vias must be placed as close to the output pin or as close to the gate pad as possible to help avoid common source inductance in the gate loop. Although a two-layer board can be used, a four-layer board helps with low-inductance, high-frequency performance. However, more layers can be added for paralleling more FETs or more phases.

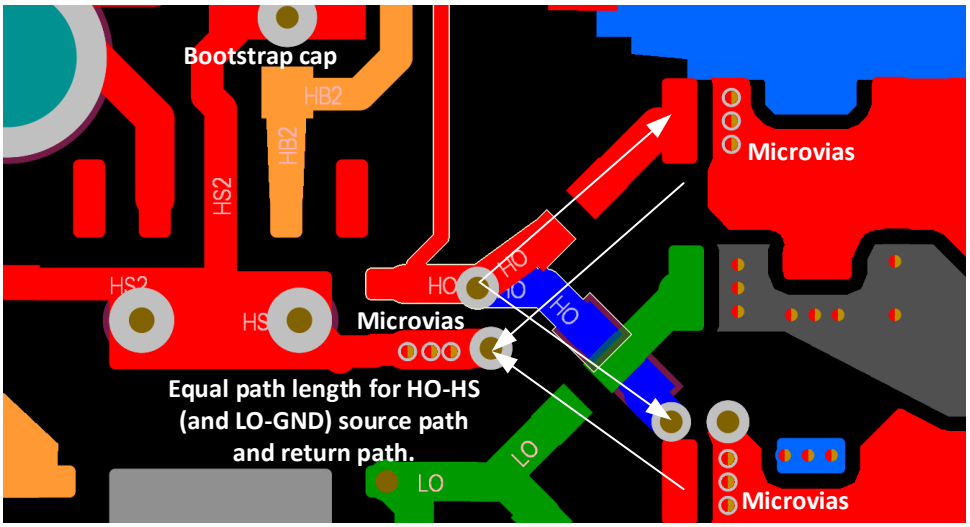

Figure 6. Gate Drive Path for Paralleled FETs

VDD-GND and HB-HS Cap Loops

VDD and the bootstrap (HB-HS) cap placement are also important to achieving a tight gate loop since the high-peak source current of the driver is sourced from these caps. The VDD cap is light green and is contained in the LO-GND green gate loop. It is highlighted as a reminder of this. The bootstrap HB node and the bootstrap charging path are orange, as seen in Figure 4. The placement of the VDD and bootstrap cap must be as close as possible to the pins. In this case, the VDD and HB cap are feedthrough caps to further minimize the lead inductance and the overall loop inductance of the VDD-VSS and HB-HS gate loops. Place the VDD and HB-HS caps on top layer about 100 mil from the center of the thermal pad. The thermal pad and pinout of LMG1210 help route the gate loops with low inductance and allow a simple connection of the HS and VSS pins back to the thermal pad. The two separate thermal pads also allow the lowest inductance connections for the source return path back to the driver. To minimize the gate loop inductance in the vertical z-direction and into the PCB board, use micro-vias to connect to the HS and GND plane on the adjacent layer. The LMG1210 has multiple HS pins to allow different HB cap placement and low-inductance connection to the FET source through an HS return plane.

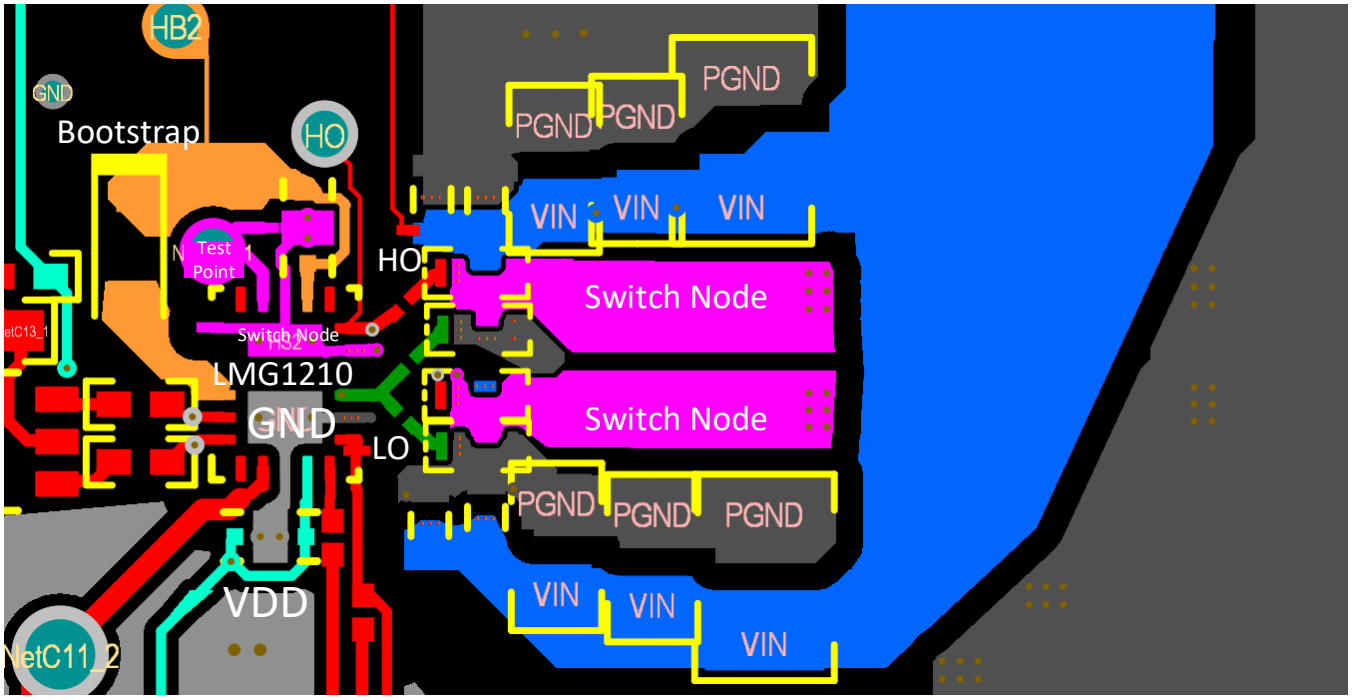

Figure 7. TIDA-01634 LMG1210 Layout Top Layer

Bootstrap Charge Loop

Every switching cycle, the bootstrap cap, found in Figure 6, starts charging after the switch node or HS pin is pulled to ground using the low-side FETs. This means the bootstrap charging path includes part of the power loop as well as the driver loop. The bootstrap path includes the following:

- LMG1210
- BST diode
- HB cap
- Low-side FETs

The bootstrap path is colored orange in Figure 4. The bootstrap cap must be very close to the BST and HB pins to allow low inductance and fast charging. The bootstrap diode must be low forward voltage to supply at least 4 V peak to HB node, and low capacitance to prevent additional parasitic capacitance and Coss power loss on the switch node. The bootstrap path can see high-peak current for charging in nanoseconds, so the connections around the driver needs to be as wide and short as possible. To charge the bootstrap cap as fast as possible while switching at 50 MHz, see section 7 from the *Get the Most Power from a Half-Bridge with High-Frequency Controllable Precision Dead Time Application Report*. To further improve the bootstrap loop in this case, the HS probe 'test point' is restricting the bootstrap cap loop area and must be removed if not needed.

1.2.1.1 Analyzing TIDA-01634 with the Shortest Dead-time Possible

To optimally switch the GaN power stage at peak efficiency, control the dead-time as short as possible, minimize the solution size, and keep thermal dissipation down. Perhaps the most important part of driving GaN is achieving a minimal dead-time, preventing third quadrant conduction. For further details on GaN third-quadrant conduction, see section 2 of the *Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN Application Report*, *Get the Most Power from a Half-Bridge with High-Frequency Controllable Precision Dead Time Application Report*, and *Optimizing Efficiency Through Dead Time Control With the LMG1210 GaN Driver Application Report*. Achieving below 5-ns dead-time on a board, such as the TIDA-01634 as shown in Figure 8, is easy for any static set of operating conditions. However, once the load, temperature, part-to-part variation, and PCB parasitics are changing, the dead-time becomes harder to control. Although with the dead-time control, the LMG1210 prevents the outputs

from overlapping, it is still possible that high-frequency, high dv/dt circuit operation can cause shoot through of the power stage. To obtain a short dead-time for high-side off to low-side on (HL) and low-side off to high-side on (LH) transitions, it helps to know more about the nature of the transitions. In buck-based DC/DC converters, one transition is hard-switched and one is soft-switched. The hard-switched one is when there is current flowing when switched. Since this is the free-wheeling nature of the synchronous FET, the HL transition is hard-switched, as shown in Figure 8. The HL dead time can be fixed to make sure the hard-switched edge does not become even more hard-switched. When measured using HO and LO, the dead time is not representative of the DHL and DLH resistor values. This can be contributed to an effect where some of the HO to LO dead-time disappears during the resonance between the Coss of upper FET and inductor current. This happens during the transition for the upper FET voltage to increase, that is the switch node voltage to drop. From the switch node voltage waveform, the dead-time can be manually measured with cursors shown in red about 1 V in to and out of the undershoot part of the switch node waveform shown in Figure 8. This manual measurement yields approximately 1.5 ns HL dead time.

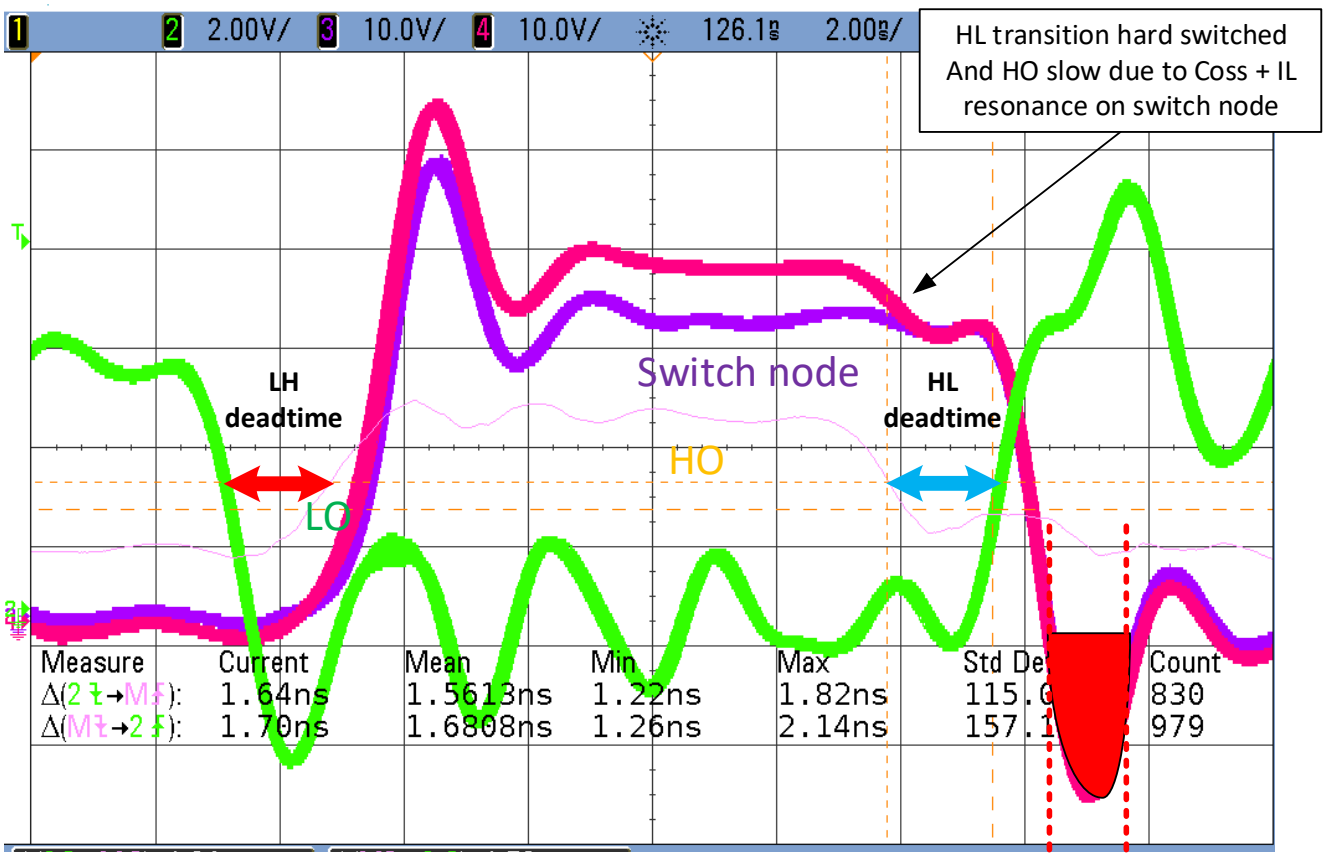

Figure 8. TIDA-01634 Operating at 40 V 30 MHz at 3-A Load with Minimum Dead Time

A more exact measurement of the dead-time can be realized by understanding that the HO signal drops slower because it is the sum of switch node and real HO gate signal. To see the true HO signal and realize the true LH dead time, use a math function in the scope to calculate HO minus the switch node waveform to see the true high-side gate signal, as shown in Figure 8. This automatic math measurement yields a mean value of 1.68-ns HL dead time and 1.56-ns for LH dead time. The LH dead time is soft-switched, and must be able to achieve shorter dead times since a negative dead-time (shoot-through) does not have as much effect on the system as negative dead time on a hard-switched edge. The LH dead time can be adapted to the load in real time with the dead-time control of the LMG1210 to make sure the LH transition stays soft-switched. For more details using a DAC to control the dead-time of the LMG1210 in real time, see the *Get the Most Power from a Half-Bridge with High-Frequency Controllable Precision Dead Time Application Report*. When attempting to fine tune the dead-time, make sure to start without a bus voltage, then slowly apply a bus voltage to see the effects. Typically a load has to be applied to see the true effects of the dead time on the system. A consistent switch node rise and fall time is necessary to prevent distorting the amplified RF signal shape. One thing that the switch node waveform

can convey is how much jitter the gate driver is producing using the persistence function on the oscilloscope as shown in Figure 9. The lower the switch node jitter, the less pulse width distortion that can give a different voltage amplitude with the same input pulse. The width of the persistence shows how much the output pulse width varies for the same input pulse width. The average width of the switch node is about 500 ps which verifies tight PWM mode delay matching between turn on and turn off from the PWM input to the switch node.

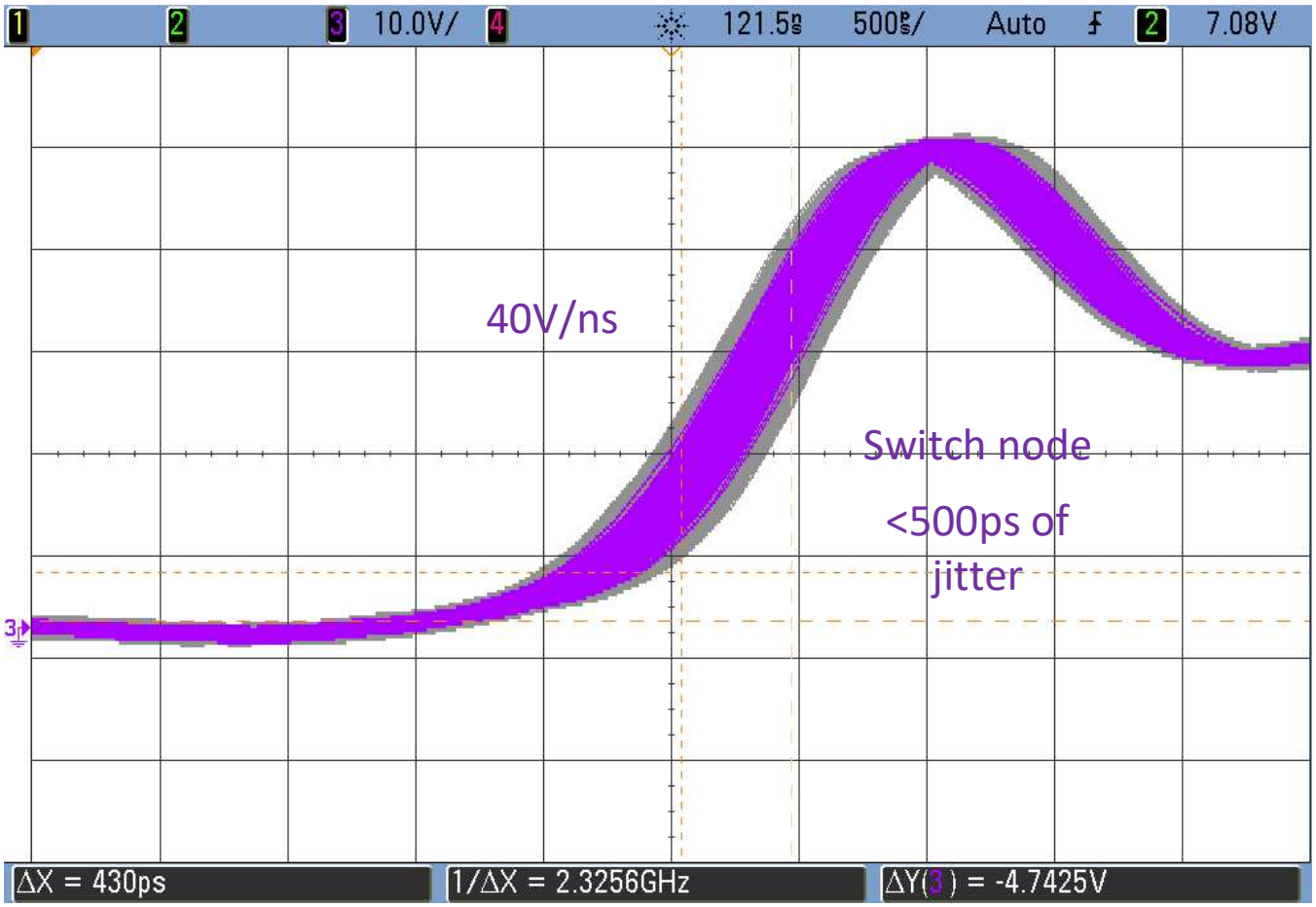

Figure 9. TIDA-01634 Operating at 30 MHz with 500 ps of Switch Node Jitter

2 Summary

Over time, amplifier efficiency has come from 50% with the class AB fixed supply to above 90% by adding a non-linear switching PA employed to handle high-power transients. This lowers the power loss of the linear amp and allows the Class D switching amplifier topology to advance in popularity, especially after GaN FETs became mainstream. GaN allows a higher switching frequency to avoid needing to use inefficient linear amplifiers. GaN also lowers conduction losses by reducing the supply current and increasing the supply voltage, making it make even more sense to parallel GaN half bridges to achieve higher power. Compared to MOSFETs, a smaller size FET for the same R_{dson} and zero reverse recovery are integral for optimal DC/DC RF amplifier performance. While driving high-current through GaN, watch out for optimal layout, especially gate driver layout, and minimizing reverse conduction loss by using the PWM mode of the LMG1210 to control a minimum dead time. A good layout can help prevent the following:

- Ground bounce
- Gate overshoot
- Thermal problems
- EMI noise

- Better matching networks

The key to a good layout is to place the component in such a way that allows the shortest and widest connection possible. Perhaps the most important part of driving GaN is achieving a minimal dead time preventing third quadrant conduction. Achieving dead time below 5 ns on a board, such as the TIDA-01634, is easy, but high dv/dt circuit operation can still cause shoot-through. Following optimal layout recommendations from *Section 3* and *Section 1.2.1*, as well as understanding how the dead-time is measured and fine tuned under high-frequency conditions found in *Section 1.2.1.1*, allows the best performance using the LMG1210 to drive a GaN Half Bridge for RF Power amplifiers.

3 Related Documentation

- Texas Instruments, *TIDA-01634 Multi-MHz GaN Power Stage Reference Design for High-Speed DC/DC Converters Reference Design*
- Texas Instruments, *LMG1210 200-V Half-Bridge MOSFET and GaN FET Driver Data Sheet*
- Texas Instruments, *Using the LMG1210EVM-012 User's Guide*
- Texas Instruments, *Design Considerations for LMG1205 GaN FET Driver for High-Frequency Operation Application Report*
- Texas Instruments, *Dead Time Optimization LMG1210 GaN Driver Application Report*
- Texas Instruments, *Achieve Cooler Thermals and Less Power Loss of Your GaN Half-Bridge Design with the LMG1210 Application Report*
- Texas Instruments, *Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN Application Report*
- Texas Instruments, *Get the Most Power from a Half-Bridge with High-Frequency Controllable Precision Dead Time*

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