Application Brief

Space-Grade, 50-krad, 2-Wire, Discrete 4–20-mA Current Transmitter Circuit

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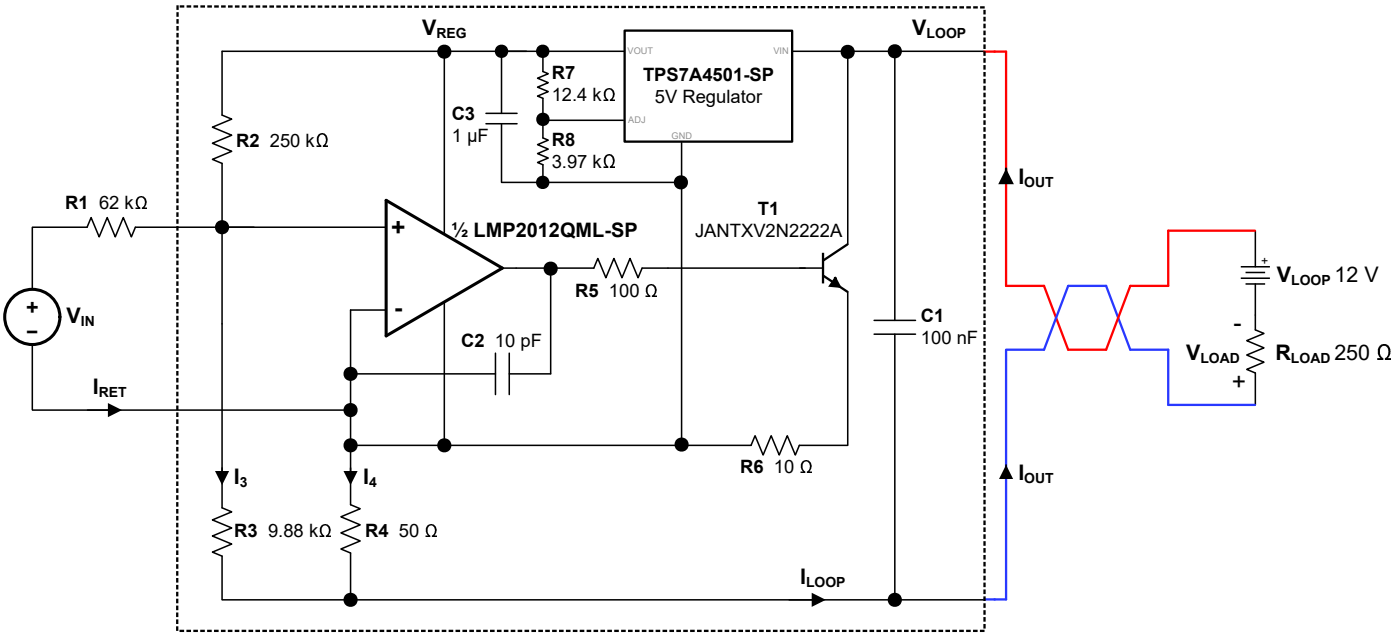
Design Goals

Input		Output		Supply	Load	Total Ionizing Dose	SEL Immunity
V_{in_min}	V_{in_max}	I_{out_min}	I_{out_max}	V_{loop}	R_{load}	≥ 50 krad(Si)	≥ 77.5 MeV·cm^2/mg
0 V	5 V	4 mA	20 mA	12 V	250 Ω		

Design Description

This design uses discrete components to implement a 4- to 20-mA V-to-I current transmitter designed using space-grade (SP) components for use in space applications. The circuit converts a differential voltage to a current which can be transmitted over a long cable. Linear operation of this current transmitter depends on the op amp input common-mode range, the headroom available for the transistor and LDO, and linear matching of currents through R_3 and R_4 across the input voltage range. Since the inverting input to the op amp is tied to its negative supply, the op amp must support common-mode voltages to its negative rail. It is important that 2-wire loop-powered current transmitters plus any peripherals that are on the same supply loop consume less quiescent current than the minimum output current because the loop return current flows through the output path.



Design Notes

1. Use low-tolerance resistors to achieve high current gain matching accuracy.
2. All resistors and capacitors must be verified space-grade for this design.
3. In this design, I_{ret} is a local ground, separate from the supply ground, and must be allowed to float.
4. The current through R_3 can be considered a quiescent current. That is, it is a current that should be minimized so as to not use up the current budget. However, as I_3 gets smaller, the matching ratio R_3 / R_4 gets larger, so in practice I_3 cannot be made arbitrarily small.
5. For linear operation, the ratio of the current through R_3 when $V_{in} = V_{in\_max}$ and $V_{in} = V_{in\_min}$, I_{3_max} / I_{3_min}, must be equal to the ratio of the maximum output current to the minimum output current, I_{out_max} / $I_{out\text{-}min}$.
6. This discrete 2-wire current transmitter solution allows the flexibility to set the output current to be different than the standard 4–20 mA or 4–24 mA. This may be necessary because options for space-grade components are relatively limited. For example, if the total quiescent current for the current transmitter plus surrounding peripherals on the same supply loop cannot meet the requirement that they sum to less than I_{out_min} (= 4 mA for this design), the output current range may be shifted to 8–24 mA or something similar.
7. C_1 is a bypass compensation capacitor and is required for the stability of the circuit. Recommended capacitor is 100 nF or greater.
8. R_5 and C_2 are additional components for compensating the circuit. They are not required for stability, but are added for flexibility if additional compensation is required.
9. C_3 is a required output capacitor for the TPS7A4501-SP. Recommended capacitor is 1 µF to 10 µF for stability.
10. R_6 linearizes the relationship between the op-amp output and the current through the transistor and limits the current through the transistor.
11. This design can be implemented with a single LMP2012QML-SP or a similar device. See Design Alternate Op Amp for an alternative device.

Theory of Operation

A 4–20-mA V-to-I current transmitter takes a differential voltage as the input and outputs a current with a linear relationship from input to output. This linear relationship depends on the common-mode range of the op amp and the headroom available for the transistor and LDO. Furthermore, a current transmitter designed with a 2-wire loop requires that the quiescent current drawn from all components on the loop path consume less than the minimum output current I_{out_min} – 4 mA in this design. This includes the op amp, LDO, the current through the R_3 and R_5 branch, and any other peripherals that are on the same supply loop. As long as this requirement is met, the op amp and transistor compensate to supply the remaining current to the loop to output the correct current to the load resistor.

The output current I_{out} is the sum of the currents through R_3 and R_4, I_3, and I_4, respectively:

$$I_{out} = I_3 + I_4$$

I_3 is set by R_1 and R_2, along with the input voltage V_{in} and regulated supply V_{reg}. Under ideal operation, the non-inverting terminal of the op amp has a virtual short to the local ground, I_{ret}. Notice also that V_{reg} and V_{in} are referenced to I_{ret}. I_3 is then the following:

$$I_3 = \frac{V_{in}}{R_1} + \frac{V_{reg}}{R_2}$$

I_4 is the sum of the local ground return current I_{ret} and the compensating current through the transistor T_1.

For correct operation of the op amp, the voltages across R_3 and R_4 must be equal, so we have $V_3 = V_4$ and it follows that:

$$I_3 R_3 = I_4 R_4$$

The previous equation is rewritten as:

$$I_4 = I_3 \frac{R_3}{R_4}$$

Combining the first equation, second equation, and previous equation, the transfer function for the circuit is derived as:

$$I_{out} = \left(\frac{V_{reg}}{R_2} + \frac{V_{in}}{R_1}\right)\left(1 + \frac{R_3}{R_4}\right) = I_3\left(1 + \frac{R_3}{R_4}\right)$$

It is apparent, then, that the current through R_3 that is set by R_1, R_2, V_{in}, and V_{reg} is amplified by the factor $1 + R_3 / R_4$.

Design Steps

See the Design References section for an Excel calculator that calculates the resistor values for the required specifications.

1. Define the input voltage range for the circuit. For this design V_{in_min} = 0 V, V_{in_max} = 5 V is chosen.
2. Define the output current range for the circuit. For this design I_{out_min} = 4 mA, I_{out_max} = 20 mA is selected.
3. Calculate R_7 and R_8 to set the output voltage for the TPS7A4501-SP LDO. The equation to set the output voltage for this adjustable LDO follows:

$$V_{reg} = V_{ref} * \left(1 + \frac{R_7}{R_8}\right)$$

In this equation, V_{ref} is the internal bandgap reference voltage for the LDO. TPS7A4501-SP has a nominal reference voltage V_{ref} = 1.21 V and this design is targeting V_{reg} = 5 V, so the following applies:

$$5V = 1.21V * \left(1 + \frac{R_7}{R_8}\right)$$

$$\frac{R_7}{R_8} = 3.13$$

To choose values, the following guideline is used: The current in the feedback resistors from output to ground of an LDO must be at least 100 times the leakage current into the ADJ pin to avoid output accuracy issues. For TPS7A4501-SP, the leakage current of the ADJ pin is 3 µA (typ). This yields the following inequality:

$$\frac{V_{reg}}{R_7 + R_8} \geq 100 * 3\mu A$$

$$\frac{5V}{R_7 + R_8} \geq 300\mu A$$

16.67 kΩ ≥ R_7 + R_8

With R_8 = 3.97 kΩ (standard value), the following equation is true:

R_7 = 3.97 kΩ * 3.13 = 12,426 Ω ≈ 12.4 kΩ (standard value)

With these values for R_7 and R_8, the following equation is valid:

R_7 + R_8 = 3.97 kΩ + 12.4 kΩ = 16.37 kΩ ≤ 16.67 kΩ

Note

Since this design has a current budget limitation, it is desirable to size R_7 and R_8 to be near the limit to minimize this quiescent current contribution.

4. Define the minimum and maximum currents through R_3. See Design Note #5 before defining these currents. For this design, I_{3_min} = 20 µA, I_{3_max} = 100 µA, is chosen.

5. Calculate the values for R_1 and R_2 to set I_{3_min} and I_{3_max} as defined in Design Step #4. To do this, use the first equation along with the specifications for V_{reg}, V_{in_min}, V_{in_max}, I_{3_min} and I_{3_max}. When $V_{in} = V_{in\_min}$, the following equations occur:

$$I_{3\_min} = \frac{V_{in\_min}}{R_1} + \frac{V_{reg}}{R_2}$$

$$20\mu A = \frac{0V}{R_1} + \frac{5V}{R_2} = \frac{5V}{R_2}$$

R_2 = 250 kΩ (standard value)

When $V_{in} = V_{in\_max}$, the following is true:

$$I_{3\_max} = \frac{V_{in\_max}}{R_1} + \frac{V_{reg}}{R_2}$$

$$100\mu A = \frac{5V}{R_1} + \frac{5V}{250k\Omega}$$

R_1 = 62.5 kΩ ≈ 62 kΩ (standard value)

6. Calculate R_3 / R_4 to set the required current gain. To do this, use this equation along with I_{out_min} and I_{3_min}.

$$4mA = 20\mu A * \left(1 + \frac{R_3}{R_4}\right)$$

$$\frac{R_3}{R_4} = 199$$

Note

Only the minimum values of I_{out} and I_3 are required to calculate R_3 / R_4 because it is assumed that Design Note #5 has been followed.

7. Choose values for R_3 and R_4. Sizing R_3 is much less important than sizing R_4 because headroom issues can arise if care is not taken when sizing R_3. To see why, analyze the nodal voltages under the maximum loading condition, $I_{out} = I_{out\_max}$ = 20 mA. The load voltage is the following:

$V_{load} = I_{out\_max} * R_{load}$ = 20 mA × 250 Ω = 5 V

Most of the output current comes through R_4, so with R_4 = 100 Ω, the voltage at I_{ret} is approximately:

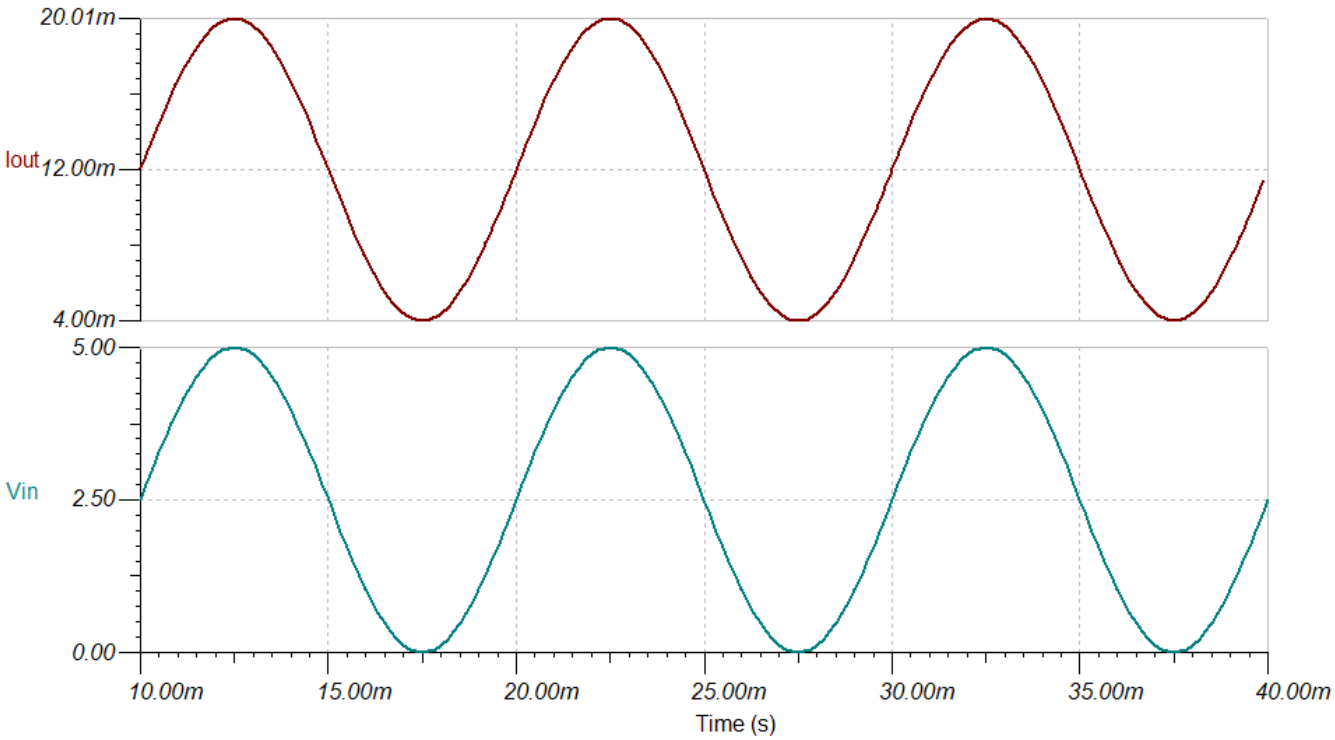
5 V + 100 Ω * 20 mA = 7 V

V_{reg} is referenced to I_{ret}, so relative to the supply ground, V_{reg} = 7 V + 5 V = 12 V, in which case the LDO enters dropout. If the LDO enters dropout, the LDO loses its power supply rejection (PSR) properties, and the op amp has a reduced positive supply and so has a reduced ability to drive the base of the transistor to provide additional output current. Furthermore, if V_{reg} droops, the current through R_3 will be reduced and the circuit begins to exhibit non-linear behavior. Also, if R_6 is too large, the additional voltage drop across R_6 further reduces the available headroom for the transistor.

With these considerations in mind, choose R_4 = 50 Ω to avoid problems with headroom. It follows that:

R_3 = 199 * 50 Ω = 9.95 kΩ ≈ 9.88 kΩ (standard value)

Transient Simulation Results



Design References

1. Texas Instruments, Excel Calculator Tool
2. Texas Instruments, TI Precision Labs - Current Loop Transmitters
3. Texas Instruments, *Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested Reference Design*

Design Featured Op Amp

LMP2012QML-SP	
V_{supply}	
V_{inCM}	–0.3 V to (V_+) +0.3 V
V_{out}	(V_-) + 40 mV to (V_+) – 22 mV
V_{os}	±120 nV
I_q	930 µA per channel
I_b	–3 pA
UGBW	3 MHz
SR	4 V/µs
#Channels	2
Total Ionizing Dose	50 krad(Si)
SEL Immunity to LET	77.5 MeV·cm^2/mg
https://www.ti.com/product/LMP2012QML-SP	

Design Alternate Op Amp

LMP7704-SP	
V_{supply}	±1.35 V to ±6 V
V_{inCM}	(V_-) – 0.2 V to (V_+) + 0.2 V
V_{out}	(V_-) – 120 mV to (V_+) + 120 mV
V_{os}	±32 µV
I_q	725 µA per channel
I_b	±200 fA
UGBW	2.5 MHz
SR	0.9 V/µs
#Channels	4
Total Ionizing Dose	100 krad(Si)
SEL Immunity to LET	85 MeV·cm^2/mg
http://www.ti.com/product/LMP7704-SP	

Design Featured LDO

TPS7A4501-SP	
V_{in}	2.3 V to 20 V
V_{out}	1.21 V to 20 V (adjustable output)
I_{out}	750 mA
V_{do} (dropout voltage)	20 mV
I_q	1.1 mA
#Channels	1
Total Ionizing Dose	150 krad(Si)
SEL Immunity to LET	91.9 MeV·cm^2/mg
https://www.ti.com/product/TPS7A4501-SP	

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