

# ***AN-1990 Compensation for Current Mode Control SEPIC Converters***

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## **ABSTRACT**

This application note discusses the use of SEPIC converters in various applications.

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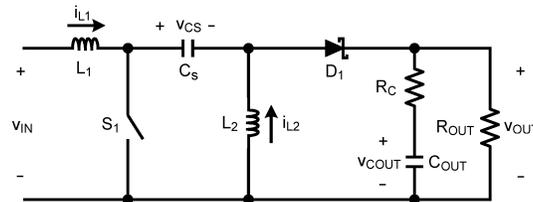
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## 1 Introduction

SEPIC converters have a number of advantages. They allow an input voltage higher or lower than the output voltage. The input voltage and output voltage can be dc isolated by a capacitor. The use of a low side switch makes the switch driver easy to implement. Unlike buck-boost and Cuk converters, the output voltage of SEPIC converters is non-inverting. Hence, SEPIC converters are useful in many applications.

This application note presents the design of compensators for current mode control SEPIC converters. The LM3478 current mode controller will be used. Detailed procedures on designing a lag compensator will be presented in an illustrative example.

## 2 Basic SEPIC Converters



**Figure 1. A SEPIC Converter**

A SEPIC converter is shown in [Figure 1](#). It consists of two inductors ( $L_1$ ,  $L_2$ ) and two capacitors ( $C_S$ ,  $C_{OUT}$ ). Let  $v_{IN}$  and  $v_{OUT}$  be input and output voltages,  $v_{C_{OUT}}$  and  $v_{C_S}$  be voltages across  $C_{OUT}$  and  $C_S$ ,  $i_{L1}$  and  $i_{L2}$  be currents through  $L_1$  and  $L_2$ , and  $R_C$  be the equivalent series resistance (ESR) of  $C_{OUT}$ . Assume that the load is a resistor  $R_{OUT}$ , and that the switch  $S_1$  and the diode  $D_1$  are ideal.

In the continuous conduction mode (CCM), when  $S_1$  is turned on,  $L_1$  and  $L_2$  are charged up by  $v_{IN}$  and  $v_{C_S}$  respectively, while  $C_S$  and  $C_{OUT}$  are discharged by  $i_{L2}$  and the output current respectively. When  $S_1$  is turned off,  $L_1$  and  $L_2$  are discharged, and  $C_S$  and  $C_{OUT}$  are charged up. The open loop small signal model of a SEPIC converter is

$$\tilde{v}_{OUT} = \frac{N_d(s)\bar{d} + N_n(s)\tilde{v}_{IN}}{\Delta(s)}, \quad (1)$$

where

$$N_d(s) = \bar{v}_{IN}R_{OUT}(1 + sR_C C_{OUT})$$

$$\left[ 1 - \frac{s\bar{D}^2 L_1}{(1 - \bar{D})^2 R_{OUT}} + s^2(L_1 + L_2)C_S - \frac{s^3\bar{D}L_1 L_2 C_S}{(1 - \bar{D})^2 R_{OUT}} \right] \quad (2)$$

$$N_n(s) = \bar{D}(1 - \bar{D})R_{OUT}(1 + sR_C C_{OUT}) \left( 1 + \frac{s^2 L_2 C_S}{\bar{D}} \right) \quad (3)$$

$$\Delta(s) = D_0 + D_1 s + D_2 s^2 + D_3 s^3 + D_4 s^4 \quad (4)$$

The coefficients of (4) will be listed in Appendix A. Also,  $N_d(s)$  and  $N_n(s)$  can be expanded to a polynomial as shown in Appendix A. The duty cycle  $d$  is the ratio between the on-time and the switching period  $T_{SW}$  of the switch  $S_1$ . Its nominal value is

$$\bar{D} = \frac{\bar{v}_{OUT}}{\bar{v}_{IN} + \bar{v}_{OUT}}$$

Under current mode control, the current of  $S_1$ , which is the sum of  $i_{L1}$  and  $i_{L2}$ , is fed to the controller during the on period in order to determine the on-time of  $S_1$ . The small signal model of a current mode control SEPIC converter is

$$\tilde{v}_{OUT} = \frac{N_{cc}(s)\tilde{i}_C + N_{cv}(s)\tilde{v}_{IN}}{D_{cc}(s)} \quad (5)$$

where  $i_C$  is the current control signal. It can be converted into a voltage control signal  $v_C$  by a resistor  $R_{SN}$  connecting between  $S_1$  and the ground. Then the relationship between the output voltage and the voltage control signal can be formulated as follows:

$$\tilde{v}_{OUT} = \frac{N_{cc}(s)}{D_{cc}(s)R_{SN}} \tilde{v}_C \quad (6)$$

where

$$D_{cc} = D_{c0} + D_{c1}s + D_{c2}s^2 + D_{c3}s^3 + D_{c4}s^4 + D_{c5}s^5 + D_{c6}s^6, \quad (7)$$

$$N_{cc} = N_{c0} + N_{c1}s + N_{c2}s^2 + N_{c3}s^3 + N_{c4}s^4 + N_{c5}s^5 + N_{c6}s^6, \quad (8)$$

The coefficients of (7) and (8) will be shown in Appendix B.

### 3 Compensator Design

A compensator can be implemented by a transconductance amplifier, with an open loop gain of  $g_m$  and an output impedance of  $R_0$ , connecting to a resistor  $R_{C1}$  and a capacitor  $C_{C1}$  in series to the ground, as shown in Figure 2. Let the negative input of the amplifier is connected to a reference voltage  $V_{REF}$ , and the positive input is connected to the output voltage  $v_{OUT}$  through a resistor divider network implemented by  $R_{F1}$  and  $R_{F2}$ , the transfer function relating  $v_C$  and  $v_{OUT}$  is

$$v_C = \left( \frac{R_{F2}}{R_{F1} + R_{F2}} v_{OUT} - V_{REF} \right) g_m \left[ R_0 \parallel \left( R_{C1} + \frac{1}{C_{C1}s} \right) \right] \quad (9)$$

By adding small signal perturbations, the AC equation can be obtained as follows:

$$\tilde{v}_C = \frac{R_{F2}}{R_{F1} + R_{F2}} g_m R_0 \frac{1 + sR_{C1}C_{C1}}{1 + s(R_{C1} + R_0)C_{C1}} \tilde{v}_{OUT}. \quad (10)$$

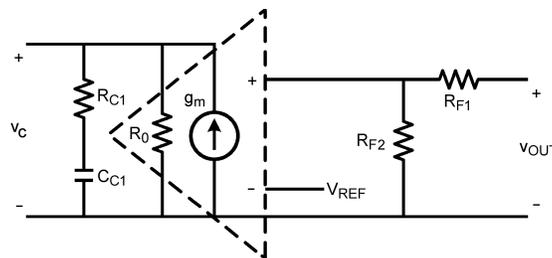


Figure 2. A Compensator Implemented by a Transconductance Amplifier Circuit

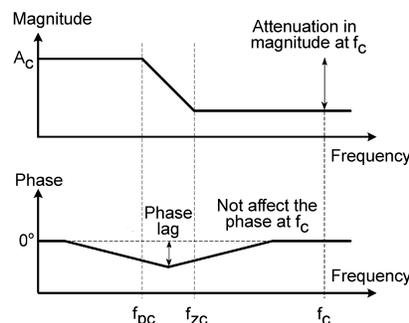


Figure 3. Frequency Response of a Lag Compensator

It can be shown from (10) that the compensator consists of a dc gain of  $A_C$ , and a pole and a zero located at frequencies  $f_{PC}$  and  $f_{ZC}$ . The three parameters can be formulated as

$$A_C = \frac{R_{F2}}{R_{F1} + R_{F2}} g_m R_0,$$

$$f_{PC} = \frac{1}{2\pi(R_{C1} + R_0)C_{C1}},$$

$$f_{ZC} = \frac{1}{2\pi R_{C1}C_{C1}}, \quad (11)$$

Since  $f_{PC}$  is always lower than  $f_{ZC}$ , (10) is a lag compensator. If  $R_{C1}$  is zero, (10) becomes a compensator with a dominant pole. The frequency response of the lag compensator is shown in [Figure 3](#), the lag compensator provides an attenuation in magnitude at the high frequency. The degree of attenuation is determined by the distance between  $f_{PC}$  and  $f_{ZC}$ . It is because the magnitude is decreased at a slope of 20dB/decade between  $f_{PC}$  and  $f_{ZC}$ . The lag compensator also provides a phase lag. However,  $f_{PC}$  and  $f_{ZC}$  can be placed at a low frequency (much lower than the frequency of interest, e.g. the cross over frequency  $f_C$ ) such that the lag compensator nearly does not affect the phase at the high frequency.

The aim of designing a lag compensator is to provide a desired phase margin for the compensated system. Starting from a bode plot of an un-compensated system, and a requirement of phase margin of  $\Phi_m$ , a new  $f_C$  can be selected at the frequency corresponding to  $180^\circ - \Phi_m$  of the un-compensated system. Then the magnitude of the un-compensated system at  $f_C$  can be found. The magnitude at  $f_C$  can be attenuated to 0dB by the lag compensator through proper design of  $f_{PC}$  and  $f_{ZC}$ . As a result, the compensated system will have a phase margin of  $\Phi_m$ , and the cross over frequency will be  $f_C$ .

#### 4 Illustrative Example

The design of a current mode control SEPIC converter with a nominal input voltage of 5V, an output voltage of 5V, and an output current of 0.5A will be shown. It is suitable for applications requiring a 5V output from four batteries, which can be 4.8V to 6V depending on whether 1.2V or 1.5V batteries are used. In this case, the input voltage may be higher or lower than the output voltage, and a SEPIC converter is a proper choice.

The major components of the SEPIC are listed in [Table 1](#). A current mode controller LM3478 will be used. The parameters of the LM3478, which can be derived from the data sheet, are also listed in [Table 2](#).

Other parameters of (6) are calculated below.

From (5),

$$\bar{D} = 0.5$$

Also,

$$T_2 = \frac{T_{SW}}{2} = \frac{1}{2f_{SW}} \tag{12}$$

$$T_2 = 1.25 \mu s \tag{13}$$

The parameter  $m_C$  is determined by an internal compensation ramp  $V_{SL}$  and an external compensation ramp determined by an internal current of 40  $\mu A$  passing through an external resistor  $R_{SL}$ . It can be calculated by the following equation:

$$m_C = (V_{SL} + 40 \mu A \times R_{SL})f_{SW}/R_{SN} = 3440000As^{-1} \tag{14}$$

$$T_M = \frac{T_{SW}}{2} \left( 2m_C + \frac{\bar{V}_{IN}}{L_1} + \frac{\bar{V}_{IN}}{L_2} \right) = 8.979A \tag{15}$$

**Table 1. Major Parameters of the Example SEPIC Converter**

Parameter	Value
$\bar{V}_{IN}$	5V
$\bar{V}_{OUT}$	5V
$R_{OUT}$	10 $\Omega$
$L_1$	33 $\mu H$
$L_2$	33 $\mu H$
$C_S$	1 $\mu F$
$C_{OUT}$	100 $\mu F$
$R_{COUT}$	0.05 $\Omega$
$f_{SW}$	400 kHz
$R_{SN}$	0.02 $\Omega$
$R_{SL}$	2 k $\Omega$

**Table 2. Parameters of the LM3478**

Parameter	Value
$V_{REF}$	1.26V
$g_m$	$800 \mu\Omega^{-1}$
$R_0$	$A_v/g_m = 38/800 \mu\Omega^{-1} = 47.5 \text{ k}\Omega$
$V_{SL}$	92 mV

Hence, all parameters for calculating the small signal model of (6) are obtained. A bode plot of (6) with the above parameters is shown in Figure 4.

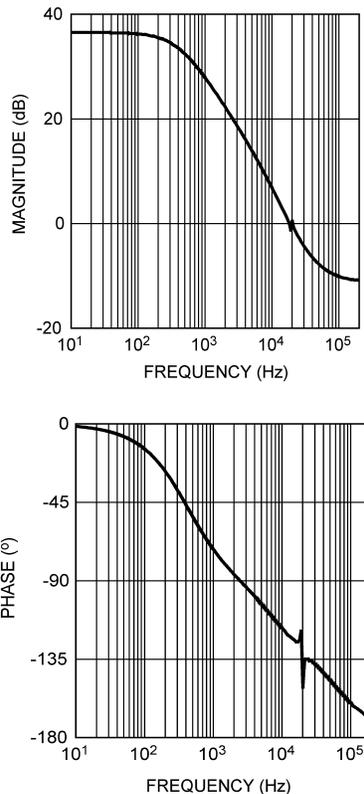
Since  $\bar{V}_{OUT}$  and  $V_{REF}$  are 5V and 1.26V respectively, we can design that

$$R_{F1} = 29.7 \text{ k}\Omega \tag{16}$$

$$R_{F2} = 10 \text{ k}\Omega \tag{17}$$

From (10),

$$\begin{aligned} A_C &= \frac{R_{F2}}{R_{F1} + R_{F2}} g_m R_0 \\ &= 9.57 \\ &= 19.62 \text{ dB} \end{aligned} \tag{18}$$



**Figure 4. Frequency Response of the Un-Compensated System**

In this example, a phase margin of  $90^\circ$  is desired. From Figure 4, the corresponding frequency (the frequency at which the phase is  $180^\circ - 90^\circ = 90^\circ$ ) is 2.1 kHz (which will also be  $f_C$  of the compensated system), and the magnitude of the un-compensated system at 2.1 kHz is 21dB. This implies that the attenuation provided by the lag compensator is  $21\text{dB} + A_C = 40.62 \text{ dB}$ . Consequently, the distance between  $f_{PC}$  and  $f_{ZC}$  should be 2.031 decade (since the magnitude is 20dB/decade in between  $f_{PC}$  and  $f_{ZC}$ ). To avoid affecting the phase at  $f_C$ ,  $f_{ZC}$  is designed to be one decade before  $f_C$ , i.e. 210 Hz. Then  $f_{PC}$  should be 1.95 Hz. Hence,

$$1/R_{C1}C_{C1} = 2\pi \times 210 \text{ Hz} \tag{19}$$

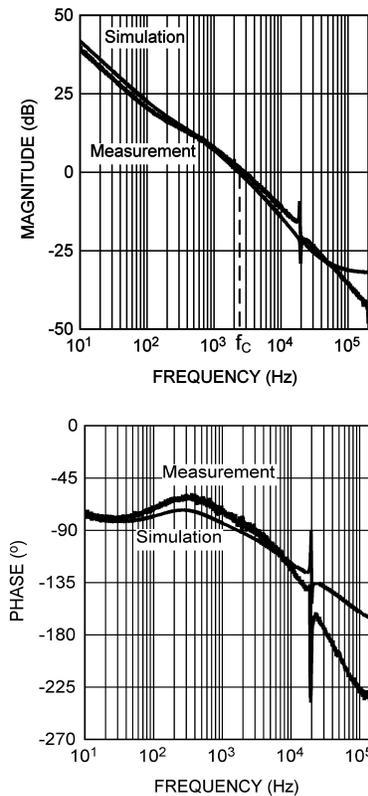
$$\frac{1}{(R_{C1} + R_0)C_{C1}} = 2\pi \times 1.95 \text{ Hz}$$

$$R_0C_{C1} = \frac{1}{2\pi \times 1.95 \text{ Hz}} - R_1C_{C1}$$

$$C_{C1} = 1.7 \mu\text{F}$$

$$R_{C1} = 445\Omega \tag{20}$$

Finally, select  $R_{C1} = 442\Omega$  and  $C_{C1} = 2.2 \mu\text{F}$ . The frequency response of the compensated system is shown in Figure 5. It can be found that the 0dB point is at around 2.5 kHz, and the phase margin is around  $90^\circ$ .



**Figure 5. Frequency Response of the Compensated System with  $90^\circ$  Phase Margin**

## 5 Conclusion

This application note details the design of a lag compensator for current mode control SEPIC converters operating in the continuous conduction mode. Based on the open loop bode plot, a lag compensator with  $90^\circ$  phase margin has been designed as an illustrative example. The design of compensator depends on a number of practical concerns including the requirement of transient response, robustness, and the effect of noise. Application engineers are suggested to design properly based on practical situations.

## 6 Appendix A

The coefficients of (4) are listed as follows.

$$\Delta(s) = D_0 + D_1s + D_2s^2 + D_3s^3 + D_4s^4, \quad (21)$$

$$D_0 = R_{OUT}(1-\bar{D})^2,$$

$$D_1 = L_M + (1-\bar{D})^2 R_C R_{OUT} C_{OUT},$$

$$D_2 = L_M(R_C + R_{OUT})C_{OUT} + (1-\bar{D})^2(L_1 + L_2)R_{OUT}C_S,$$

$$D_3 = L_1L_2C_S + (1-\bar{D})^2(L_1 + L_2)R_C R_{OUT}C_S C_{OUT},$$

$$D_4 = L_1L_2(R_C + R_{OUT})C_S C_{OUT},$$

$$L_M = \bar{D}^2L_1 + (1-\bar{D})^2L_2. \quad (22)$$

From (2),  $N_d(s)$  can be expanded as follows.

$$N_d(s) = N_0 + N_1s + N_2s^2 + N_3s^3 + N_4s^4, \quad (23)$$

$$N_0 = \bar{V}_{IN}R_{OUT},$$

$$N_1 = \bar{V}_{IN}R_C R_{OUT} C_{OUT} - \frac{\bar{D}^2}{(1-\bar{D})^2} \bar{V}_{IN}L_1,$$

$$N_2 = \bar{V}_{IN}(L_1 + L_2)R_{OUT}C_S - \frac{\bar{D}^2}{(1-\bar{D})^2} \bar{V}_{IN}L_1R_C C_{OUT},$$

$$N_3 = \bar{V}_{IN}(L_1 + L_2)R_C R_{OUT}C_S C_{OUT} - \frac{\bar{D}}{(1-\bar{D})^2} \bar{V}_{IN}L_1L_2C_S,$$

$$N_4 = -\frac{\bar{D}}{(1-\bar{D})^2} \bar{V}_{IN}L_1L_2R_C C_S C_{OUT}. \quad (24)$$

From (3),  $N_n(s)$  can be expanded as follows.

$$N_n(s) = N_{n0} + N_{n1}s + N_{n2}s^2 + N_{n3}s^3,$$

$$N_{n0} = \bar{D}(1-\bar{D})R_{OUT},$$

$$N_{n1} = \bar{D}(1-\bar{D})R_C R_{OUT} C_{OUT},$$

$$N_{n2} = (1-\bar{D})L_2R_{OUT}C_S,$$

$$N_{n3} = (1-\bar{D})L_2R_C R_{OUT}C_S C_{OUT}. \quad (25)$$

## 7 Appendix B

The coefficients of (7) are listed as follows.

$$D_{cc} = D_{c0}s + D_{c1}s + D_{c2}s^2 + D_{c3}s^3 + D_{c4}s^4 + D_{c5}s^5 + D_{c6}s^6, \quad (26)$$

$$D_{c0} = C_{d0}D_1 + C_{d1}D_0 - C_{v0}N_1 - C_{v1}N_0,$$

$$D_{c1} = C_{d0}D_2 + C_{d1}D_1 + C_{d2}D_0 - C_{v0}N_2 - C_{v1}N_1 - C_{v2}N_0$$

$$D_{c2} = C_{d0}D_3 + C_{d1}D_2 + C_{d2}D_1 - C_{d3}D_0 - C_{v0}N_3 - C_{v1}N_2 - C_{v2}N_1$$

$$D_{c3} = C_{d0}D_4 + C_{d1}D_3 + C_{d2}D_2 - C_{d3}D_1 - C_{v0}N_4 - C_{v1}N_3 - C_{v2}N_2$$

$$D_{c4} = C_{d1}D_4 + C_{d2}D_3 + C_{d3}D_2 - C_{v1}N_4 - C_{v2}N_3$$

$$D_{c5} = C_{d2}D_4 + C_{d3}D_3 - C_{v2}N_4$$

$$D_{c6} = C_{d3}D_4$$

$$C_{d0} = \frac{\bar{V}_{IN}L_1L_2}{(1 - \bar{D})},$$

$$C_{d1} = L_1L_2L_M T_M + \frac{\bar{D}}{(1 - \bar{D})} [(1 - D)L_2 - \bar{D}L_1] \bar{V}_{IN}L_1 \left[ T_2 + \frac{L_2}{R_{OUT}(1 - \bar{D})} \right],$$

$$C_{d2} = \frac{\bar{V}_{IN}L_1L_2}{(1 - \bar{D})} \left[ (L_1 + L_2)C_S - L_1T_2 \frac{\bar{D}^2}{R_{OUT}(1 - \bar{D})} \right],$$

$$C_{d3} = L_1^2L_2^2C_S T_M$$

$$C_{v0} = (1 - \bar{D})L_1L_2,$$

$$C_{v1} = \bar{D}L_1(L_M - \bar{D}L_1)T_2,$$

$$C_{v2} = (1 - \bar{D})L_1L_2(L_1 + L_2)C_S,$$

$$T_2 = \frac{T_{SW}}{2}, \quad T_{SW} \text{ is the switching period,}$$

$$T_M = \frac{T_{SW}}{2} \left( 2m_c + \frac{\bar{V}_{IN}}{L_1} + \frac{\bar{V}_{IN}}{L_2} \right), \quad -m_c \text{ is the slope of a compensation ramp,} \quad (27)$$

The coefficients of (8) are listed as follows.

$$N_{cc} = N_{c0} + N_{c1}s + N_{c2}s^2 + N_{c3}s^3 + N_{c4}s^4 + N_{c5}s^5 + N_{c6}s^6, \quad (28)$$

$$N_{c0} = C_{c0}N_0,$$

$$N_{c1} = C_{c0}N_1,$$

$$N_{c2} = C_{c0}N_2 + C_{c2}N_0,$$

$$N_{c3} = C_{c0}N_3 + C_{c2}N_1,$$

$$N_{c4} = C_{c0}N_4 + C_{c2}N_2,$$

$$N_{c5} = C_{c2}N_3,$$

$$N_{c6} = C_{c2}N_4,$$

where

$$C_{c0} = L_1L_2L_M,$$

$$C_{c2} = L_1^2L_2^2C_S.$$

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