ABSTRACT
Sensing the inductor DCR voltage can be an accurate and lossless technique of obtaining current
information in DC/DC regulators. The absence of a series current sense resistor permits high current and
high efficiency designs at a lower cost and higher density. Inductor DCR sensing also allows continuous
monitoring of the inductor current as opposed to MOSFET $R_{DS(ON)}$ sensing that usually samples the voltage
information across a FET during a small interval of time. Unlike MOSFETs, inductors can be purchased
with low tolerance DCR specifications thus increasing the overall current sense accuracy.

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1 Introduction

The LM27402 is equipped with a low offset current sense comparator to handle inductor DCR current sense applications. A +10 µA current in series with a resistor provides a voltage offset compared to the DCR voltage to set the current limit level. This application report walks through the process of choosing the DCR current sense circuit components to optimize the current limit performance of the LM27402 DC/DC buck regulator controller.

2 DCR Current Sense Topology

Figure 1 shows a typical topology for sensing the DCR voltage in a buck regulator.

![Figure 1. DCR Current Sense Topology](image)

Components $R_S$ and $C_S$ create an RC filter. The time constant of the RC filter should match the time constant related to the inductor and its DCR to accurately reproduce the DCR voltage across $C_S$. Given the following circuit:

![Figure 2. DCR Sense Equivalent Circuit](image)

The derivation for matching time constants is as follows:

$$V_{DCR}(s) = V_L \frac{R_{DCR}}{sL + R_{DCR}} = V_L \frac{1}{C_S} \frac{1}{R_S + 1}$$

$$\frac{1}{sL + R_{DCR}} = \frac{1}{R_S C_S + 1}$$

$$R_S C_S + 1 = \frac{sL}{R_{DCR}} + 1$$

$$R_S C_S = \frac{L}{R_{DCR}}$$

$$T_{RC} = T_L$$

(1)

If the time constants do not match, the voltage $V_S$ will either lead or lag $V_{DCR}$. Particularly:

If $T_{RC} > T_L$, $V_S$ will lag $V_{DCR}$ by a factor of $T_{RC}/T_L$ at any point in time $<< T_{RC}$.

If $T_{RC} < T_L$, $V_S$ will lead $V_{DCR}$ by factor of $T_{RC}/T_L$ at any point in time $<< T_{RC}$.
Time constant mismatching can be useful in some situations where tight or loose limiting of current limit must be applied. For example, if a buck regulator responds readily to fast $dI/dt$ load transients, the inductor current must supply the output current in addition to the output capacitor current. This can cause the inductor current to temporarily overshoot, thereby, exceeding the current limit setpoint. The $V_S$ signal can filter this event if $\tau_{RC}$ is designed moderately larger than $\tau_L$ in anticipation of inductor overshoot. However, time constant mismatching must be used carefully. If $\tau_{RC}$ is much greater than $\tau_L$, the inductor current may reach dangerous levels before the current limit condition is detected.

3 LM27402 DCR Current Sense Design

The LM27402 is designed to detect the voltage across the DCR of an inductor through the use of a sensitive current limit comparator. Five current limit events within 32 switching cycles must occur to mitigate the effects of noise and transitory over current events before hiccup mode activates. This allows the current limit level to be set close to the peak inductor ripple current during maximum output current where the voltage across the comparator may only be several millivolts. Figure 3 shows the typical circuit used to set the current limit level:

![Figure 3. LM27402 Typical Current Limit Circuit](image)

A $+10 \mu A$ current source, $I_{CS-}$, is internally connected from the VIN pin to the CS- pin to set the comparator offset voltage, $V_{SET}$, across $R_{SET}$. During operation, $V_{SET}$ is compared to the voltage $V_S$, across $C_S$. The equation for $R_{SET}$ to set the current limit set point is shown in Equation 2:

$$R_{SET} = \frac{I_{LIMIT}R_{DCR}}{I_{CS-}}$$

(2)

$I_{LIMIT}$ (A) is the desired current limit level, $R_{DCR}$ (Ω) is the rated DC resistance of the inductor (DCR), and $I_{CS-}$ (A) is the $+10 \mu A$ current source flowing out of the CS- pin. $I_{LIMIT}$ should be set sufficiently higher than the peak inductor current at maximum output current to minimize false current limit signals. Components $R_S$ and $C_S$ should be chosen to match the inductor $L/R_{DCR}$ time constant. A typical range of capacitance used in the $R_S\,C_S$ network is 100 nF to 1 µF. After choosing a $C_S$ capacitor, $R_S$ can be calculated by:

$$R_S = \frac{L}{R_{DCR}\,C_S}$$

(3)

Capacitor $C_{SBY}$ is used to filter any noise that may exist across the CS+ and CS- pins. A working range for the $C_{SBY}$ capacitance is 47 pF to 100 pF. A second resistor can be placed between CS+ and the $R_S\,C_S$ network to match the impedance into the inputs of the current sense comparator for extra noise rejection shown here as $R_{CS+}$:

![Figure 4. Added Resistor for Noise Rejection](image)
The value of $R_{CS+}$ should be equal to $R_{SET}$.

4 **CS- Current Source Compliance Voltage**

The CS- current source requires at least 1.0V of headroom to ensure a current of $+10 \mu A$. If the voltage across the current source ($V_{IN} - V_{CS-}$) decreases below 1.0V, the current will decrease as with the voltage across $R_{SET}$ effectively lowering the current limit setpoint. If $V_{IN} - V_{OUT}$ is less than 1.0V, the current source will lose compliance because $V_{CS}$ closely follows $V_{OUT}$. This can be avoided by enabling the LM27402 at an input voltage 1V higher than $V_{OUT}$ or by lowering the common mode voltage of the current limit comparator with a resistor divider network shown in Figure 5.

![Figure 5. Resistor Divider Network](image)

The voltage divider network in Figure 5 reduces the common mode voltage of the comparator and will effectively sense the inductor current. $R_{SET}$ is calculated in the same way as discussed previously. $R_{S3}$ should be sized to avoid a condition where $V_{IN} - V_{CS}$ is less than 1.0V. $R_{S1}$, $R_{S2}$ and $R_{S3}$ should be sized to match the ratio set by $R_{SET}$ and $R_{S3}$.

5 **Example Application**

In this example, the application is as follows:

$V_{IN} = 3.3V$, $V_{OUT} = 2.5V$, $I_{OUT} = 20A$, $I_{LIMIT} = 25.7A$, $L = 0.6 \mu H$, $R_{DCR} = 1.89 \Omega$, $f_{SW} = 300 kHz$. An $I_{LIMIT}$ of 25.7A will produce a maximum DC output current of 24.5A at 25°C.

The value of $R_{SET}$ should be:

$$R_{SET} = \frac{(25.7A)(1.89 \Omega)}{10\mu A} = 4.87 \Omega$$

(4)

The lowest input voltage for this application ($V_{INMIN}$) is 2.7V. $R_{S3}$ should be sized to force $V_{CS}$ to be less than 1.7V when $V_{IN} = 2.7V$ to maintain at least 1V of headroom. The equation solving for $R_{S3}$ is shown in Equation 5:

$$R_{S3} = R_{SET} \frac{V_{CS}}{V_{INMIN} - V_{CS}}$$

(5)

Substituting $V_{INMIN} - V_{CS} = 1V$ and $V_{CS} = V_{INMIN} - 1V$ results in:

$$R_{S3} = R_{SET}(V_{INMIN} - 1) = 4.87 \Omega(2.7 - 1) = 8.25 \Omega$$

(6)

Resistors $R_{S1}$, $R_{S2}$, and $R_{S3}$ must be designed to maintain the following ratio:

$$\frac{R_{SET}}{R_{S3}} = \frac{R_{S1} + R_{S2}}{R_{S2}}$$

(7)

It is recommended to design the CS+ branch of resistors to be higher impedance than the CS- branch of resistors to yield a $C_S$ value in the nf range. In this example, the CS+ branch impedance will be set eight times larger than the CS- impedance. $R_{S2}$ is calculated as follows:

$$R_{S2} = 8R_{S3} = 66.5 \Omega$$

(8)
Unfortunately, the ratio of $R_{S1}/R_{S3}$ is not equal to $R_{SET}/R_{S3}$ thus allowing transient differential signals to feed through the $C_S$ capacitor causing an error voltage between the CS+ and CS- pins. $R_S$ and $R_{S1}$ should be sized appropriately to minimize this error. Specifically, $R_S$ should be sized 5% of $8R_{SET}$ and $R_{S1}$ should be sized 95% of $8R_{SET}$ as shown here:

$$R_S = (0.05)(8)R_{SET} \approx 1.96 \, \text{k\Omega}$$

$$R_{S1} = (0.95)(8)R_{SET} \approx 37.4 \, \text{k\Omega}$$

(9)

$C_S$ is calculated using the parallel combination of $R_S||(R_{S1}+R_{S2})$ to match the inductor time constant shown here:

$$C_S = \frac{L}{R_{DCR}(R_S||(R_{S1}+R_{S2}))}$$

$$= 165 \, \text{nF}$$

(10)

6 Layout

The circuitry to sense the DCR voltage is sensitive to noise and demands careful layout practices. Following these general guidelines will help ensure a robust design.

7 CSBY Placement

The CSBY capacitor should be placed as close to the CS+ and CS- pins as possible. CSBY serves as the last line of defense between board noise and the current limit comparator. CSBY should be a small 0603 or 0402 surface mount capacitor to facilitate close placement to the LM27402.

8 CS+ and CS- Traces

Certain applications will call for long CS+ and CS- traces. For example, the LM27402 evaluation board incorporates a temperature compensated current limit circuit with a PTC resistor in series with CS-. This requires the CS- trace to be routed from the LM27402 to the inductor. It is essential to route the CS+ and CS- traces away from noise emitting nodes, particularly the switch-node and gate drives nodes on the PCB. Routing the CS+ and CS- traces side by side for close coupling and in between ground planes is a sufficient way to mitigate differential noise.
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