

LM25037,LM5020,LM5037,LM5112

An Alternative Approach to Higher-Power Boost Converters



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An Alternative Approach to Higher-Power Boost Converters

— By David Baba, Product Applications Engineer

A higher-power boost converter often requires special consideration to minimize power losses and temperature rise in the FETs, diode, and inductor. Regarding FETs, many designers opt to place FETs in parallel to reduce conduction losses. However, placing FETs in parallel can increase transitional losses. This article discusses a number of approaches that can be considered to reduce total losses in boost FETs. Possible options include selecting lower gate-charge FETs, selecting alternative controllers with higher gate-drive current, or using a gate driver such as the LM5112. An alternative approach using National Semiconductor's PowerWise[®] LM25037 dual-output gate-drive controller and its benefits are considered as compared to using a single gate-drive controller such as the LM5020. Further, this article will examine ways to approximate total FET losses and then make a selection from the potential approaches that best suits the application requirement.

General Overview of a Boost Converter

Figure 1 shows: a boost converter with its basic components, (a); the operation of the boost converter during the on period D , (b); and the operation during the off period $(1-D)$, (c).

All three waveforms in Figure 2 illustrate behavior over one complete switching cycle. In (a), the inductor current can be seen; in (b), the switch current is depicted; and in (c), the voltage across the FET is illustrated.

The boost converter supplies a voltage that is always greater than its source voltage. The volt-second balance of the inductor L , for the D period, is added to the input voltage during the $(1-D)$ period and is rectified to the

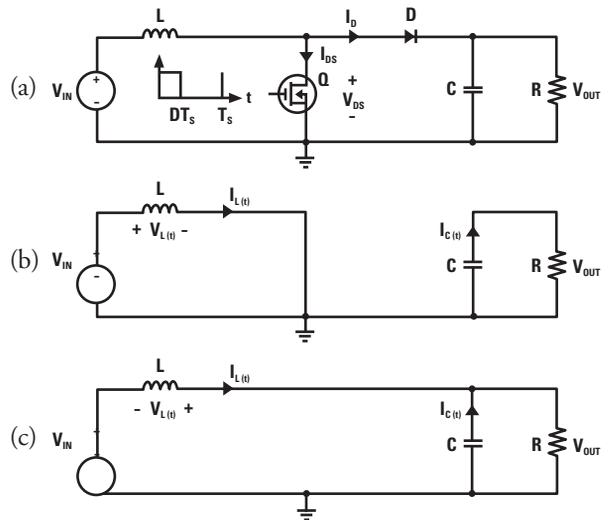


Figure 1. The Boost Converter during the D and $(1-D)$ Switching Period

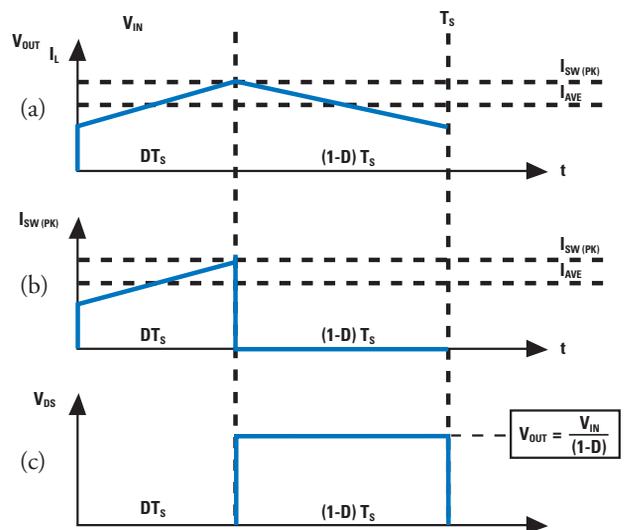


Figure 2. Basic Behavioral Waveforms of the Boost Converter

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output through the diode. The longer the D period, the shorter the 1-D period becomes, thereby increasing the voltage during the off time in order to maintain volt-second balance.

A benefit to the alternative approach using the LM25037 PWM controller is evident in applications where the output voltage is many times greater than the input. The relationship of input and output voltage as it relates to the duty ratio is highlighted in the following equation:

$$\text{EQ1} \quad \frac{V_{OUT}}{V_{IN}} = \frac{1}{(1-D)}$$

From *Equation 1*, it is apparent that a single-channel gate-drive solution with a limited maximum duty ratio can inhibit large step-up ratios. Some controllers have a maximum period of 80% which will limit the step-up ratio to five times the input. However, using the LM25037 controller presents no such limitations. The reason for this is that the alternating outputs of the LM25037 gate driver have only a small dead time between the two outputs which allows a maximum duty ratio beyond 80%. And therefore, it is possible to obtain output voltages that are 10 times the input.

Losses in the Boost FET

Losses due to the boost FET can be separated into three different categories, namely, conduction, transition, and switching losses. Conduction and transition losses are discussed as they are dissipated directly in the FET which impacts thermal performance.

Conduction Losses

Conduction losses in the boost FET are directly related to the output power of the boost converter, the input voltage, the output voltage (relating to D), and the $R_{DS_{ON}}$ of the FET.

Conduction loss is an I^2R term where I is the RMS switch current and R is the $R_{DS_{ON}}$ of the FET. For a boost converter, the conduction losses are shown in the following equations.

$$\text{EQ2} \quad SW_{COND} = I_{SW_{RMS}}^2 \times R_{DS_{ON}}$$

Where

$$\text{EQ3} \quad I_{SW_{RMS}} = \sqrt{\frac{D}{3} \times (I_{PEAK}^2 + I_{PEAK} \times I_{TROUGH} + I_{TROUGH}^2)}$$

$$\text{EQ4} \quad I_{PEAK} = 1.25 \times I_{IN_{AVE}}$$

$$\text{EQ5} \quad I_{TROUGH} = 0.75 \times I_{IN_{AVE}}$$

$$\text{EQ6} \quad I_{IN_{AVE}} = \frac{I_{OUT}}{(1-D)}$$

$$\text{EQ7} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Note: *Equations 3 and 4* relate to the peak-to-peak inductor current which is 50% of the average input current.

Transitional Losses

Transitional losses occur during the time period when the FET is turning on or off. During steady-state operation before the FET turns on, the output voltage is across the drain and the source of the FET. As the FET begins to turn on, current begins flowing from the drain to the source after which the voltage begins to fall. During this time, the current is increasing as the voltage remains across the FET and losses are incurred. During turn off, the exact reverse occurs.

As the frequency increases, transitional losses increase as more transitions occur per second.

Also, if transition times increase, transitional losses increase because the FET endures a longer period of time within the described loss period. Transitional losses can be approximated by the following equations:

$$\text{EQ8} \quad Trans_{LOSSES} = 2 \times V_{OUT} \times I_{IN,AVE} \times T_{TRANS} \times F_{SW}$$

Where

$$\text{EQ9} \quad V_{OUT} = \frac{V_{IN}}{(1 - D)}$$

$$\text{EQ10} \quad I_{IN,AVE} = \frac{I_{OUT}}{(1 - D)}$$

F_{SW} is the switching frequency and T_{TRANS} is the transitional switching time.

Figure 3 depicts a graph showing the drain current and the voltage across the FET and illustrates how much charge is required to fully turn on the FET.

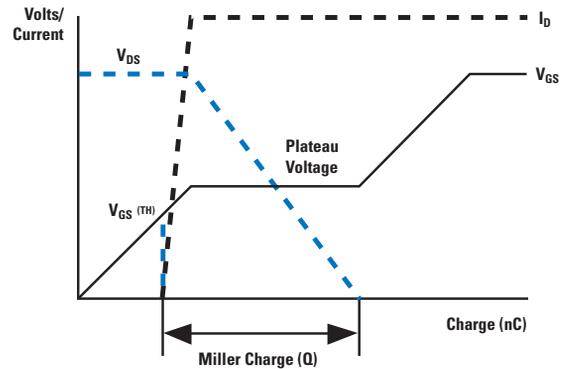


Figure 3. Approximating Transitional Switching Time

The charge relates to time and is proportional to the gate-drive current being supplied to the gate of the FET. The more available current, the quicker the FET will turn on. Conversely, turning off the FET requires that the gate driver sinks current out of the gate, and thus, the more current the gate driver can sink, and the faster the FET will turn off. For the purpose of simplicity, it is assumed the turn-on time is equal to the turn-off time, with the gate driver providing the same source and sink-current capability.

Many FET datasheets include a graph that relates the V_{GS} on the Y axis with the charge on the X axis. *Figure 3* has additional V_{DS} and I_D curves for relating the topic being discussed. To estimate the charge required to fully switch on a FET, the designer must estimate the differential charge, shown as the Miller charge. Another approximation can be made by estimating the Miller charge to be approximately 60% of the typical gate charge.

The gate drive resistance for MOSFET gate drivers is typically quoted in its datasheet. For the Bipolar Junction Transistor (BJT) output stage, it will not be quoted as a resistance. V_{SAT} is quoted for a BJT

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output-driver stage. However, the V_{SAT} information provided can be used to approximate the drive resistance as is seen in the following equation. The V_{G_DROF} is the V_{SAT} of the transistor output stage.

$$EQ11 \quad \frac{V_{G_DROF}}{Gate_{CURRENT}} = Drive_R$$

The voltage available to drive a FET needs to be determined. This is simply calculated by subtracting the Miller plateau voltage from the total output voltage at the gate drive. The voltage available to drive the FET after its threshold is met is:

$$EQ12 \quad V_{G_AVAIL} = V_{GATE} - V_{GS}(MP)$$

Equation 11 calculates the resistance of the gate driver. From this calculation, the gate-drive current is therefore:

$$EQ13 \quad I_{GATE} = \frac{V_{G_AVAIL}}{Drive_R + R_G}$$

where, R_G is the gate resistance of the FET.

Once the gate-drive current is determined, the transitional time can be calculated:

$$EQ14 \quad T_{TRANS} = \frac{Charge_{Miller}}{I_{GATE}}$$

And the evaluation of transition losses (Equation 8) is now possible.

By way of example, a boost specification will be considered using the two-switch approach and compared to the single gate-drive, parallel-switch approach.

$$V_{IN} = 12V$$

$$V_{OUT} = 24V$$

$$I_{OUT} = 6A$$

$$F_{sw} = 300\text{ kHz}$$

$$L = 3.6\ \mu H$$

Single Gate-Drive Parallel-FET Approach using the LM5020 Controller

Considering the previously-identified specification, the designer may opt to use National's LM5020 PWM controller. The LM5020 controller is a common selection for many boost applications and serves as a good comparison in a typical design scenario.

Placing two FETs in parallel will increase switching losses as the gate charge will double and therefore switching transition times will double. With high RMS switch currents and the doubling of gate charge, it is essential to select FETs that have a low R_{DS_ON} and a low gate charge. These types of FETs tend to be more costly than FETs that have similar R_{DS_ON} with a higher gate charge. To address this transitional loss issue, the FET selected for this example is the SiR472DP FET from Vishay.

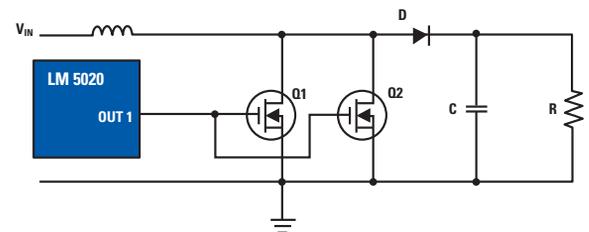


Figure 4. A Single Gate-Drive Controller Switching Two FETs in Parallel

A traditional method of using a single gate-drive controller switching two FETs in parallel is shown in *Figure 4*.

From the calculation in *Equation 7*,

$$D = 0.5$$

and from *Equation 6*, the average input current is calculated as:

$$I_{IN_{AVE}} = 12A$$

Choosing 50% of the average input current as being the peak-to-peak current in the inductor and using *Equations 4 and 5*, this yields the following peak and trough values:

$$I_{PEAK} = 15A$$

$$I_{TROUGH} = 9A$$

Using *Equation 3*, the switch RMS currents can be calculated:

$$I_{SWITCH_{RMS}} = 8.57A$$

And the conduction losses also can now be calculated. The $R_{DS_{ON}}$ for the SiR472DP is 0.012Ω at 10V of gate-drive voltage. As two of these FETs are placed in parallel, the effective $R_{DS_{ON}}$, is half of this value (0.006Ω).

$$SW_{COND} = 0.441W$$

In order to evaluate *Equation 8*, the transitional switching time must be estimated. It is assumed the $V_{GS(th)}$ of the SiR472DP is 1.85V (typical) from the

datasheet. By referencing the SiR472DP datasheet and using the V_{GS} versus total gate charge (nC) in a graph similar to the one shown in *Figure 3*, the Miller charge is shown to be 4 nC for a V_{DS} of 24V. The effective Miller charge doubles (8 nC) due to two FETs being placed in parallel.

The LM5020 datasheet does not provide gate-drive resistance data as it has a BJT output stage, but the source resistance of the gate drive can still be estimated. The table on page 5 of the LM5020 datasheet shows the voltage drop (0.25V) of the gate-drive output for a given sourcing current (0.05A). By dividing the current flowing out of the gate drive into the voltage drop, the gate resistance can be estimated. Using *Equation 11* yields:

$$Drive_R = 5\Omega$$

The LM5020 controller has an output gate-drive voltage of 7.6V supplied by the V_{CC} regulator; from *Equation 12*:

$$V_{G_{AVAIL}} = 4.6V$$

A gate resistance of 1.8Ω (typical) is specified in the SiR472DP datasheet. Using *Equation 13*, the gate-drive current can be calculated:

$$I_{GATE} = 0.68A$$

Using *Equation 14*, the transitional time yields:

$$T_{TRANS} = 11.76 ns$$

Using *Equation 8*, the transitional losses can be approximated to:

$$Trans_{LOSSES} = 2W$$

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By adding the conduction losses with transitional losses, the total FET losses are obtained. Total FET losses using the single gate-drive parallel-FET method is:

$$FET_{LOSS\ TOTAL} = 2.47W$$

Half of the calculated power (1.24W) is dissipated in each FET.

There are alternative approaches in circumstances where the single gate-drive approach is causing the FET to dissipate too much power. For example, a single gate-drive controller with higher drive current (if one is available) can be employed or an additional IC using the gate driver (LM5112) can be used. Another alternative is to consider the dual gate-driver approach.

Dual-Output Gate-Driver Approach using the LM25037 Controller

A basic schematic of the LM25037 dual gate driver switching the gates of two FETs independently is shown in *Figure 5*.

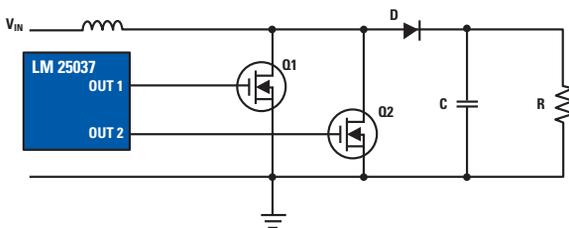


Figure 5. LM25037 Dual-Output Gate Drivers Switching Two FETs Independently

Switching two independent FETs from a dual gate-drive controller typically allows the designer to select low $R_{DS\ ON}$ FETs with a higher gate charge. Higher gate-charge FETs tend to be less expensive than their lower gate-charge counterparts.

The two FETs selected to be switched independently are the SiR468DP. As previously mentioned, driving two FETs in parallel produces a 50% reduction in

$R_{DS\ ON}$. Switching FETs independently, however, no longer yields the 50% reduction in $R_{DS\ ON}$ but transitional losses are reduced.

The $R_{DS\ ON}$ of the SiR468DP is 0.0057Ω . The duty ratio (D) for each FET is now reduced to 25% due to the independent switching of the FETs. Using *Equation 2* and using the revised effective D, we yield:

$$I_{SWITCH\ RMS} = 6.06A$$

$$SW_{COND} = 0.209W$$

There are two FETs dissipating the above conduction losses. The total conduction losses are twice this amount, therefore the total conduction losses in both FETs are:

$$SW_{COND\ TOTAL} = 0.42W$$

Each gate drive of the LM25037 controller has the same gate-current drive capability as the LM5020 controller. The datasheet specifications can be referred to for more details.

A gate resistance of 1.1Ω (typical) is specified in the SiR468DP datasheet. Using *Equation 13*, the gate-drive current can be calculated as:

$$I_{GATE} = 0.75A$$

It is assumed the $V_{GS(th)}$ of the SiR468DP is 2V (typical) from the datasheet. From the SiR468DP datasheet, using the V_{GS} versus total gate charge similar to the graph shown in *Figure 3*, the Miller charge is shown to be 6 nC for a V_{DS} of 22.5V. Using a dual gate-drive controller switching independent FETs reduces the transitional losses due to the halving of the effective Miller charge which decreases the transitional switching times. Transitional switching time is calculated using *Equation 14*:

$$T_{TRANS} = 7.96\ ns$$

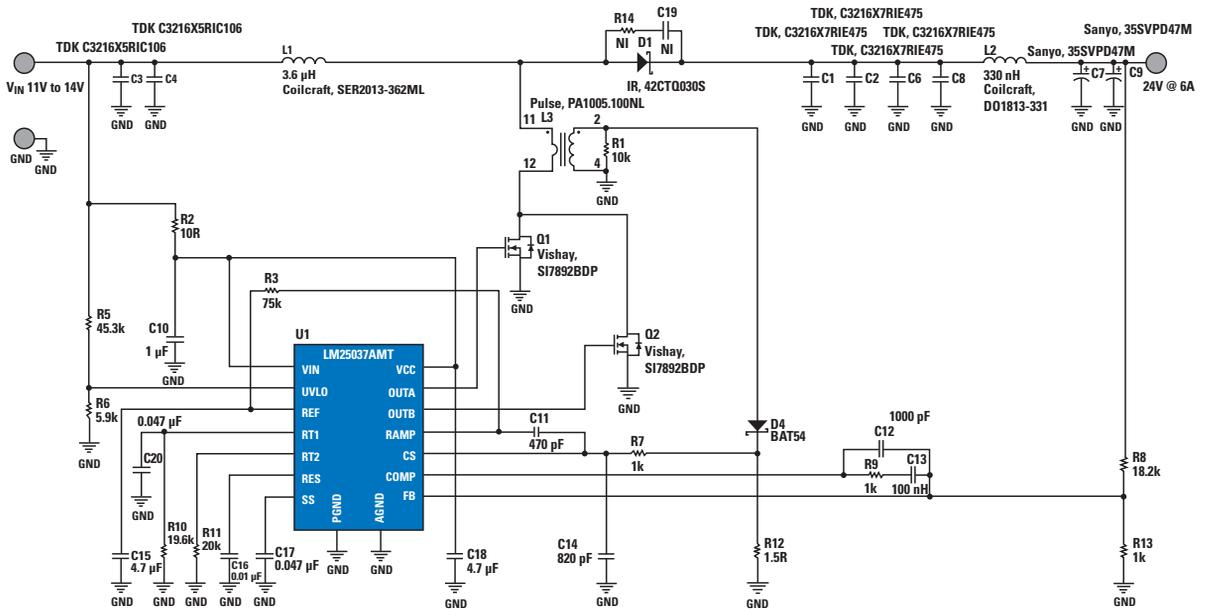


Figure 6. Application Example of a 12V IN, 24V OUT at 6A

From Equation 8:

$$Trans_{LOSSES} = 1.37W$$

Including the conduction losses, the total losses in both FETs are:

$$FET_{LOSS\ TOTAL} = 1.79W$$

The total FET losses recovered using two independent gate drives are:

$$FET_{LOSS\ REC} = 2.47W - 1.79W = 0.675W$$

Each FET will dissipate 0.34W less.

Figure 6 shows an example schematic of the boost example considered.

Summary

Using the LM25037 controller for higher-power boost applications is a simple straightforward approach that can provide benefits over using a typical single gate-drive controller. The benefits can include higher step-up ratios and lower FET losses due to the reduction in transitional losses. Although there are a number of possible approaches to reduce total FET losses in higher-power boost converters, the equations in this article can be used to calculate total losses in the boost FETs for a number of different approaches. Considering the 150W boost converter example, it has been shown that total losses in the FETs are reduced when comparing the LM25037 dual-output gate-drive controller with the LM5020 single-output gate-drive controller.

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