LM5046

Using a Phase-Shifted Full-Bridge Topology in Small Form Factor Power Converters

Literature Number: SNVA610

POWER designer

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No. 132

Using a Phase-Shifted Full-Bridge Topology in Small Form Factor Power Converters

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Introduction

Phase-Shifted Full-Bridge (PSFB) topology has been traditionally used in high input voltage (~400V), high power (>500W) converters that are usually not required to be packed in a small form factor such as the telecom industry standard 1/4th (2.28*1.45 inches) and 1/8th brick format (2.28*0.89 inches). The complexity of the topology, lack of easy-to-use controllers, its perceived benefits only at high input voltages and the use of an additional commutating inductor for resonant transitions are some of the reasons why PSFB topology has not been applied at standard telecom input range of 36V to 75V.The LM5046 is the industry's first PSFB controller with integrated 100V primary drivers. Its high level of integration eases application of PSFB topology into small form factor power converters.

Operation of the Phase-Shifted Full-Bridge Topology

The PSFB topology is a derivative of the classic hard switching full-bridge topology. When tuned appropriately the PSFB topology achieves zero voltage switching (ZVS) of the primary FETs while maintaining constant switching frequency. The ZVS feature is highly desirable as it reduces both the switching losses and the EMI emissions. ***Figure 1*** illustrates the circuit arrangement for the PSFB topology. The power transfer mode of the PSFB topology is similar to the hard switching full-bridge i.e. When the FETs in the diagonal of the bridge are turned-on (Q1 & Q3 or Q2 & Q4), a power transfer cycle is initiated from the primary to the secondary. At the end of the power transfer cycle, COMP turns-off the switch Q3 or Q4 depending on the phase with a pulse width determined by the input

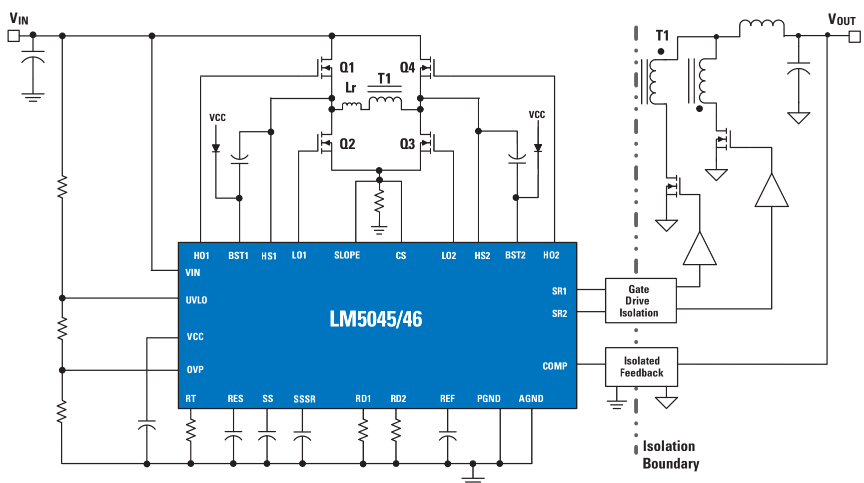

Figure 1. Simplified Schematic of a Phase-Shifted Full-Bridge Converter.

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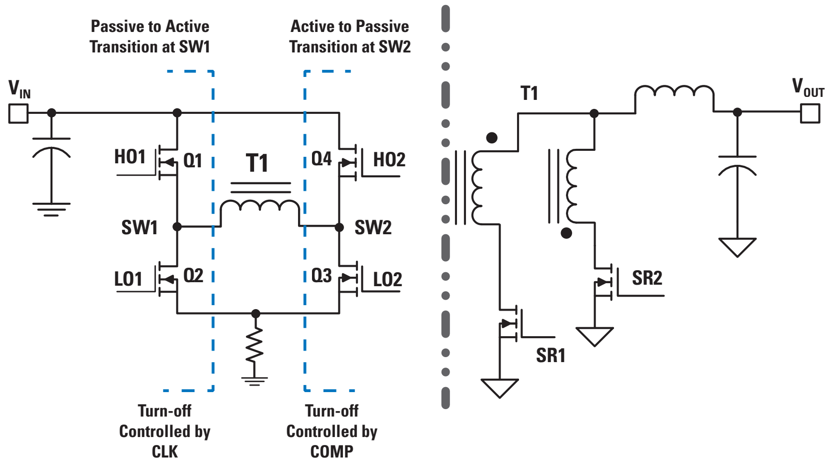

Figure 2. Simplified PSFB Topology Showing the ZVS Mechanism

and output voltages and the transformer turns ratio. In the freewheel mode, unlike the classic full-bridge, where all the four primary FETs are off, in the PSFB topology the primary of the power transformer is shorted by activating either both the top FETs (Q1 and Q4) or both the bottom FETs (Q2 and Q3) alternatively. When turned ON, each diagonal (Q1 and Q3 or Q2 and Q4) applies input voltage to the primary of the transformer. The resulting secondary voltage is then rectified and filtered with an LC filter to provide a smoothened output voltage.

Zero Voltage Switching Mechanism

Active to Passive Transition

As noted, the PSFB differs from the conventional hard-switching full-bridge during the freewheeling period. In the freewheel period, either the top or the bottom FET pairs of the full-bridge are activated. This mechanism facilitates zero voltage switching for all four primary FETs. For example, the power transfer cycle enabled by activating Q1 and Q3 is terminated by turning-off Q3 and the freewheeling cycle is initiated by activating Q4. Once Q3 is terminated, the reflected load current plus the magnetizing current propels the SW2 node towards the V_{IN} and activating Q4 at that instance results in ZVS. This transition, shown in ***Figure 2***, is often called the active to passive transition (power transfer to freewheel transition). The active to passive transition time can be approximated by using the following formula:

Equation A

$$T_{AP} = \frac{C_{parasitic} \times V_{IN}}{\left(I_m + \frac{I_{LPEAK}}{N_{TR}}\right)}$$

Where, I_m is the magnetizing current, N_{TR} is the power transformer's turns ratio, I_{LPEAK} is the peak output filter inductor current and $C_{parasitic}$ is the parasitic capacitance at the node SW2. The LM5046 is setup such that the SW2 node always sees active to passive transition.

Passive to Active Transition

At the end of a freewheeling cycle (and end of one switching period), the primary switch Q1 is turned-off. The voltage at the node SW1 begins to fall towards the GND due to the resonance between leakage inductance of the power transformer plus any additional commutation inductor and the parasitic capacitances at SW1. At this instant, ZVS can be realized by turning on the switch Q2.

The magnetizing inductor is shorted in the freewheel mode and therefore does not play any role in this transition. The LC resonance results in a half-wave sinusoid whose frequency is determined by the leakage inductor and parasitic capacitor. The passive to active transition time can be approximated by using the following formula:

Equation B

$$T_{PA} = \frac{\pi}{2}\sqrt{(L_{leakage} + L_{commutation}) \times C_{parasitic}}$$

Where, $C_{parasitic}$ is the parasitic capacitance at the node SW1.

The peak of the half-wave sinusoid is a function of the load current and the additional commutating inductance and/or leakage inductance and is given by

Equation C

$$V_{PK} = \frac{I_L}{N_{TR}}\sqrt{\frac{(L_{leakage} + L_{commutation})}{C_{parasitic}}}$$

From ***Equation A*** it is evident that the active to passive transition can always result in ZVS as long as sufficient dead-time is inserted. However, from ***Equation B and C***, it can be seen that the passive to active transition can result in ZVS only if there is enough energy stored in the commutating inductor and/or leakage inductance.

Fitting into a Small Form Factor

The power density in small form factor power converters such as the 1/4th and the 1/8th brick format is constantly increasing. With increasing power density new topologies are being pursued, more efficient high power topologies are being employed into lower power applications. Topologies such as the full-bridge and the PSFB used in high power and bulky converters are finding applications in small form factor power converters. To facilitate this trend, a PWM controller with integrated drivers and a high level of control logic integration that simplifies the use of complex topologies is essential. Further, to meet the height requirements, a PC board integrated planar transformer is also required. The PSFB topology with its ZVS feature can accommodate higher frequencies so that the sizes of bulky passive components are reduced.

Example

A 150W PSFB power converter was built using the LM5046 in the telecom industry standard eighth brick (2.28*0.89 inches). The operating input voltage range is 36V to 75V and the output voltage is 12V. The output current capability is 12A. The converter is configured for current mode control with robust hiccup mode current limiting that initiates at 13A of average load current. The power converter operates at a frequency of 420 kHz. The PCB integrated transformer has 5 turns in the primary and 2 turns in each secondary. The primary and secondary turns were not interleaved and were stacked serially to deliberately increase the leakage inductance to about 1 µH. The efficiency curves for the LM5046 are shown in *Figure 3*. The following are the reasons that made this integration possible:

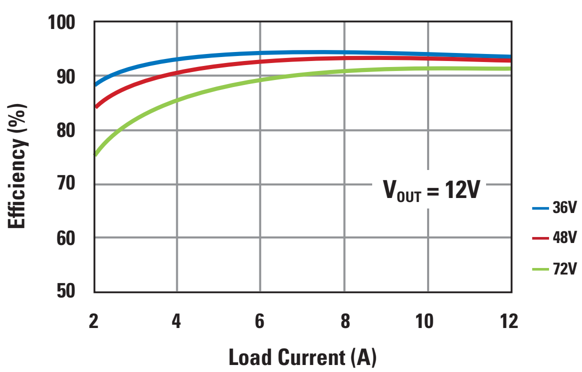

Figure 3. Efficiency Curves for a 150W DC-DC Converter Built Using the PSFB in Eighth Brick Format.

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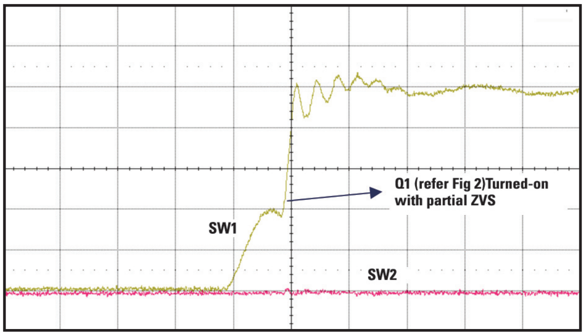

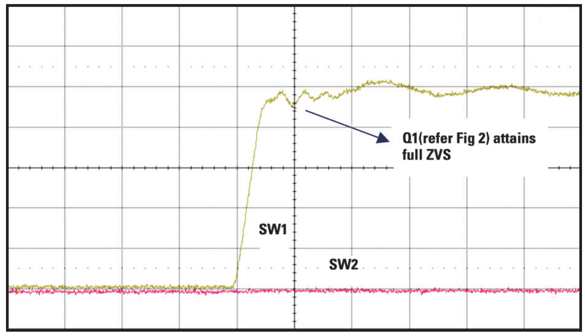

(A) (B)

Figure 4. Passive to Active Transition at Partial Load (A) and Full Load (B) Condition

Highly Integrated PWM Controller Driver

The LM5046 is the highest integration controller for small form factor, high density power converters. It features four integrated gate drivers with 2A source and 3A sink capability which saves the use of the two 8-pin half-bridge drivers that are required to implement a PSFB converter. Approximately 50% PC board area is saved by using one LM5046 in a LLP package over a traditional PSFB controller plus two extra gate drivers in LLP package. This is highly desirable as it frees up lot of valuable PCB real estate.

LM5046 also includes intelligent synchronous rectifier startup to enable linear turn-on into pre-biased loads. LM5046 comes with a 100V startup regulator and other features such as optional hiccup mode, wide-bandwidth opto coupler interface, and integrated UVLO and OVP comparators that avoid discrete circuitry.

Commutating Inductance

From *Equation C*, it can be seen that during the passive to active transition the peak of the half-wave sinusoid depends on both the load current and the commutating inductance. Therefore to enable ZVS at light to medium load conditions considerable commutating inductance is necessary.

The additional commutating inductor needs be selected such that the combined core and copper losses associated with it do not swamp out any gain in efficiency due to ZVS. This often leads to a physically large inductor. While in high input voltage (~400V) applications it is a common practice to use an additional commutating inductor, due to the real estate challenges in the 1/4th and 1/8th brick format power converters the use of an additional inductor is unattractive.

By deliberately increasing the transformer leakage inductance the available commutating inductance can be increased. This can be achieved by avoiding the primary and secondary interleave and stacking the windings serially. It should be noted that conventionally leakage inductance is kept to a minimum by interleaving the primary and the secondary. Further, one additional advantage of integrated transformers is that by design they reduce the variation of the leakage inductance in mass production compared to wound transformers.

The only drawback of this approach is that depending just on leakage inductance might not be enough to enable ZVS under all the load conditions. In such a situation, the switching losses will occur. However, since the capacitive losses are proportional to V^2, the losses will reduce considerably even if SW node rises to at least half the input voltage as shown in *Figure 4* and it is still considerably better than hard switching. Even though there is some switching loss at light load conditions, the overall efficiency achieved (as shown in *Figure 3*) by employing PSFB is excellent.

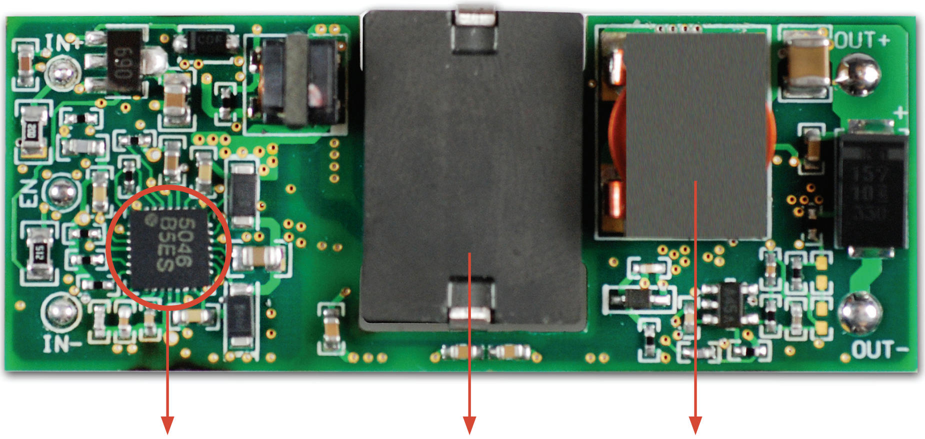

Figure 5. Top Side View of the Eighth Brick

Figure 5 shows the 1/8" brick board with the chief components highlighted.

Conclusion

With ever increasing power density, topologies such as the PSFB which have only been used in the past for high-power and bulky designs, are now finding applications in small form factor power converters. The trend is here to stay. To facilitate this trend, highly integrated PWM controllers are necessary and LM5046 is a big first step in that direction. Intelligent choices need to be made in the transformer design such as integrated transformers and avoiding interleaving the primary and the secondary windings. Increasing frequency of operation to reduce the size of passive components is a must. Further, topologies such as PSFB with ZVS switching will gain more prominence as it enables increasing frequency without incurring major efficiency loss while reducing EMI emissions.

References

LM5046 Datasheet

LM5046 Lab Demo Video

LM5046 Evaluation Board

AN-2126 App Note for LM5046 1/8 Brick Reference Design

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