Uninterruptible Synchronization Clock Circuit

SVA - SimpleSwitcher

Devices that utilize a phase-locked loop (PLL) for accepting an external clock signal for synchronization, may not operate as expected if the external clock is removed. Once the PLL recognizes a clock is present, the device relies on the PLL to control the switching frequency and ignores the frequency setting resistor. However, if the PLL is controlling the switching frequency and the external clock is removed, the PLL waits for a clock pulse that never comes. There is a time-out period that the PLL must wait before it recognizes that no clock is present and switches to the frequency setting resistor. During the time-out period, the PLL frequency decreases. The time-out period could be long enough to cause problems for your system, such as over-current or increased ripple. For the LMZ3 Simple Switcher power modules the switching frequency drops to approximately 100 kHz before returning to the switching frequency set by the RT resistor.

Using a CMOS 555 timer (such as LMC555) configured as shown in Figure 1, between the external synchronization clock signal and the RT/CLK pin of the LMZ3 power module, will ensure a clock signal is present at the RT/CLK pin even if the external clock signal goes away. In this configuration, as long as the external synchronization clock is present, the clock pulses at the output of the 555 timer will be at the same frequency as the clock signal at the RESET pin. However, if the external synchronization clock is disabled, the 555 timer will continue to output clock pulses at the frequency set by the external R and C, without missing a pulse. **The external clock signal must be programmed to a High state when the clock is disabled (if not, the signal can be inverted before the 555 timer).** The frequency of the 555 timer should be programmed to approximately the same frequency as the external clock for the most seamless transition when the external clock is removed.

Figure 1 shows the schematic of an external synchronization clock feeding the RESET pin of a 555 timer and the output of the 555 timer is feeding the RT/CLK pin of an LMZ3 device. The values for R and C can be selected from Table 1 or can be calculated using Equation 1. The scope shot in Figure 2 shows the external sync clock on trace 2 (blue). The clock pulses are present at first, then the clock goes away (High), and then the clock starts switching again. Trace 1 (pink) shows the clock pulses at the OUT pin of the 555 timer, feeding the RT/CLK pin of the LMZ3 device. Notice that the clock pulses feeding the RT/CLK pin of the LMZ3 device never go away. During the period when the external clock pulses are missing, the 555 timer produces the clock.

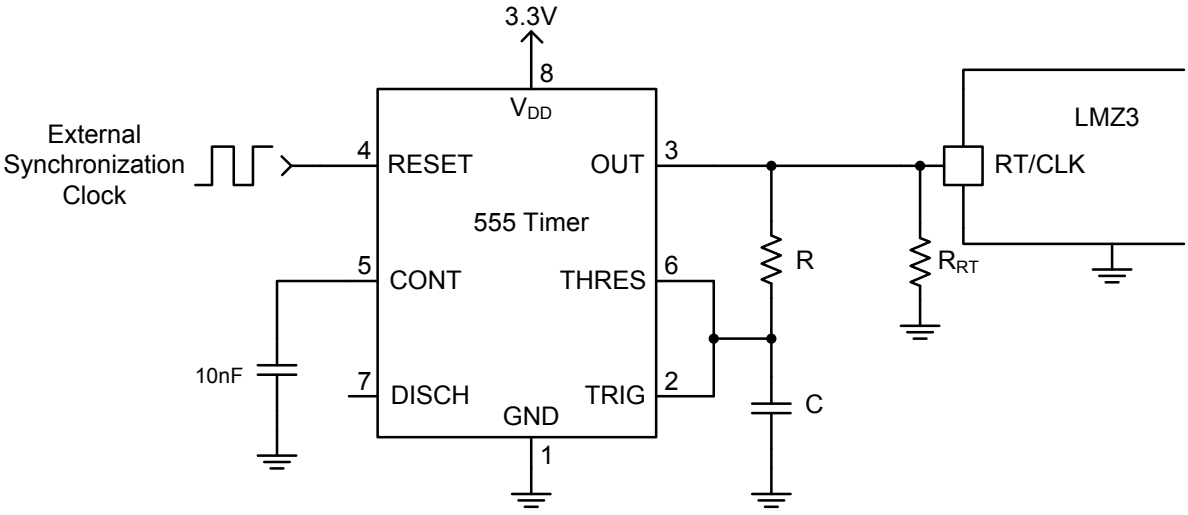

Figure 1. 555 Timer Uninterruptible Clock Circuit

$$Freq = \frac{1}{1.4 \times (R \times C)} \quad (1)$$

Table 1. 555 Timer Frequency Setting

Freq (kHz)	250	300	350	400	450	500	550	600	650	700	750
R (kΩ)	13	11	9.31	8.25	7.32	6.49	5.9	5.49	4.99	4.64	4.32
C (pF)	220	220	220	220	220	220	220	220	220	220	220

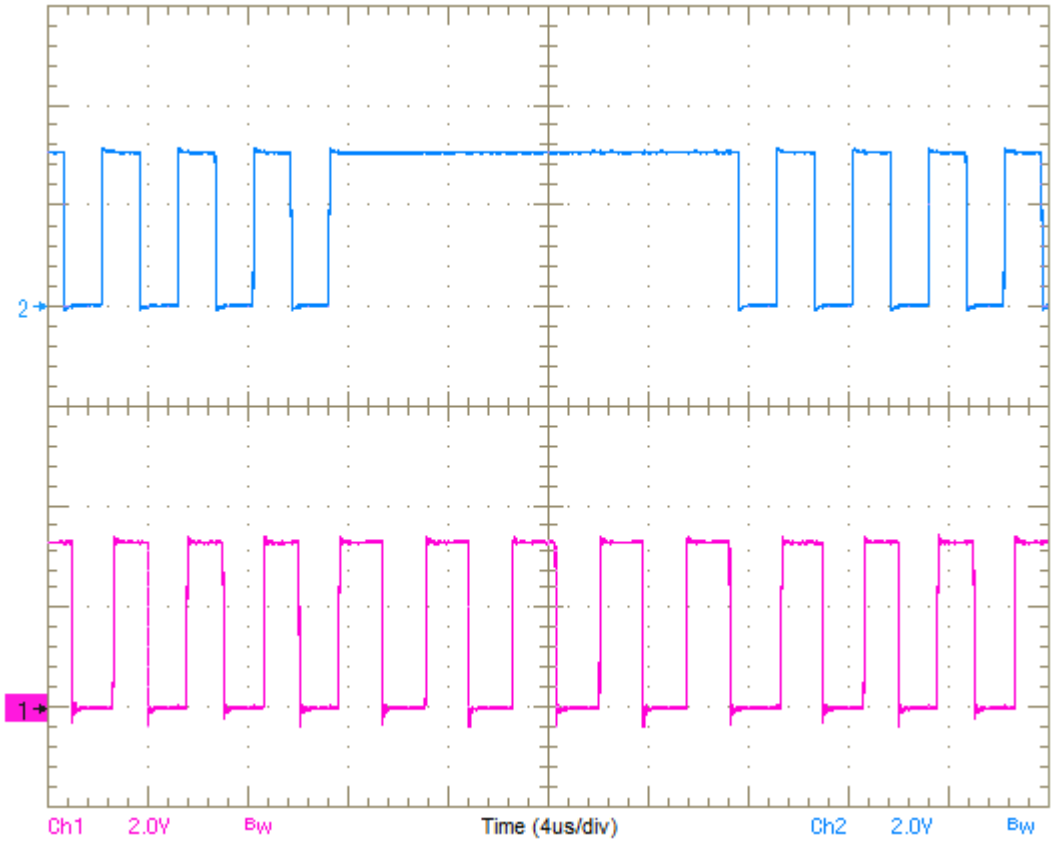

Figure 2. Sync Clock and 555 Timer Output Pulses

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