

Enhancing Bit-Flip Recovery and PMU Design for Defense/Industrial Applications

Application Report



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Abstract

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ABSTRACT

Customers have evaluated several TI power-management (PMU) devices and have found that some designs can make the PMUs operate beyond typical data-sheet application specifications. This report reviews the backgrounds of various relevant design features of a family of 5-V CMOS sub-PMUs, suggests solutions to accommodate system requirements, mitigates radiation concerns, and proposes best practices for new PMU designs.

1 Introduction

Low-voltage PMUs are increasingly being deployed in tactical applications for defense and industrial applications. This article addresses how a designer can deploy commercial PMUs and operate them effectively in transient harsh environments. Concrete design considerations are provided to enable CMOS mixed-signal devices perform more robustly in a bit-flip circumstance, bit-flip meaning that the register or memory cell could change logic state from 0 to 1 or 1 to 0 under the influence of electromagnetic interference (EMI) or ionization radiation.

2 Harsh Environments

In industrial applications electronic circuits often are subject to harsh and noisy EMI. These circuits must be designed and properly shielded to guard against interference or possible damage from such severe operating ambient. People familiar with the sight and sound of elevator motors, arc welding, or thunderstorms can relate their experience to similar disturbances on the radio or cell phone. In some defense and industrial applications electronic systems can encounter intense electromagnetic pulse interference. Hence, these systems need to be well designed and strongly shielded to withstand and recover from the disturbance.

3 Mission-Critical System Considerations

One of the most important components in a system is perhaps the PMU and point-of-load (POL) regulators, which are often neglected in the early stages of design. A feeble PMU is the last thing an engineer wants because, in worst-case scenarios, unreliable power rails and distribution may cause the system to fail. [Table 1](#) shows a partial list of TI CMOS-5V sub-PMUs and key features which users have evaluated or selected devices for critical mission applications.

Table 1.

Device ID	Regulators	-Q1 Grade	Output Selection	UVLO	Spread Spectrum	Thermal Flags, TSD	Power-u/d sequencing	nPOR + Buck Power Good	Power Good	Ext. Sync
LM3370	dual bucks	-	I ² C	-	Yes	TSD	pin enable	nPOR	2 pins	-
LM26480	dual bucks, dual LDOs	Yes	external resistors	Yes	-	Yes	pin enable	single pin w/ fixed delay	integrated	Yes
LM26484	Dual Bucks, Dual LDOs	-	external resistors	Yes	-	Yes	pin enable	single pin w/ fixed delay	integrated	-
LP3906	dual bucks, LDO controller	-	I ² C	Yes	Yes	Yes	Auto sequence, programmable delay or pin enable	-	integrated	Yes
LP3907	dual bucks, dual LDOs	Yes	I ² C	Yes	Yes	Yes	Auto sequence, programmable delay or pin enable	single pin, programmable delay	integrated	-
LP8731	dual bucks, dual LDOs	Yes	I ² C	Yes	Yes	Yes	Auto sequence, programmable delay or pin enable	single pin, programmable delay	integrated	-

The PMUs discussed herein are mostly dual-bucks and/or dual low dropout (LDO) regulators for broad-market uses. Initially they were intended for consumer, industrial, and vehicular applications such as powering application processors, DSPs, FPGAs, dashboards, compasses, infotainment systems, sensors, and radios, among others. Their commendable performance and cost effectiveness have also made them good solutions for mission-critical systems applications. In tactical arenas, for example, some are designed into night-vision gears, GPS radios, fire-controls, camera systems, and portable and handheld field gears.

Adjustable output PMUs can be programmed on the fly or set via external resistors. Additionally, default outputs and feature parameters can be factory-programmed via non-volatile memories. Because register and floating gate memory are involved, system interaction with every PMU programmable features needs to be understood. Good design considerations and time-proven practices are imperative for ensuring robust recovery from a severe electromagnetic interference event.

In mission critical systems, adequate protection and shielding are always in place to prevent permanent damage to the integrated circuit (IC) components upon multiple exposures to severe electromagnetic pulse. Nonetheless, gradual device performance degradation and soft errors may result. There might be subtle system design concerns on soft error and bit-flip effects from PMU control registers and non-volatile memory cells used in default configurations. Examples include output, sequencing time delays, nPOR pulse delay, supervisory circuits, and so on.

4 Design Consideration for Configurable PMUs

In a mission-critical system, for example, a system is mandated to power down prior to any severe electromagnetic disturbance event. After the disturbance has passed or dissipated, the system executes a discharge routine. Power cycling then begins by loading the default system configuration to the control registers. The internal power-on-reset (POR) signal initiates the loading of factory programmed EPROM cell contents to the relevant control registers. Next the output power rails sequence up, setting the modes of operation, and commencing supervisory functions in this order.

When these tasks are completed, and PMU recovery is successful, the system can resume normal operations. In such a circumstance, programmable PMUs might potentially experience bit-flips in memory cells, which is a concern that requires system design consideration. While system failures in tactical equipment can be easily replaced, generally they mandate that electronic systems remain functional throughout any electromagnetic disturbance events.

5 PMU Output Voltage Programming

Regulator outputs may be programmed by control registers and defaults are set by non-volatile memory, or they can be fixed with external resistors. The latter is more convenient because the user has an infinite choice of values within the specification range as well as avoiding the delay, cost, and limited values made available by IC vendors. Passive support components are unaffected by any abnormal EMI disturbance. Even if component values deviate slightly, they only incur a transient disturbance and circuit functional changes are unremarkable. For control register memory-aided programmable output regulators, the effects of output default to higher voltages than target values should be considered when temporary or permanent register bit-flip occurs. If the circuits to be powered can tolerate the full range of the regulator output, then there is no issue. But, for loads like sensitive sensors and flash memories that require low voltages and tight tolerance, they should have clamping protection or a design-around to prevent from high-output voltage issue.

Figure 1 shows a practical clamping circuit that shunts excess current thus preventing accidental overvoltage to the sensitive load to mitigate the issue. After a power-up sequencing, the system application processor can reconfigure the PMU control register settings, returning all regulator outputs to their target voltages.

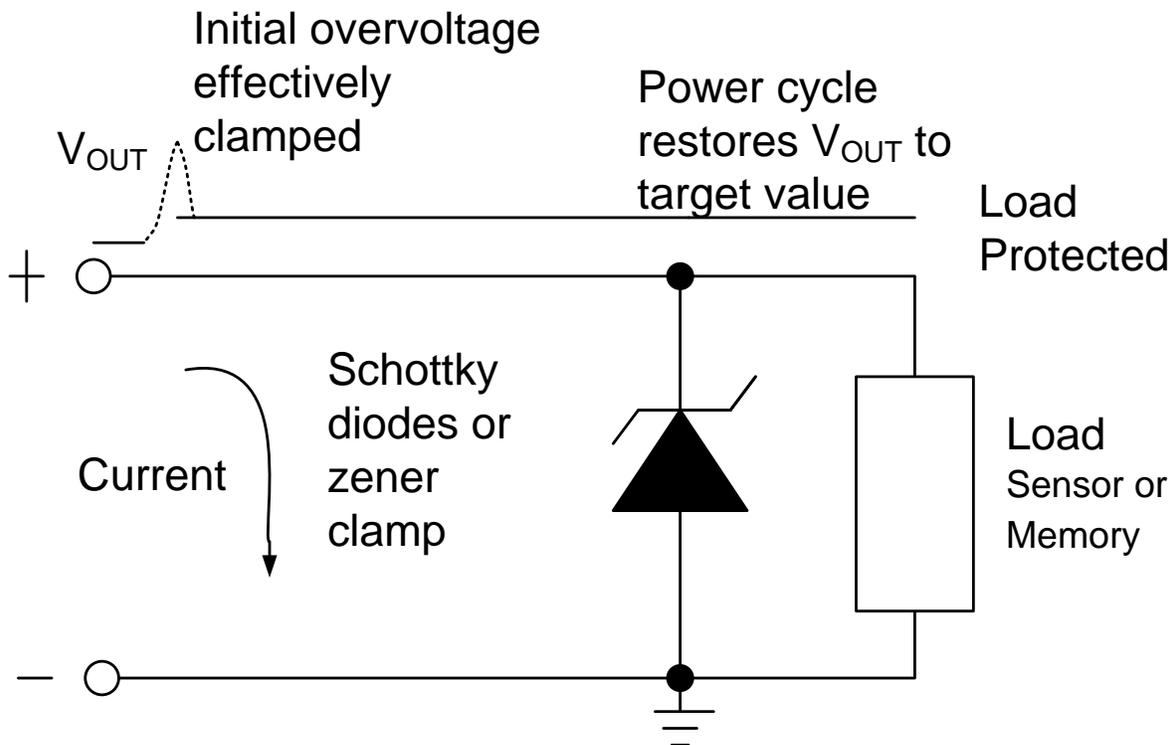


Figure 1. Practical Clamping Circuit

Only PMUs with a built-in spread spectrum clock feature and I²C interface are user configurable. Should a bit-flip corrupt the default modulation parameters or enable settings, these parameters and settings can be recovered by reconfiguring the control register contents upon power cycling. The switching regulators oscillator frequency is typically trimmed to 10 percent accuracy. Should the EPROM cells experience a permanent bit-flip, the oscillator frequency is slightly offset and should incur no functional issues. If more accurate frequency or synchronized clock operation is required, then selecting a switcher with external sync option is recommended. Similarly, a switcher pulse-frequency modulation/pulse-width modulation (PFM/PWM) default mode setting issue is not likely to affect system operation because reconfiguring the register bit can recover the modulation setting to the desired mode.

Moreover, the switcher ramp rate typically is set at 8 mV/μs as the default. The ramping range can be selected either native fast or from 1 mV/μs to 10 mV/μs in increments of 1 mV/μs. A good system design should ensure that the system can accommodate the native ramp rate because there are no user control registers involved in the event of a permanent bit-flip occurrence. Likewise, an undervoltage lock out (UVLO) default typically is set between 2.6 V to 2.9 V with no user-control register, except for the enabled/disabled bit. Generally there are no concerns if a disturbance affects the target default because the range is relatively narrow, and the main supply is usually well-regulated in these applications. For battery-operated systems, input is fairly constant until UVLO, so either disable this feature or deploy a backup solution. The UVLO enable/disable register bit can be restored upon power cycling.

For PMUs with nPOR output, the pulse delay time default ranges from 50 μs to 200 ms. Likewise, it has no user control registers. A system should be designed to accommodate the shortest pulse delay in the event of an irrecoverable bit-flip. Alternatively, one can augment it with a pulse stretcher to ensure the desired pulse delay be used for system reset.

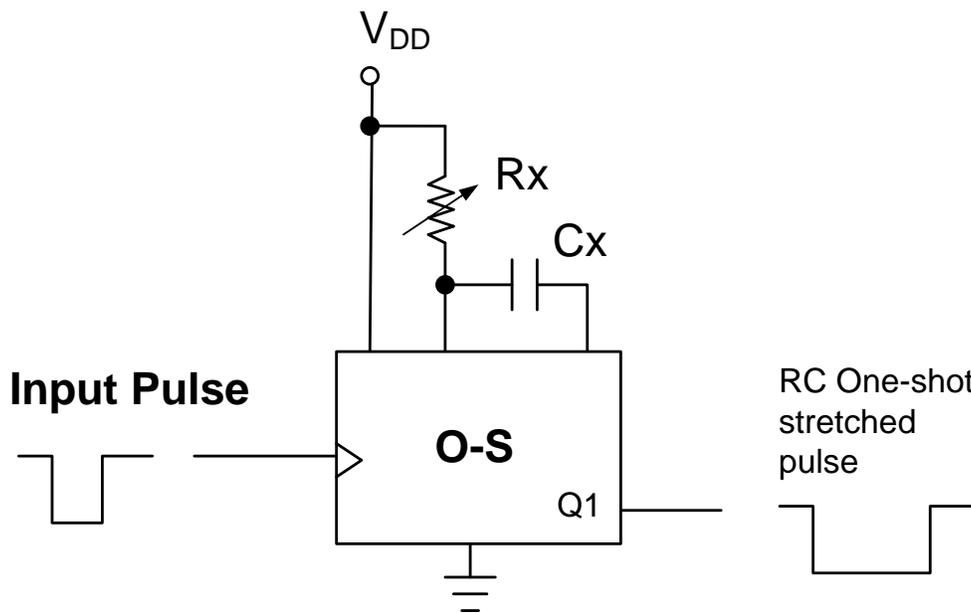


Figure 2. RC-Based One-shot Pulse Stretcher

Figure 2 depicts one method for implementing a suitable pulse delay (a RC-based one-shot pulse stretcher) that may be used to prevent a short nPOR pulse from properly resetting various devices in a system. PMUs with power-up auto sequencing have a default delay time setting of 1.0 ms to 6 ms in five steps on delays between regulators during power-up or down, with no user control registers involved. A system should be designed to accommodate the minimum time delay of 1 ms between regulators during sequencing, should a bit-flip cause a default setting change.

Enable control is an option that mission critical user may consider. All PMUs in Table 1 have enable-pin control to facilitate custom sequencing order and time delays. This allows greater flexibility system implementation that user could take advantage where off-chip hardware can effect more robust design such as redundant power sequencing.

Lastly, a desirable option for these PMUs is an alternative to EPROM-based memory cells. Polysilicon and metal fuse technology have already been used in analog circuit trimming and for digital configuration in the industry. As cost and reliability improved, new PMUs need to employ laser programming techniques via fuse-cells to configure non-user accessible defaults and trims to obviate bit-flip issues from current EPROM and EEPROM technology. Existing PMUs need be considered to provide non-EPROM-based options for defense and critical need potential customers. As a general precaution, user should best make it a system flow to reconfigure functional-feature control registers upon power cycling in case of bit-flip default registers occurs.

6 Summary

Low-voltage PMUs have been popular in consumer and industrial sectors. Recently, they are being designed into mobile and field defense systems. In such applications PMUs can be subjected to intense electromagnetic pulse effects. Increasingly, standalone LDOs and switching regulators are being integrated in flexible and programmable PMUs, delivering versatile uncompromising system-on-chip (SOC) performance. With the convenience of control registers and EPROMs for programming defaults, it is important that system engineering coordinates the minimum best timing and default parameters of PMUs with system start-up needs. This ensures reliable recovery from potential electromagnetic disturbances. An overview of modern adjustable PMUs' voltage control, mode setting, and supervisory functions is presented with their companion system design considerations. Proven good practices of the trade are discussed to enable PMUs to recover from scenarios of bit-flip in registers or change of state in EPROMs.

Using mature technology in advanced PMUs complements proper protection/shielding techniques, making permanent memory bit-flip less likely to occur. Furthermore, abiding proper design-application considerations, default issues can be obviated in the event of non-volatile memory upset. New PMU products should use laser fuse as non-volatile programming technique to replace EPROMs and EEPROMs to further improve device applications in harsh operating environments.

7 References

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