Soft-start Using Constant Current Approach

Akshay Mehta, Frank De Stasi

ABSTRACT

In many systems backup power is provided either by batteries or simply by a large value capacitor. In these applications the capacitor would only provide the current when the primary power source fails. Further, these applications are usually for light load currents. During normal operation the backup capacitors are kept charged up by a DC/DC converter. The challenge involved in an application like this is how to charge up the large value capacitor without overwhelming the input power supply and/or causing the DC/DC regulator to malfunction. This application note addresses that challenge.

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1 Introduction

Charging large capacitors at the output of a DC/DC converter can be a challenge. When the capacitor is completely depleted and is charging up from 0V, it is going to pull large currents from the input power supply which may cause the supply to crash or in some other cases cause the DC/DC regulator to malfunction. To address this issue longer soft start times are added to the charge up of the capacitor. But even then in most devices maximum allowable soft-start times are about 10ms. This time is not going to be enough when you want to charge up a capacitor of more than 1000µF up to a few Farads. This is when you would need an external soft-start circuit that can provide a custom soft-start time.

This application note addresses this issue by using the LM2588 in a SEPIC configuration with an external circuit which works as constant current controller. The LM2588 is part of the LM258x family of SIMPLE SWITCHER® boost regulators from Texas Instruments. The internal NPN is capable of handling a voltage of 65V and has a current limit of 6.5A. The maximum input voltage that the device can handle is 40V. Thus this device makes a good candidate for wide V_{IN} solutions. The design shown here is created for a typical input of 5V and an output of 12V.

2 Basic Operation

The LM2588 SEPIC circuit is shown in Figure 1. During the on-time of the internal NPN, the current is flowing from the input through L1 in to the internal power switch. The catch diode would thus be reverse biased and the output capacitor will now be providing the current to the load. The SEPIC cap is now charging up to V_{IN}. During the off-time of the power switch, the polarities on the inductors are reversed to maintain the same current flow through them. The diode is forward biased causing V_{OUT} to be established on L2, and V_{OUT} + V_{IN} at the switch node.

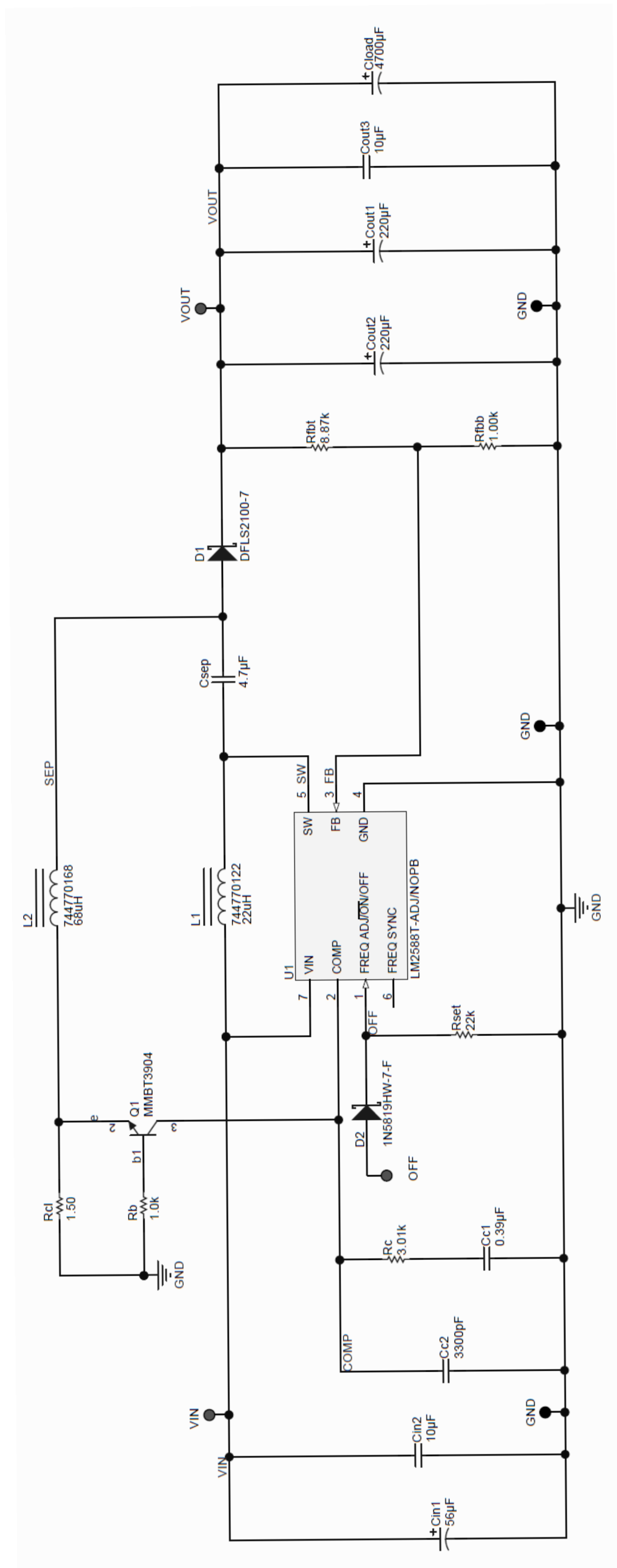

Figure 1. Design Schematic

3 External Soft-start

The SEPIC topology is chosen for this application because of the intended method of adding extra soft-start time. The SEPIC topology allows low side current sense because of the direction of the current flow through L2. Low side current sense is generally preferred because it keeps the sensing circuit simple and doesn't require it to be level shifted.

In normal condition at startup since the output voltage is low, the error generated inside the IC is large. This causes the error amplifier to increase its output in order to increase the duty cycle and help transfer current to the output. A large value capacitor will want to charge immediately to the output voltage and thus require a large current. Due to the large duty cycle, a large current will be drawn from the input source which can cause it to crash. In another situation where the input supply is capable of providing large currents but the DC/DC regulator doesn't have a limited maximum duty cycle, it will cause the device to stay on all the time and consequently the output voltage will never get established. It is therefore important to limit the inrush current and adding extra soft-start time is one way to do it.

In this application the extra soft-start time is added by controlling the COMP pin of the IC during the charging of the large capacitor. A current sense resistor is added in series with the secondary winding to ground. Thus during every switching cycle, the current flowing through the sense resistor and the inductor will causes a slight voltage drop across sense resistor. Consequently the emitter of Q1 will be a bit below ground. The base of Q1 is tied to ground through a resistor. Therefore with every cycle, the NPN turns on and yanks down on the COMP pin. This limits the COMP voltage from railing and forces a maximum duty cycle. This in turn prevents a large inrush current draw from the input power supply.

The sense resistor is part of the steady state circuit too. This means that the steady state current that can be pulled from the output will also be limited. We can use the following equations to estimate the steady state output current that can be delivered. The duty cycle for the SEPIC topology is:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad (1)$$

The ripple current through L2 can be calculated as shown.

$$I_{PP} = \frac{V_{IN} \cdot D}{L_2 \cdot F_{SW}} \quad (2)$$

The peak current through L2 will be limited because of Q1. It can be estimated as

$$I_{PK} \approx \frac{V_{BE}}{R_{CL}} \quad (3)$$

Now knowing the peak and the ripple current, the average DC current can be estimated as

$$I_{OUT} \approx I_{PK} - \frac{1}{2} \cdot I_{PP} \quad (4)$$

This value will not be exact and will depend on the V_{BE} drop and resistor tolerances. Since the addition of the circuit limits current delivered and also the maximum duty cycle, it increases the time it takes for V_{OUT} to reach regulation. This time is directly proportional to the value of the resistor. Larger resistor values will cause longer soft-start times and vice versa.

4 Test Results

In this example the output capacitor is 4700µF. Figure 2 shows the converter starting-up with no external soft-start.

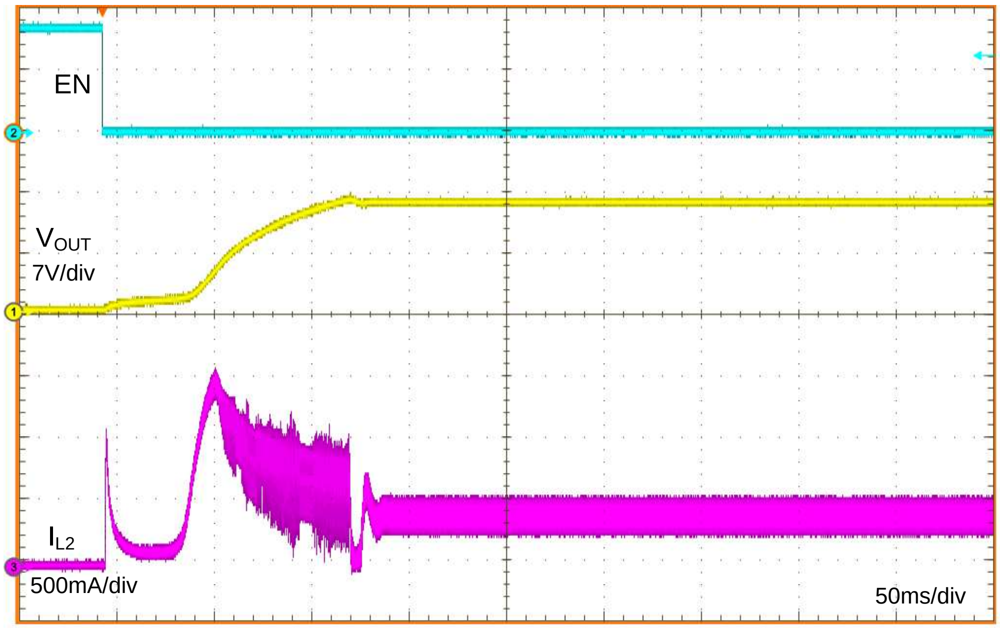

Figure 2. No External Soft-start

With the addition of Q1 and R_{cl} = 0.75Ω, we get the results shown in Figure 3

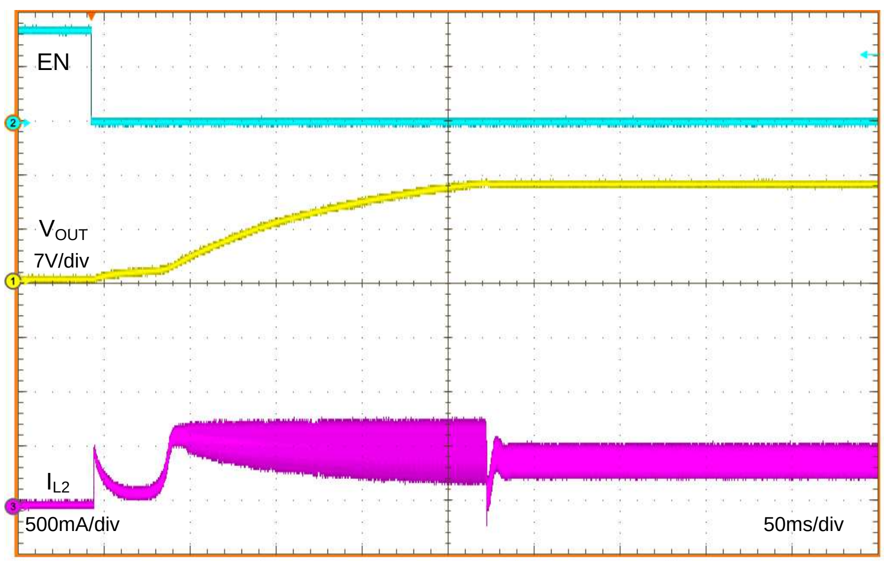

Figure 3. With External Soft-start; R_{cl} = 0.75Ω

Increasing the value of R_{cl} to 1.5Ω will increase the soft-start time and reduce the inrush current further. This is seen in Figure 4.

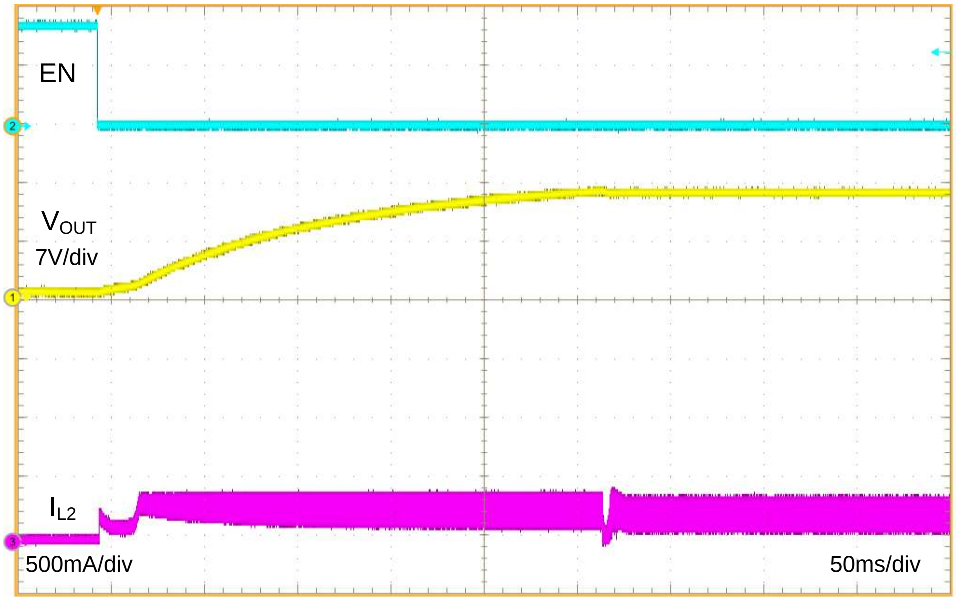

Figure 4. With External Soft-start; R_{cl} = 1.5Ω

Since the external soft-start circuit stays in effect during the steady state operation, this puts a limit on the maximum obtainable load current. Table 1 gives an idea of how the load current will change with change in the value of R_{cl}.

Table 1. Max Steady state I_{OUT}

R_{cl}(Ω)	I_{OUT}(A)
1.5	250mA
0.47	540mA

5 Conclusion

Thus we see that in situations where the inrush current needs to be limited and the maximum soft-start time set by the IC is not enough, addition of external soft-start time is needed. The circuit demonstrated does that and is able to limit the inrush currents.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265