

Analog PWM Dimming in White-LED Drivers

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ABSTRACT

Pulse-width modulation (PWM) is a common type of dimming used to adjust the current in white-LED driver devices. PWM dimming takes a rectangle waveform with variable positive duty cycle (D) and adjusts the LED current proportionally. For many smaller format white LED drivers (7-inch screen size or smaller), the PWM signal is converted to a DC control voltage and made to drive the LED current in a DC (or analog) method. This application note discusses some of the benefits and drawbacks of a PWM-to-analog dimming method.

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1 PWM Dimming

PWM dimming can be grouped into two major categories:

- True PWM
- Analog PWM

1.1 True PWM Dimming

In true PWM dimming the LED current is turned on/off at the programmed duty cycle and frequency. The frequency can be the same as the input PWM signal (direct PWM), or can be at a different frequency (indirect PWM). True PWM has been, for a long time, considered better in preserving the white point of the LED light output. The argument is made that because the peak current is the same across the entire dimming range, the white point vs current will be unchanged. This has largely been deemed as not truly an issue, and in fact most (if not all) smart phones have adopted either a PWM-to-analog control or an I2C-to-analog control.

Although the white-point shift may or may not be an issue, true PWM does hold a couple definite advantages. First, offset errors at low currents are largely avoided because the LED current is turned on/off at the maximum current. This allows for the reference voltage to maintain a high level, well above any offset induced errors. Secondly, LED brightness at very low DC current can have large errors in light output. These errors can occur when the LED is biased at < 0.1% of its rated current. True PWM avoids this because the LED current is constant and near a high level at all brightness levels.

1.2 Analog PWM Dimming

Analog PWM dimming takes the PWM input and converts it to an analog control signal. This analog control signal is used to adjust the voltage reference, which then sets the DC LED current (either across an external feedback resistor, or in a regulated current sink). The primary benefit of PWM-to-analog dimming is its low noise operation. Because the LED current is always continuous at the output, it is essentially noise free. This eliminates any acoustic noise generated due to large voltage fluctuations across ceramic output capacitors.

Another benefit with PWM-to-analog dimming is the better efficiency vs load current. In true PWM dimming, when the LED current is on, the switch and inductor are always conducting the maximum load current. This forces the maximum possible I^2R losses in the resistive elements (inductor, switch, diode) of the circuit. In the PWM-to-analog dimming driver, the lower brightness levels always force lower conduction losses. For example, consider a true PWM driver with 400-mA peak inductor current operating at 50% duty cycle. The power loss in a 0.3- Ω inductor is ($PL = 400 \text{ mA} \times 400 \text{ mA} \times 0.3 \Omega \times 0.5 = 24 \text{ mW}$). Compare this to a PWM-to-analog driver with the same average load ($PL = 200 \text{ mA} \times 200 \text{ mA} \times 0.3 \Omega = 12 \text{ mW}$). In reality the PWM-to-analog driver would be even lower considering the lower V_{OUT} and the elimination of added losses required to slew the LED current on/off that exist in the true PWM driver.

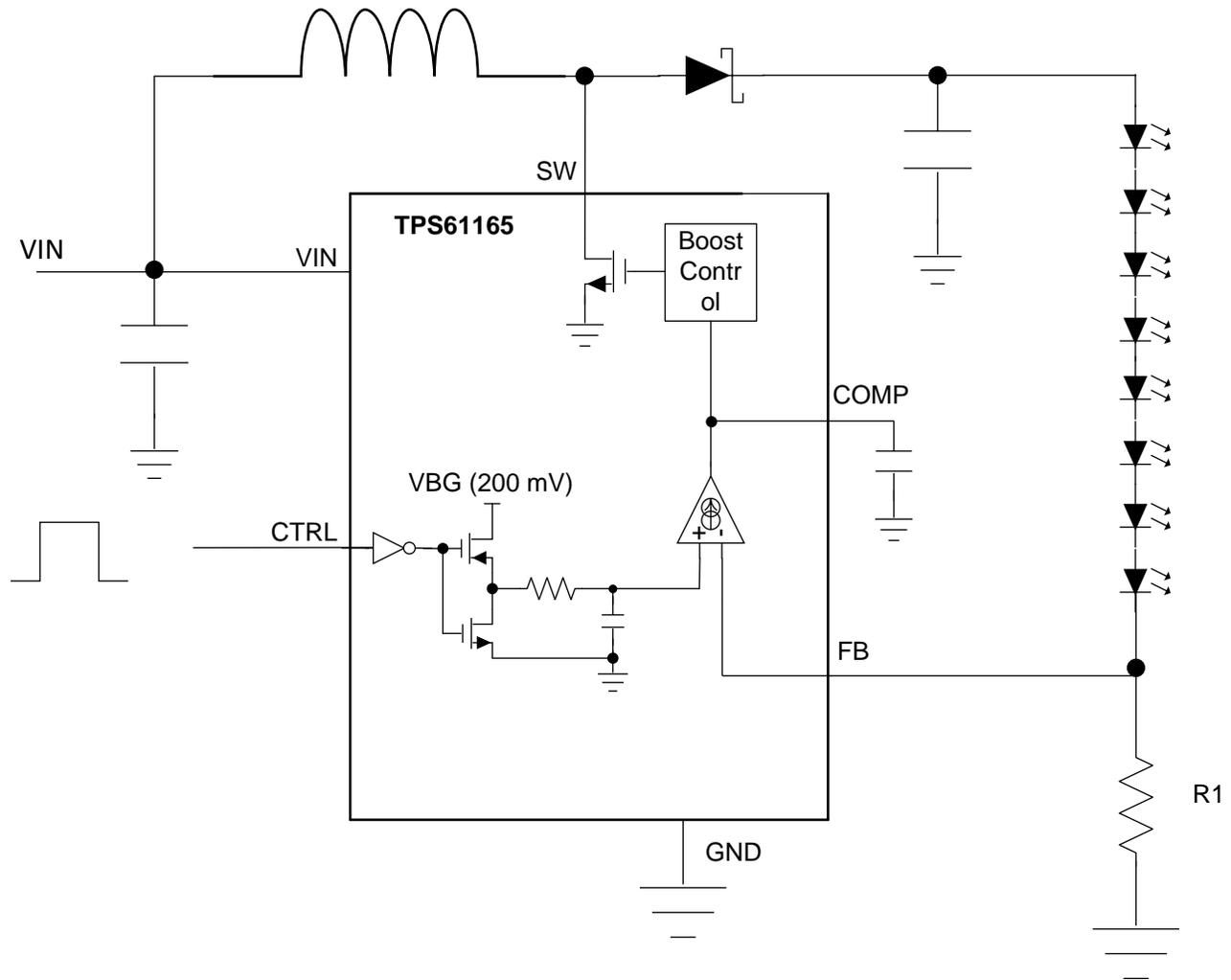
2 PWM-to-Analog Methods

Two primary methods are used to convert the PWM input signal to an analog control voltage. The first method uses a low-pass filter (LPF). This can be integrated into the device (typical) or can exist as an external filter capacitor. Once filtered the analog signal is used to drive the error amplifier (or current sink).

The second method uses a PWM sampler. Here the PWM input is continuously sampled and converted into a digital code, which is fed into a digital-to-analog converter (DAC) and then used to drive the error amplifier (or current sink).

2.1 Low-Pass Filter

Adding a low-pass filter in line with the PWM input is the simpler of the two PWM-to-analog dimming methods. An integrated filter turns the PWM input into a DC reference voltage, which is then used to set the voltage at the boost FB pin, (or used to adjust the current in an integrated current sink). [Figure 1](#) shows a typical LED driver incorporating an LPF in a boost white-LED drive incorporating an external RSET. The logic level PWM signal is buffered and level shifted so it swings between the reference voltage (VBG) and GND. The filtered signal is then used as the reference for the boost error amplifier, forcing the FB node to regulate to VREF in order to set the LED current across the low side resistor R1.



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Figure 1. LED Driver With Low-Pass-Filtered PWM Input

Figure 2 shows the low-noise-output response with the filtered PWM-to-analog dimming circuit of Figure 1. Channel 1 (VFB), and channel 3 (VOUT) show a constant DC (low noise) waveform. CTRL shows the PWM input pulse.

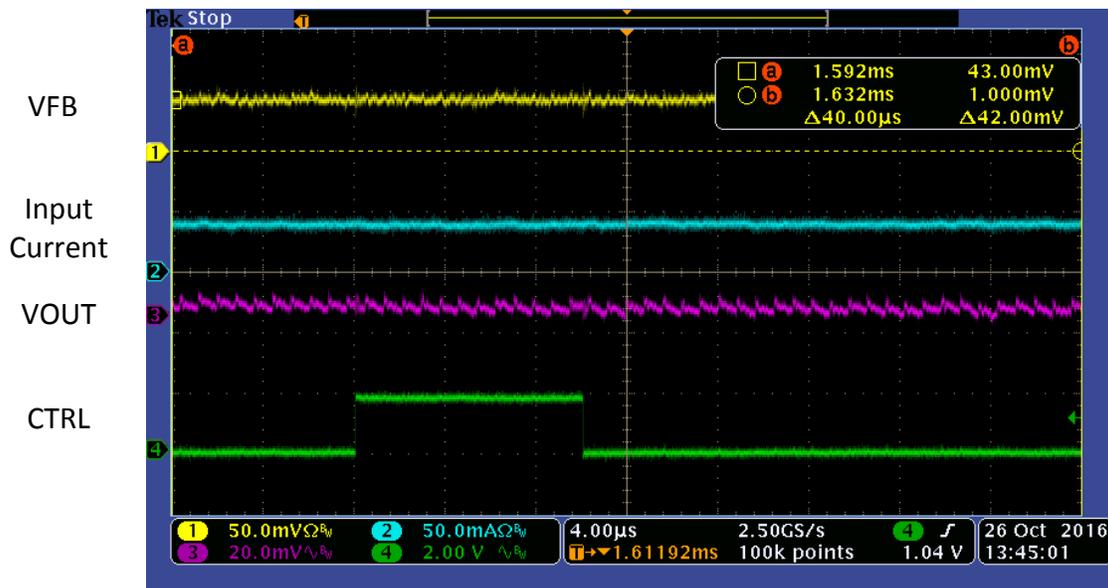


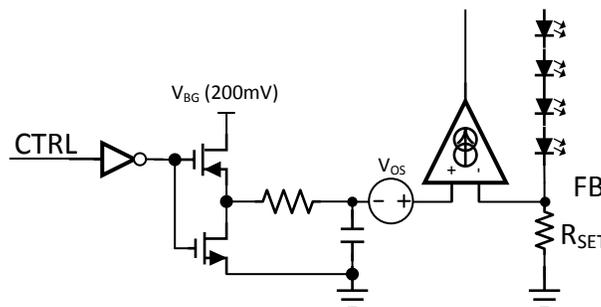
Figure 2. TPS61165 (Low-Pass-Filtered PWM) Waveforms

The main drawbacks to the filtered PWM are:

1. The slow response of the boost output voltage when the PWM duty cycle changes quickly from 0 to 100% duty cycle. This is primarily a result of the boost output voltage needing to slew between different levels due to the change in LED forward voltage.
2. The introduction of offset errors when the filtered reference becomes very small.

Offset errors are the main issue with this type of control. As VREF gets very low (low duty cycle) the offset of the error amplifier becomes a large portion of the reference voltage. To correct this, either trimming must be done, or more complicated offset canceling amplifiers must be implemented. Figure 3 shows the effective block diagram of the offset voltage (V_{OS}) on the LED current set-point. This can be modeled as an offset in the reference voltage at the + input to the error amplifier (V_{OS} can be positive or negative). For positive V_{OS} , this places a minimum LED current that can be achieved when $D = 0$.

Figure 4 shows the response of four white-LED drivers that incorporate a low-pass-filtered PWM input. The TPS61169 is a low-cost device, which shows a lot of low current offset error. The LM3530 is an I2C-controlled device with its PWM input used for CAB control. The TPS61165 and the TPS61158 are simple PWM-only controlled devices that have their offset voltages much better managed. All of these devices have been designed to ensure a positive offset voltage. To allow the ability for 0 duty cycle to force 0 current, these devices incorporate a time-out counter on their PWM input. This counter starts when PWM goes low, and if a rising edge is not seen before the counter times out, the boost is forced off.



$$I_{LED} = V_{FB}/R_{SET} \quad V_{FB} = (V_{BG} \times D + V_{OS})$$

Figure 3. Offset Error in Feedback Voltage

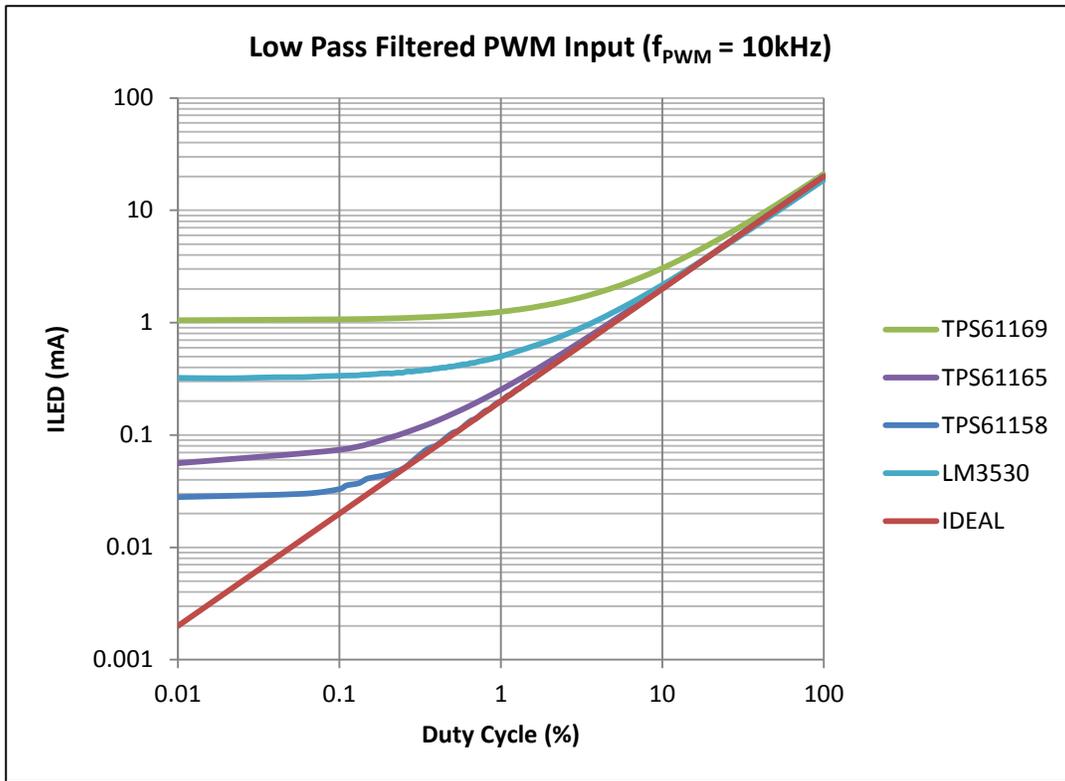


Figure 4. Low-Pass-Filtered Current Response vs Duty Cycle

Table 1 shows a list of TI devices with integrated low-pass filters.

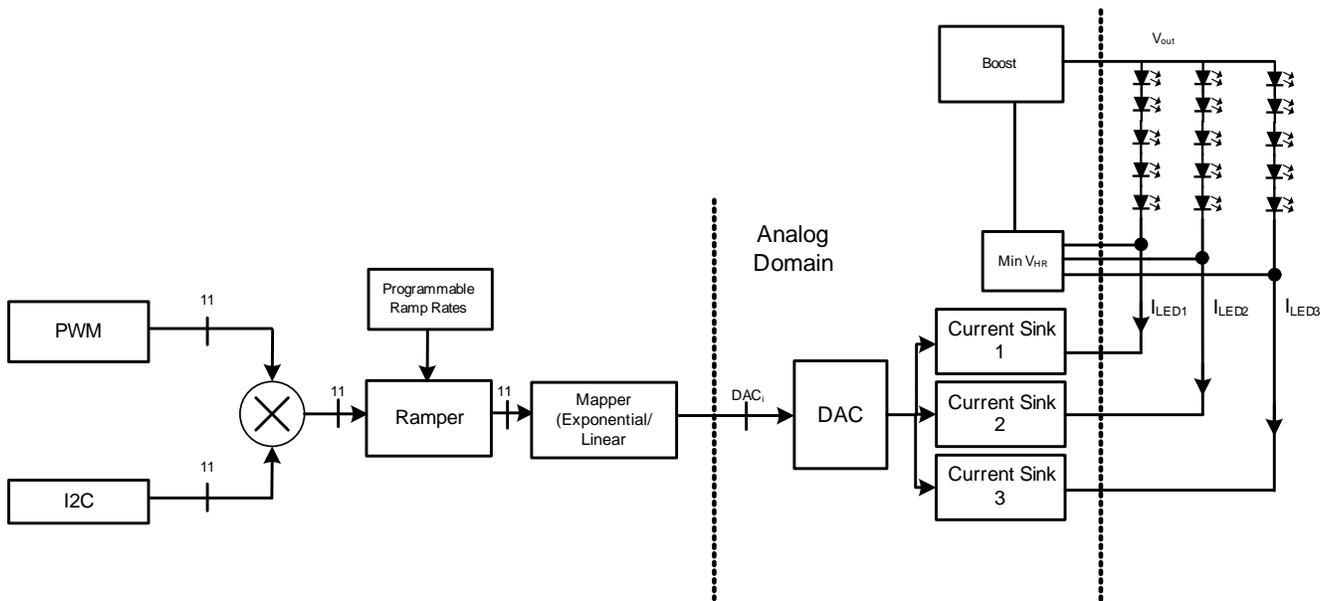
Table 1. White LED Drivers with Low-Pass-Filtered, PWM-to-Analog Dimming

Device	Filter Time Constant	Maximum VOUT	PWM Timeout Counter	Peak Current Limit (min)	RSET or Current Sinks
TPS61169		37.5 V	2.5 ms	1200 mA	RSET
TPS61161	180 μ s	38 V	2.5 ms	560 mA	RSET
TPS61160	180 μ s	26 V	2.5 ms	560 mA	RSET
TPS61158	230 μ s	28.2 V	2.5 ms	500 mA	RSET
TPS61165	180 μ s	38 V	2.5 ms	960 mA	RSET
TPS61162A	180 μ s	26.5 V	20 ms	1000 mA	Dual Current Sinks
TPS61163A	180 μ s	37.5 V	20 ms	1000 mA	Dual Current Sinks
LM3530	330 μ s	41 V	2 ms	739 mA	Single Current Sink
LM3532	295 μ s	41 V	None	880 mA	Triple Current Sink (Dual PWM Input)
LM3533	295 μ s	40 V	None	880 mA	Dual Current Sink
LM3697	295 μ s	40 V	None	880 mA	Triple Current Sink
LM3633	295 μ s	40 V	None	880 mA	Triple Current Sink

2.2 Sampled PWM-to-Analog

An improvement on the low-pass-filtered PWM dimming method is made by moving to a sampled topology. Instead of managing the PWM entirely in the analog domain the PWM input signal is converted to a digital code, and this digital code is applied to an internal DAC. Because this is designed for higher performance LED drivers, this is mainly found on devices with integrated current sinks. Additionally, these devices offer the ability to multiply the PWM input with the I2C duty-cycle code.

Figure 5 shows a typical block diagram of a sampled PWM-to-analog input.



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Figure 5. Sampled PWM-to-Analog Block Diagram

Because the sampled PWM method converts the response to a code, the offset issue is more of an LSB sizing issue than an current offset. This can be seen in Figure 6 where the minimum current is 50 μA (equivalent to code 1 in the 11-bit dimming response of the LM3692x devices). However, time-out counters are included to ensure 0 current at 0 duty cycle.

The main disadvantage to the sampled PWM topology is with the higher quiescent current required to drive the sampler. This is mostly due to the high-frequency oscillator (see Section 2.2.1).

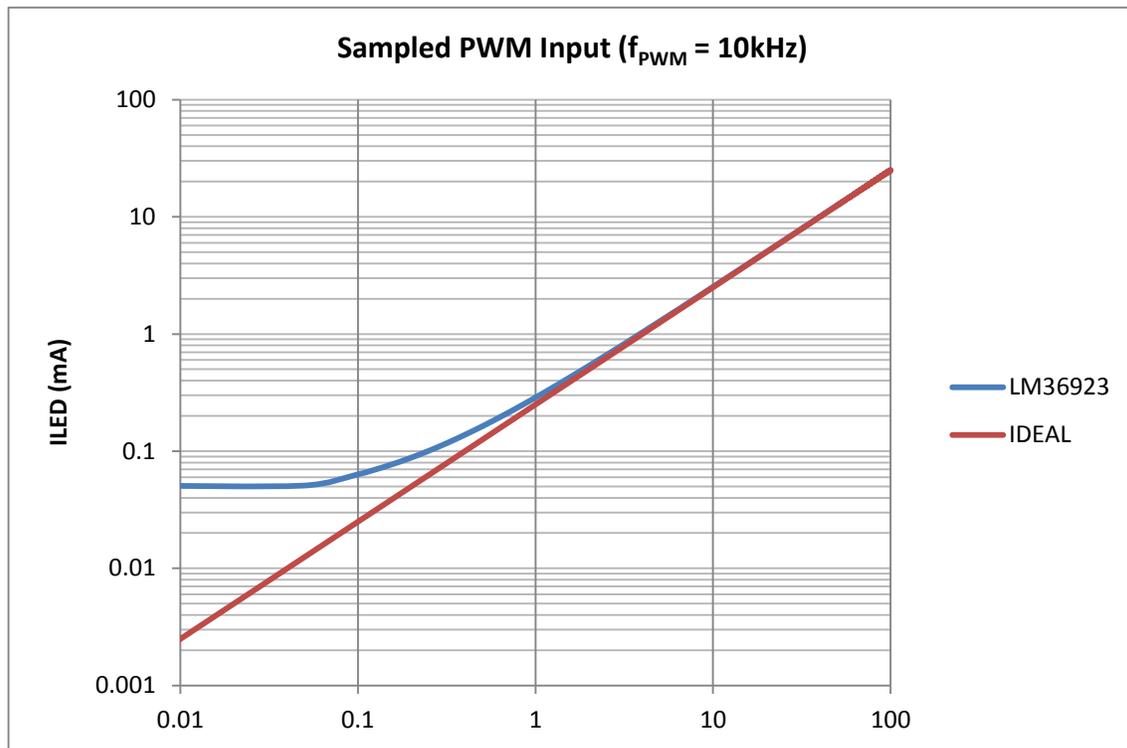


Figure 6. Sampled PWM Current Response vs Duty Cycle

The main advantages of the sampled PWM method (over the LPF) are the following:

1. Allows for mapping the PWM input to an exponential dimming curve (or any other mapping mode available).
2. Allows LED current ramping between duty cycle changes. Using programmable ramping can translate low-resolution PWM duty cycle inputs into higher resolution current ramping.
3. Digital filters (programmable hysteresis) can be used to eliminate jitter in the PWM input that might cause flicker in the LED brightness.
4. Allows for very low frequency PWM inputs. Because the PWM input is converted to a digital code it avoids large low pass filters that would be required for low frequency PWM.
5. Allows a faster response to duty-cycle changes. Because the PWM sample clock is much higher than the PWM input frequency, any change in duty cycle is interpreted within a single PWM period. However, for large deviations in the PWM duty cycle, the slew of the LED voltage can become the bottleneck.

Table 2. White LED Drivers With Sampled PWM-to-Analog Dimming

Device	Sample Rate Options	Configuration	V _{OUT} Range	Other Features
LM36922	800 kHz/4 MHz/24 MHz	2 strings	Up to 28 V	None
LM36923	800 kHz/4 MHz/24 MHz	3 strings	Up to 28 V	None
LM36922H	800 kHz/4 MHz/24 MHz	2 strings	Up to 38 V	None
LM36923H	800 kHz/4 MHz/24 MHz	3 strings	Up to 38 V	None
LM3631	24 MHz	2 strings	Up to 28 V	Integrated LCD bias with programmable turnon
LM36272	1 MHz/4 MHz/24 MHz	2 strings	Up to 28 V	Integrated LCD bias
LM36273	1 MHz/4 MHz/24 MHz	3 strings	Up to 28 V	Integrated LCD bias
LM36274	1 MHz/4 MHz/24 MHz	4 strings	Up to 28 V	Integrated LCD bias

2.2.1 Programmable Sample Rate

The PWM sampler can require high frequency oscillators, depending on the PWM input frequency and resolution required, which can result in high quiescent current. Having a programmable sample frequency can help better fit the sample clock to the input PWM frequency and thus save on quiescent power. [Table 2](#) lists some of the LED driver parts with a sampled PWM input to an analog LED current.

[Figure 7](#) shows the useful PWM input frequency and resolution achievable for the 3 different sample rate options in the LM3692x family of white LED drivers. These curves are generated from the following ($\text{MAX Resolution} = \text{LN}(f_{\text{SAMPLE}}/f_{\text{PWM}})/\text{LN}(2)$). The devices in [Table 2](#) all have a maximum resolution of 11 bits. Additionally, the PWM timeout counter is adjusted depending on the sample rate, so this gives a minimum achievable PWM input frequency based on sample rate options.

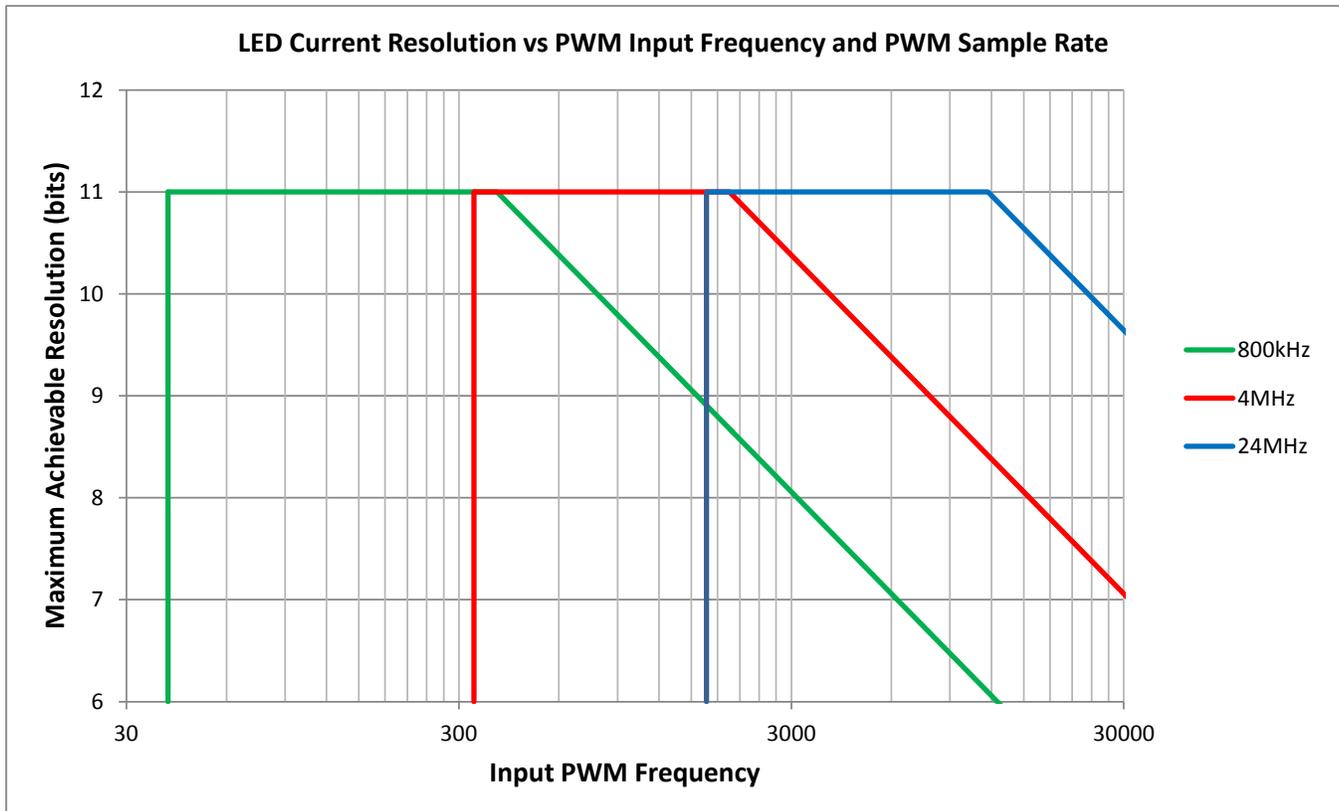


Figure 7. PWM Sample Rate Options (LM36923x Devices)

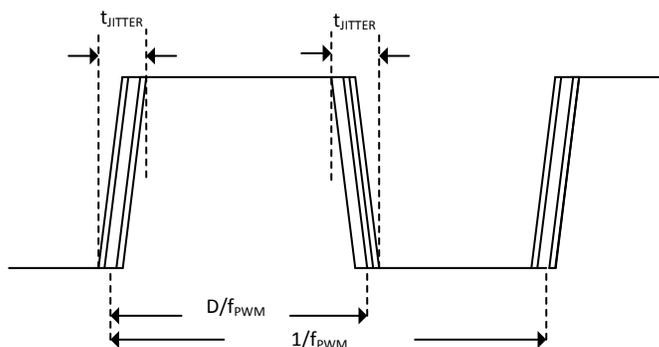
[Table 3](#) shows the sample rate options/PWM timeout, and the corresponding increase in quiescent current for each sample rate option.

Table 3. Programmable Sample Frequencies (LM3692x Devices)

PWM Sample Rate	Input Quiescent Current (mA) For PWM Sampler	Frequency Range for 11-Bit Resolution	PWM Timeout	f_{PWM} Minimum
800 kHz	30 μA	$f_{\text{PWM}} < 400 \text{ Hz}$	25 ms	48 Hz
4 MHz	50 μA	$f_{\text{PWM}} < 2 \text{ KHz}$	3 ms	400 Hz
24 MHz	350 μA	$f_{\text{PWM}} < 12 \text{ kHz}$	600 μs	2 kHz

2.2.2 PWM Hysteresis

Another benefit of the sampled PWM input is the ability to program the hysteresis. Hysteresis helps filter out jitter in the PWM input that could cause LED flicker (predominately at light currents). Jitter causes a time varying PWM frequency that could result in a time varying duty cycle. If the duty cycle variation is large and slow enough, this could appear as flicker at the LED output. Hysteresis works by controlling the amount of change in the LED current in response to a direction change in the PWM input duty cycle. This means that for successive increases or successive decreases in duty cycle, the LED current changes at the minimum step size. However, if the duty cycle had been increasing and then turned and began decreasing, the initial change in duty cycle in the decreasing direction would have to overcome the hysteresis before the LED current is allowed to change. This effectively prevents the PWM jitter from being passed through to the LED current by keeping the LED current from changing in the opposite direction from the previous change, until the hysteresis is overcome.



1. The amount of hysteresis needed depends on the amount of variation in the PWM period t_{JITTER}
2. Because hysteresis is in terms of 11 bit LSBs, the hysteresis setting would be given as: $\text{Hysteresis Setting} > \text{LN}(t_{JITTER} \times f_{PWM} \times 2048) / \text{LN}(2)$

Figure 8. Determining PWM Hysteresis Based on Jitter

For the devices listed in [Table 2](#) the programmable hysteresis is set in increments of LSBs. [Table 4](#) shows the hysteresis options in the LM36922/23/22H/23H.

Table 4. Programmable Hysteresis Options (LM3692x Devices)

Hysteresis Setting	Minimum Duty cycle change required to overcome hysteresis ($2^{\text{HYST}}/2047$)
0 LSB (no hysteresis)	0.0489%
1 LSB	0.0978%
2 LSB	0.195%
3 LSB	0.39%
4 LSB	0.781%
5 LSB	1.56%
6 LSB	3.13%

For example, if 3 LSBs are selected for the hysteresis, then when the duty cycle direction changes, it must change greater than ($2^3/2047 = 0.781\%$) for the LED current to also change. Once the initial change is overcome then subsequent changes (in the same direction) can then change at a single LSB ($1/2047 = 0.0489\%$).

2.2.3 Re-Mapping the PWM Response

Having the PWM input converted to a digital code allows the ability to re-map the input duty cycle to a different current mapping. Typically duty cycle has a linear response from D to ILED. However, when the PWM input is converted to a digital code, the code can then be re-mapped to an exponential changing current. An exponential response is beneficial because it compensates for the logarithmic response of the eye (the eye perceives an exponential change as linear). [Figure 9](#) shows the ILED vs duty cycle for the exponential mapped current compared to typical linear mapped current. The exponential mapped current changes by 0.3% per 1/2047 change in PWM duty cycle. All devices in [Table 2](#) have the ability to re-map the PWM input duty cycle to an exponential current.

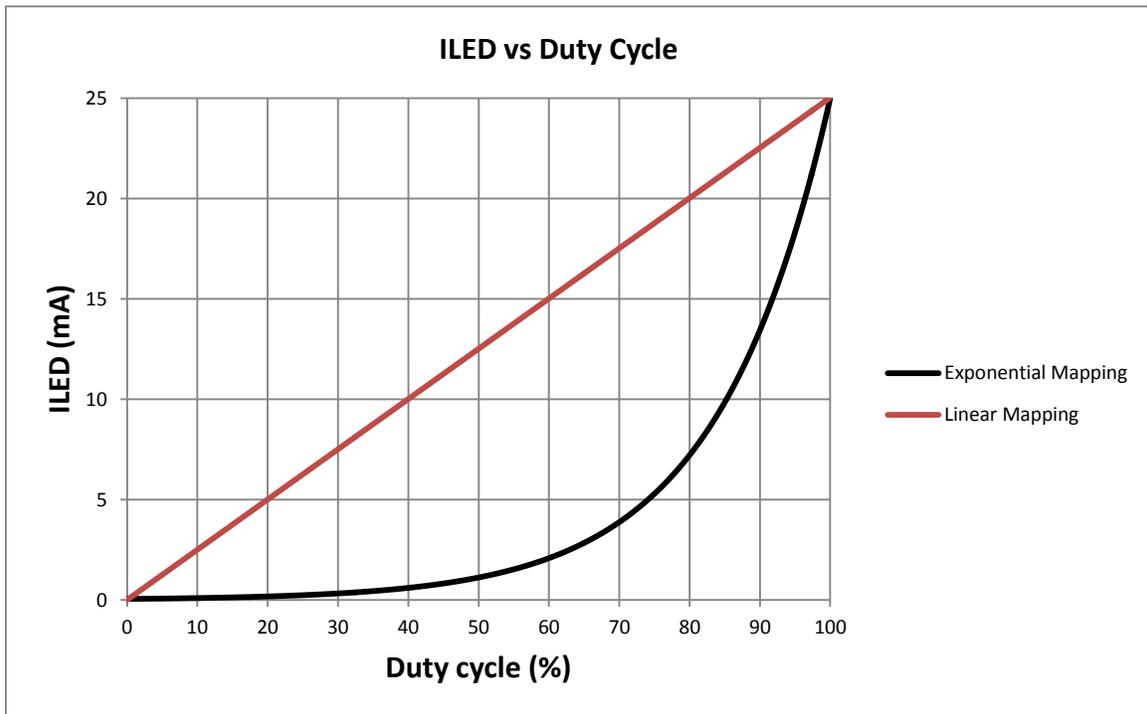
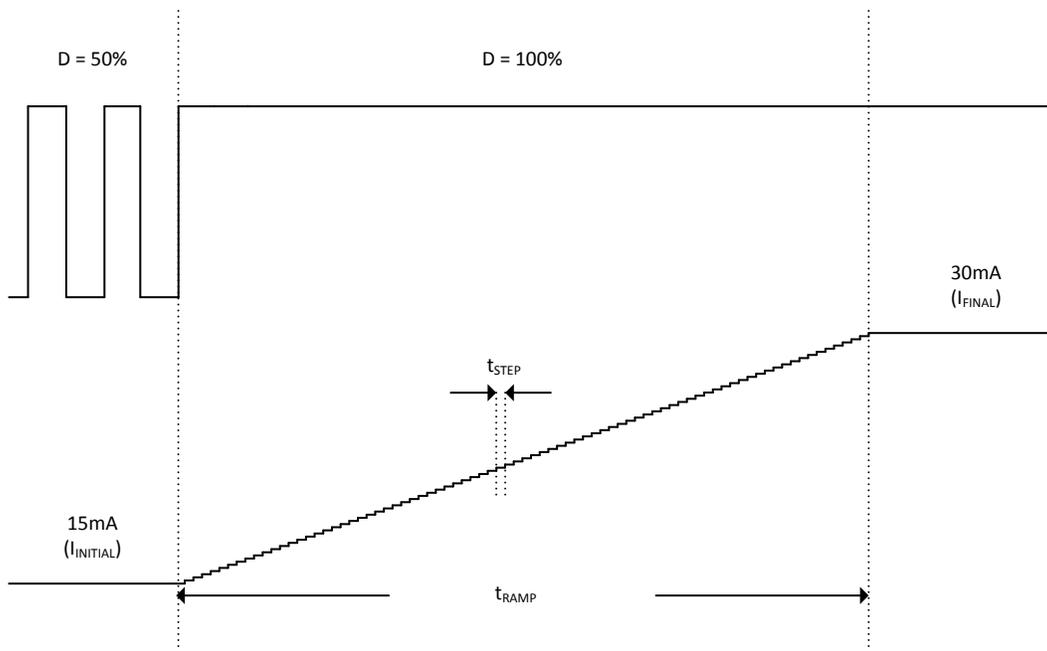


Figure 9. LED Current-Mapping-Mode Options

2.2.4 Automatic Current Ramping

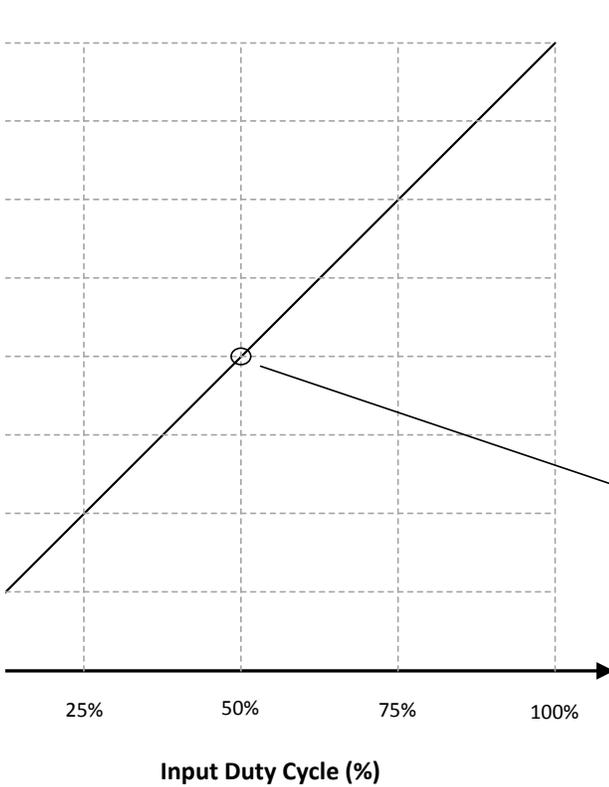
Once the PWM input is converted to a digital code, the code can be applied to any preset internal current ramps. [Table 5](#) shows the ramp options available in some devices with sampled PWM inputs. These ramps have two main benefits. First, automatic ramping provides a controlled turnon and turnoff without the need to manage the PWM duty cycle ramp. Second, automatic ramping steps through the brightness codes independent of the resolution of the PWM input. This allows for low resolution input duty cycle (or step change in input duty cycle) to give a high resolution LED current response. An example would be a system with a low resolution duty cycle (that is, 32 levels). When the duty cycle changes, for example from 50% to 100%, and ramping is enabled, the LED current increments at the programmed ramp rate, through each available current setting, until the end duty cycle is reached (see [Figure 10](#)). This would effectively increase the 32-level PWM input to a 2047-level current ramp. For some devices the ramping can be set as a time per code, and some devices have this ramp given as a fixed time between codes.

[Figure 11](#) shows the effect of an 8-bit PWM input being gained up to an 11-bit linear and an 11-bit exponential mapping.



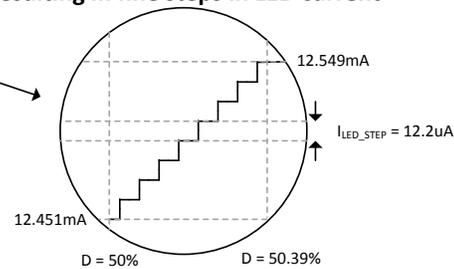
1. For devices with fixed time ramping, t_{RAMP} is the programmed ramp time independent of the number of code changes between endpoints
2. For devices with time per step ramping, t_{RAMP} is equal to # Codes between I_{FINAL} and $I_{INITIAL}$ multiplied by the programmed time per step

Figure 10. LED Current Ramping With Duty Cycle Changes

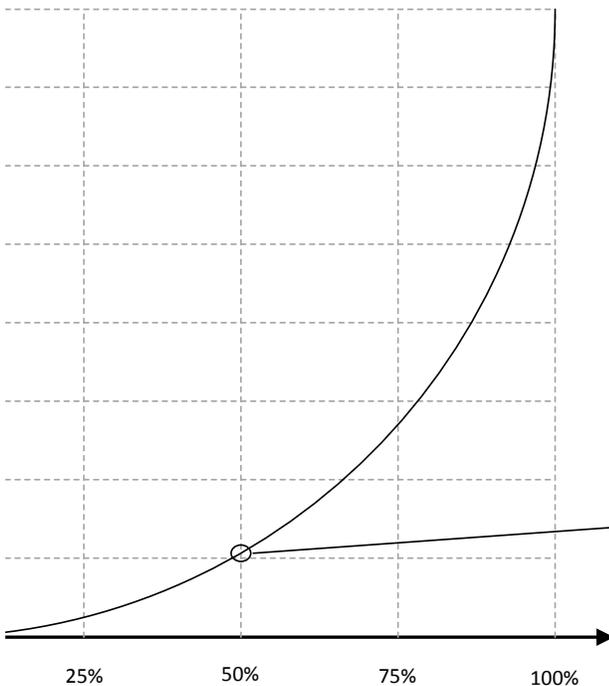


1. With Linear Mapping Selected, Ramping from one current to the next is 11 bit ($I_{LED_STEP} = I_{LED_MAX}/2047$), or 12.21uA/step (assuming 25mA max current).
2. This would increase an 8 bit input duty cycle resolt to an 11 bit LED current resolution (8x increase in resolu when ramping between duty cycle changes).

Zoom In on an 8 bit step in duty cycle resulting in fine steps in LED current



1. With Exponential Mapping Selected, Ramping from the next has 11 bits of resolution, but each LED current ch codes is ($I_{LED_STEP} = 0.3\%$). This results in a minimum curre 152nA (between code 1 and code 2).
2. This would effectively increase a linear 8 bit input di 11 bit exponential current when ramping between duty c An increase in resolution by as much as 645x



Zoom In on an 8 bit step in duty cycle resulting in very fine steps in LED current

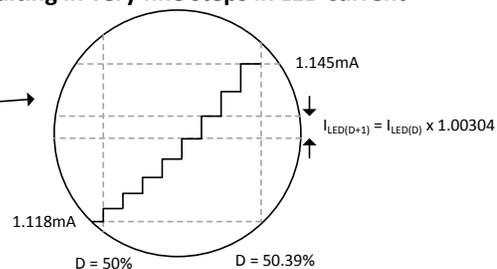


Figure 11. Increasing PWM Resolution With Automatic Ramping

Table 5. Devices With Ramping Between PWM Duty Cycle Changes

LM36922/23 (Time per Step)	LM36272/3/4 (Fixed Time)
0	0
125 μ s/ 11 bit LSB	500 μ s
250 μ s/11 bit LSB	750 μ s
500 μ s/11 bit LSB	1 ms
1 ms/11 bit LSB	2 ms
2 ms/11 bit LSB	5 ms
4 ms/11 bit LSB	10 ms
8 ms/11 bit LSB	20 ms
16 ms/11 bit LSB	50 ms
	100 ms
	250 ms
	800 ms
	1 s
	2 s
	4 s
	8 s

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