Application Note

Designing an Isolated Buck (Fly-Buck™) Converter using the LMR36520

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ABSTRACT

The purpose of this application note is to lead the reader through the design of an isolated buck also known as a Fly-Buck™ converter using the LMR36520 from Texas Instruments. This application note will describe the typical operation of a Fly-Buck™ converter from a theoretical perspective, and then walk through the process of Fly-Buck™ converter design from a set of given operating conditions using design equations derived in referenced reports. Physical measurements will be compared to expected results, and design limitations will also be discussed.

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1 Introduction

Many applications require various power rails to supply power to different devices within a system. It is not uncommon for these different power rails to each have differing load requirements. Some rails may need to be very tightly regulated, offering a minimum of peak-to-peak variation to meet their respective load requirement. Some rails on the other hand, can power loads that are more robust to variations on the input supply and, therefore, do not require such tight regulation.

Rather than having a different DC/DC regulator for each different power line, some systems can benefit from using a single IC to produce multiple power rails. The Flyback topology offers the possibility of producing multiple power lines from a single input, but that comes with a cost of using more complex control circuitry to regulate the secondary. This is where the isolated buck, or Fly-Buck™ converter, comes in. The Fly-Buck™ converter is a modification to the standard buck converter topology that replaces the standard inductor with a coupled inductor or transformer to produce one or multiple isolated secondary outputs.

The Fly-Buck™ converter topology is beneficial because it produces a tightly regulated primary output, along with one or multiple electrically isolated secondary outputs without the need of using an optocoupler to regulate the secondary. This means that the design of a Fly-Buck™ converter is relatively straight forward and can be done similarly to the design of a typical buck converter with some minor variations.

This application note will detail the process of designing a Fly-Buck™ converter using the LMR36520.
The LMR36520 is a 4.2-V to 65-V 2-A synchronous buck converter that is well-suited for industrial power applications. The HSOIC-8 package can handle PCB strain better than other leadless packages and also makes debugging in the field much easier by enabling visual inspection of the device leads. Internal compensation reduces external component count and simplifies pinout making the LMR36520 ideal for Fly-Buck™ converter applications.

2 Fly-Buck™ Converter Device Operation

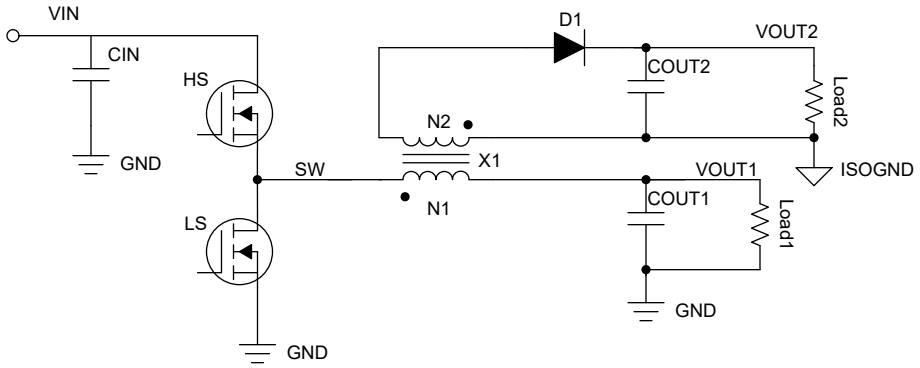

Figure 2-1. General Fly-Buck™ Converter Circuit Diagram

The simplest definition of a Fly-Buck™ converter is a synchronous buck converter with the inductor replaced by a coupled inductor and an isolated secondary output. The primary side output is still regulated just like a typical buck converter, and the ideal transfer function from input to primary output is:

$$V_{out1} = \frac{t_{on}}{t_{on} + t_{off}} \times V_{in} = D \times V_{in} \quad (1)$$

The secondary winding of the coupled inductor acts as the source for the secondary output which in its simplest form consists of a rectifier diode and an output capacitor. More components can be added to the secondary output to optimize its performance. See *Section 3* for more details. The combination of the rectifying diode and secondary output capacitor provide a DC output voltage to the secondary load determined by Equation 2:

$$V_{out2} = \left(V_{out1} \times \frac{N_2}{N_1}\right) - V_f \quad (2)$$

The coupled inductor or transformer provides electrical isolation between primary and secondary outputs, essentially making the secondary float with respect to the primary. Electrical isolation ensures that users are protected from dangerously high voltages which may be present on the input to the device. It is important to note that the secondary output voltage can be either positive or negative with reference to the isolated ground simply by changing the isolated ground location. This is illustrated in Figure 2-2.

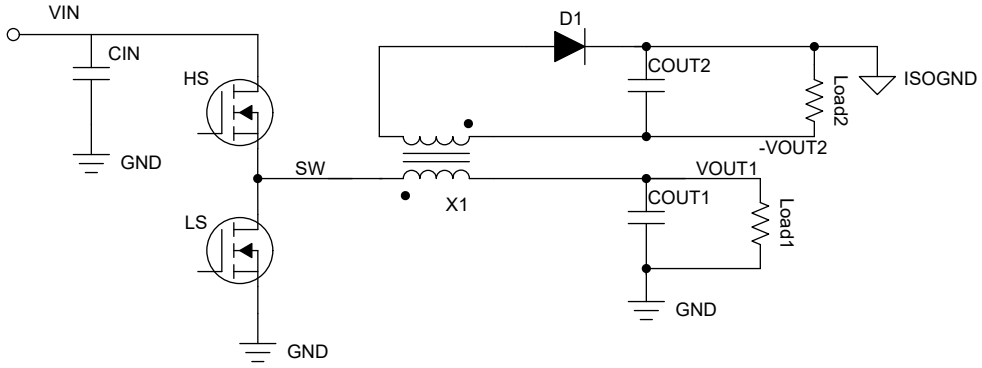

Figure 2-2. Fly-Buck™ Converter with Inverting Secondary

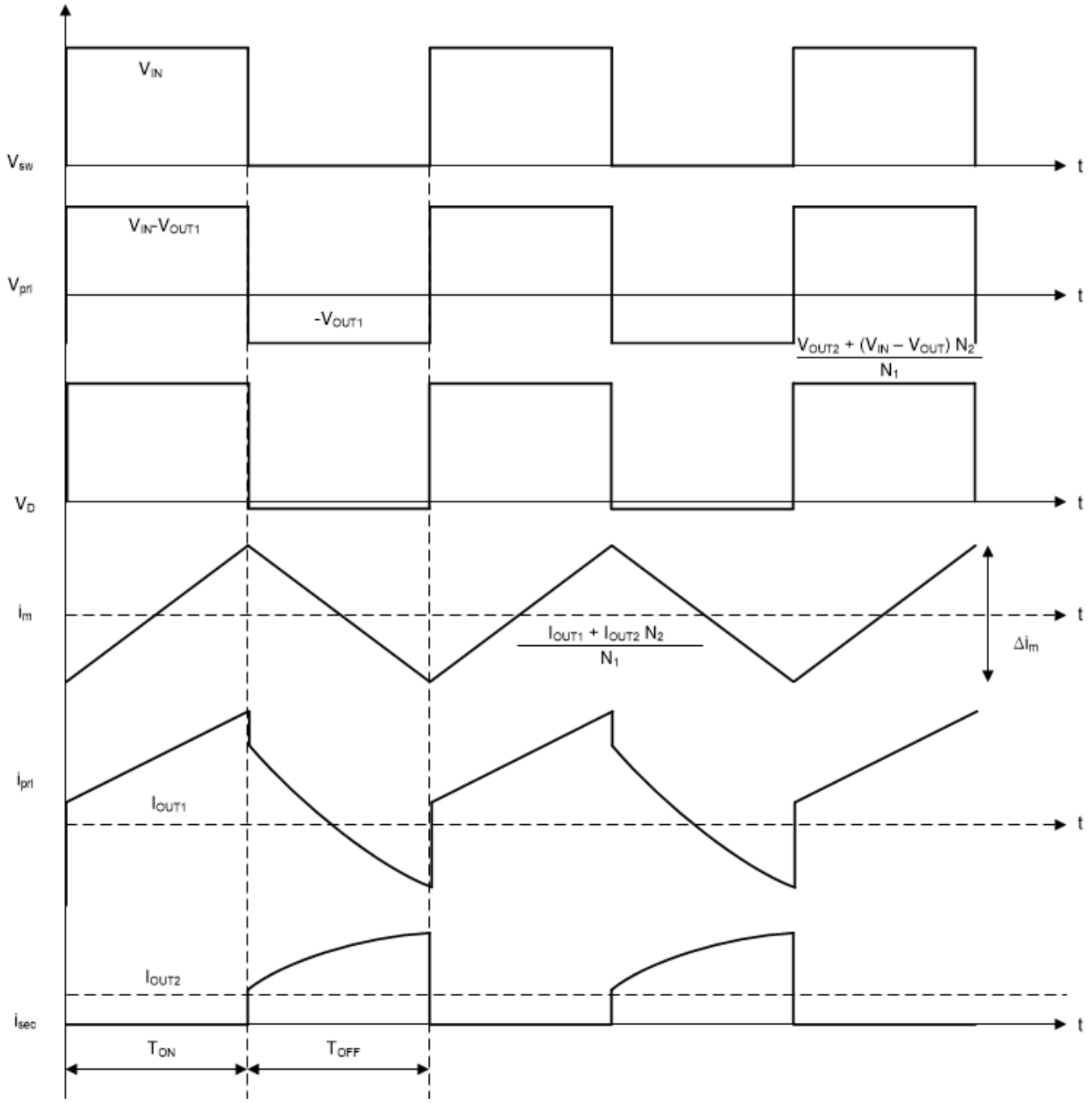

Figure 2-3. Fly-Buck™ Converter Steady State Waveforms

Figure 2-3 shows the typical steady state waveforms expected of a Fly-Buck™ converter. During the ON-time, the HS or high-side MOSFET is ON and ideally looks like a short circuit. This means that the SW node voltage is equal to the input voltage and the voltage across the primary side of the coupled inductor is $V_L = V_{IN} - V_{OUT}$. Since this is a buck converter, $V_{IN} > V_{OUT}$ so V_L is positive during the on-time. The voltage induced across the secondary winding is:

$$V_{L2} = V_{L1} \times \left(\frac{N_2}{N_1}\right) \quad (3)$$

Following the dot convention, the voltage at the dotted terminal of the secondary winding is positive because current enters the dotted terminal of the primary winding. This means that the rectifying diode is therefore reverse biased since the voltage seen at its anode is negative with respect to the isolated ground, and current

is supplied to the secondary load by the output capacitor. This reverse bias voltage across the diode during the on-time is given by:

$$V_D = V_{out2} + \left(\frac{N_2}{N_1}\right) \times (V_{in} - V_{out1}) \quad (4)$$

During the off-time, the SW node voltage is pulled down to GND potential due to the LS or low-side MOSFET conducting. The resulting primary winding voltage is:

$$V_{L1} = -V_{out1} \quad (5)$$

Following the same procedure as during the ON time, the voltage induced across the secondary winding is now negative at the dotted terminal, which results in the rectifier diode being forward biased. The secondary winding now acts as a current source, as it transfers energy from the primary side to the secondary load. Similar to what happens in normal buck operation, the DC portion of this current is provided to the secondary load while the AC portion of the current charges the secondary output capacitor.

2.1 Output Current Equations and Considerations

The magnetizing current waveform is identical to the typical triangular inductor current waveform that is familiar to typical buck converter operation. For the case of a coupled inductor with a single secondary winding, this magnetizing current can be written as:

$$I_m = I_{L1} + \left[I_{L2} \times \left(\frac{N_2}{N_1}\right)\right] \quad (6)$$

The magnetizing current equation can be expanded for the case of a multi-winding transformer but will not be discussed in this report. The *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter* application report provides more information on this.

On a cycle-by-cycle average, the winding currents can be related to the output currents as follows:

$$I_{out1} = I_{L1} \quad (7)$$

$$I_{out2} = I_{L2} \quad (8)$$

Since the magnetizing current is the same as the typical buck inductor current waveform, you can calculate the peak-to-peak current ripple the same way using Equation 9:

$$\Delta i_m = \frac{[(V_{in} - V_{out1}) \times t_{on}]}{L_{pri}} = \frac{[(V_{in} - V_{out1}) \times D]}{L_{pri} \times f_{sw}} \quad (9)$$

This peak-to-peak magnetizing current ripple is useful for estimating the peak current through both the high-side and low-side FETs. The peak current through the primary winding is given by Equation 10:

$$I_{pri\_pospk} = I_{out1} + \left[\left(\frac{N_2}{N_1}\right) \times I_{out2}\right] + \left(\frac{\Delta i_m}{2}\right) \quad (10)$$

The peak negative current through the primary winding can be approximated by Equation 11:

$$I_{pri\_negpk} = -\left[\left(\frac{N_2}{N_1}\right) \times I_{out2} \times \left(\frac{2D}{1-D}\right)\right] - \left(\frac{\Delta i_m}{2}\right) + I_{out1} \quad (11)$$

Equation 10 and Equation 11 are extremely important in determining whether an IC will work as a Fly-Buck™ converter in a given application. This is because the peak HS current limit of the device and the peak negative (also known as sink) current limit of a device cannot be exceeded in order for the device to properly regulate the output. This can be written mathematically as:

$$I_{pri\_pospk} \leq I_{SC} \quad (12)$$

$$|I_{pri\_negpk}| \leq |I_{L\_NEG}| \quad (13)$$

Leakage inductance and duty cycle are also critical factors in Fly-Buck™ converter operation. Real world transformers and coupled inductors have some amount of leakage inductance arising from magnetic flux that is not shared between both the coils. In practice, this leakage flux affects the power output of the secondary side by limiting the rate at which the secondary side current can ramp up. For cases of higher leakage inductance, the ramp rate of the current in the secondary side is reduced compared to that of a lower leakage case. This means that a longer amount of time is required for the same amount of energy to be transferred from primary to secondary. For a fixed frequency part, this requires that a lower maximum duty cycle be chosen to ensure that there is enough off-time for energy to be transferred from primary to secondary. By convention, the maximum duty cycle for a Fly-Buck™ converter is held to 50%, larger duty cycles would result in less off-time which would result in larger negative peak currents being reflected to the primary side. Leakage inductance should therefore be minimized to ensure the widest duty cycle range possible.

3 LMR36520 Fly-Buck™ Converter Design

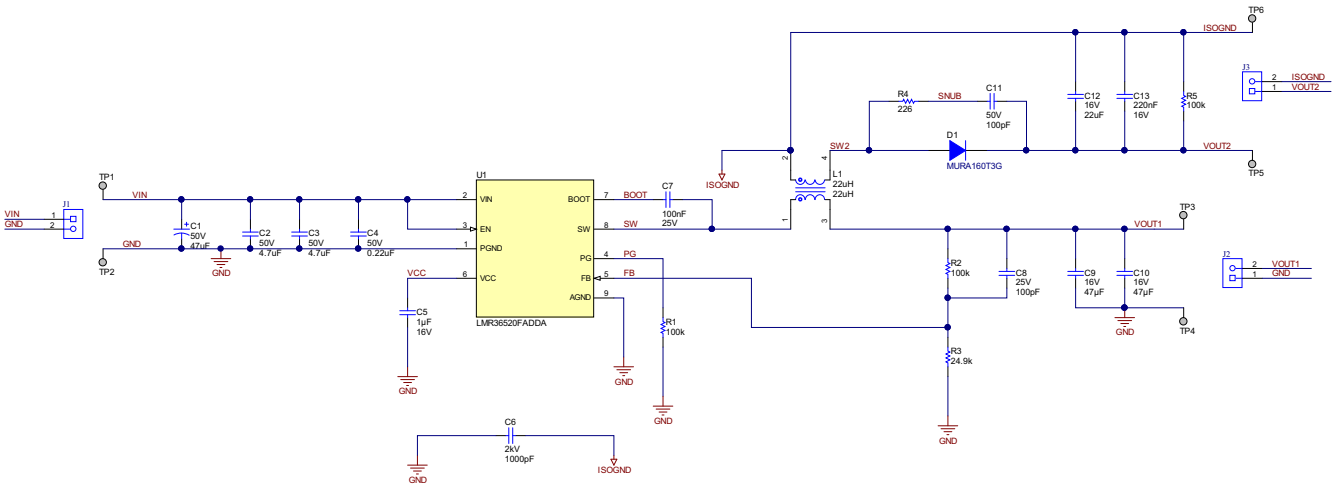

Figure 3-1. Fly-Buck™ Converter Schematic

Table 3-1. Fly-Buck™ Converter Design Input and Output Parameters

V_{IN} minimum	10 V
V_{IN} maximum	36 V
V_{out1}	5 V
I_{out1}	500 mA
V_{out2}	3.3 V
I_{out2}	500 mA
Switching frequency	400 kHz

In order to operate as a Fly-Buck™ converter, an IC that offers Forced Pulse Width Modulation (FPWM) must be selected to ensure that the part can handle negative inductor current. In this case, the LMR36520FADDA is selected for this reason.

The LMR36520 data sheet should be consulted for recommended values and equations for components such as input capacitor, feedback resistors, EMI filter, feedforward capacitor, C_{VCC}, and bootstrap capacitor. The following design example will focus on calculating component values for Fly-Buck™ converter components specifically.

3.1 Coupled Inductor

Once the above input and output parameters are known, the first thing to do is to select an appropriately-sized coupled inductor or transformer by first finding the turns ratio required to generate the desired secondary output voltage. From there, the critical inductance can be calculated the same way as for a typical non-isolated buck converter.

Two windings will be needed to establish the two output voltages. The secondary output voltage can be described by applying Kirchoff's voltage law around the secondary loop:

$$V_{out2} = V_{out1} \times \left(\frac{N_2}{N_1}\right) - V_f \tag{14}$$

$$3.3\ V = 5\ V \times \left(\frac{N_2}{N_1}\right) - V_f \tag{15}$$

By targeting a diode forward voltage drop (Vf) of 1 V, the ratio of N2/N1 comes to be 0.86. The closest whole number ratio is 1:1, therefore, a coupled inductor is selected. This will result in the secondary output voltage being slightly greater than 3.3 V. To address this, a series connected Zener diode and resistor can be placed in parallel with the secondary load to clamp the output to 3.3 V.

Because the magnetizing inductance current waveform is the same as that of the inductor current waveform for a typical inductor, the primary winding inductance can be calculated using the same methodology.

$$L_{pri} = V_L\left(\frac{\Delta t}{\Delta i}\right) \tag{16}$$

The Δi term in Equation 16 represents the peak-to-peak magnetizing current ripple and is typically set around 30% to 40% of the magnetizing current supplied by the converter which is 1 A in this case.

Setting Δi = 0.4 A then yields:

$$L_{pri} = (36\ V - 5\ V)\left(\frac{\frac{5\ V}{36\ V}}{0.4 \times 400000\ Hz}\right) = 26.9\ \mu H \tag{17}$$

This Δi term can be adjusted to be higher or lower based on the needs of the application. The selected Δi term can work as long as the primary winding current does not exceed either the high-side current limit or the negative current limit. The calculated L_{pri} in this case is not a typical nominal inductance value so a 22-µH coupled inductor is selected instead resulting in the following peak-to-peak magnetizing current ripple:

$$\Delta i_m = \frac{[(V_{in} - V_{out1}) \times D]}{L_{pri} \times f_{sw}} = \frac{\left[(36\ V - 5\ V) \times \left(\frac{5\ V}{36\ V}\right)\right]}{22\ uH \times 400000\ Hz} = 0.489\ A \tag{18}$$

Now to ensure this magnetizing ripple current does not violate our peak current conditions:

$$I_{pri\_pospk} = I_{out1} + \left[\left(\frac{N_2}{N_1}\right) \times I_{out2}\right] + \left(\frac{\Delta i_m}{2}\right) = 0.5\ A + \left[\left(\frac{1}{1}\right) \times 0.5\ A\right] + \left(\frac{0.489\ A}{2}\right) = 1.244\ A \tag{19}$$

$$I_{pri\_negpk} = -1 \times 0.5^{*}\left(\frac{2 \times 0.5}{1 - 0.5}\right) - \left(\frac{0.489\ A}{2}\right) + 0.5\ A = -0.744\ A \tag{20}$$

The minimum LMR36520 HS current limit is 2.4 A, while the negative current limit is -1.7 A according to the data sheet. Slight variations occur between chip-to-chip which is why it is important to use the minimum HS current limit when evaluating this condition to ensure that the limit is not violated under worst case conditions.

The selected 22-µH coupled inductor is, therefore, adequate to ensure that the peak current limits are not violated. This inductor should also have a saturation current rating that is at least as large as the maximum short circuit current limit of the device. Here, the maximum short circuit current limit is used to ensure the limit is not violated under worst case conditions as previously discussed.

3.2 Primary Output Capacitor

The primary output capacitor determines the amount of output voltage ripple and load transient performance that the regulator can achieve on its primary output. Equation 21, Equation 22, Equation 23 and can be used to estimate the lower bound of the output capacitance and upper bound of the capacitor ESR.

$$C_{out} \geq \frac{\Delta I_{out}}{f_{sw} \times \Delta V_{out} \times K} \times \left[(1 - D) \times (1 + K) + \frac{K^2}{12} \times \left(2 - D\right)\right] \tag{21}$$

$$ESR \leq \frac{(2 + K) \times \Delta V_{out}}{2 \times \Delta I_{out}\left[1 + K + \frac{K^2}{12} \times \left(1 + \frac{1}{(1 - D)}\right)\right]} \tag{22}$$

$$D = \frac{V_{out}}{V_{in}} \tag{23}$$

where

- ΔV_{out} = output voltage transient
- ΔI_{out} = output current transient
- K = ripple factor

Although not specified in Table 3-1, let ΔI_{out} = 0.5 A and ΔV_{out} = 20 mV, while K ≅ 0.5 from the previous section. Solving for C_{out} and ESR:

$$C_{out} \geq 97.6\ \mu F \tag{24}$$

$$ESR \leq 32\ m\Omega \tag{25}$$

Selecting two 47-µF multilayer ceramic capacitors to be placed in parallel will result in slightly lower output capacitance than Equation 24 and, therefore, higher output voltage ripple, but this is acceptable for this design.

Using Equation 26 to approximate the output voltage ripple results in:

$$V_r \cong \Delta I_L \times \sqrt{ESR^2 + \frac{1}{(8 \times f_{sw} \times C_{OUT})^2}} \tag{26}$$

$$V_r \cong 0.015\ V_{pk-pk} \tag{27}$$

This expected voltage ripple in Equation 27 is less than 1% of the desired output voltage so this is acceptable for most applications.

To reduce high frequency noise on the primary output, an additional high frequency capacitor of around 100 nF can also be placed at the output.

All of the primary output capacitors should have a voltage rating greater than that of the desired output voltage and may have to be rated higher in order to account for de-rating associated with DC bias and temperature. Consult the capacitor data sheet to ensure output capacitance does not significantly de-rate at the desired output voltage and temperature conditions. A voltage rating of 16 V to 25 V is appropriate for this application.

The RMS current rating of the primary output capacitor is another important parameter that must be met in order to ensure proper operation. The figure below shows the straight line approximations of the AC current waveforms through the primary and secondary output capacitors. The RMS values of these current waveforms can be estimated using the piecewise linear approximation method which is detailed below.

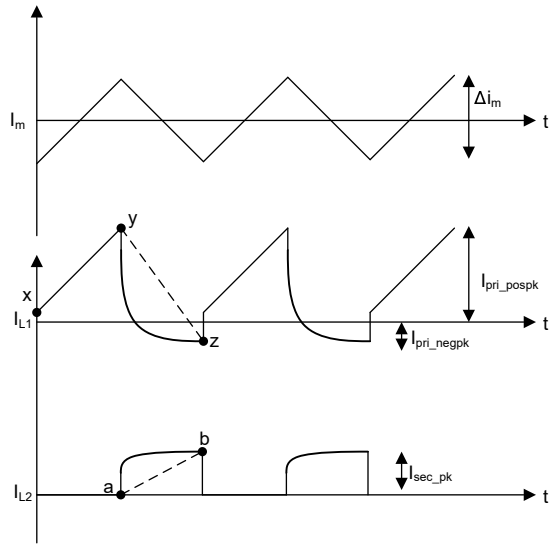

Figure 3-2. Straight Line Approximation of AC Current Through Output Capacitors

$$i_{pri\_cout\_rms} = \sqrt{\frac{y^2 + x^2 + x*y}{3} \times \left(\frac{t_{on}}{T}\right) \times \frac{x^2 + z^2 + x*z}{3} \times \left(\frac{t_{off}}{T}\right)} \tag{28}$$

$$x = I_{pri\_pospk} = 1.244\ A \tag{29}$$

$$y = I_{out1} - \frac{\Delta i_m}{2} = 0.256\ A \tag{30}$$

$$z = I_{pri\_negpk} - I_{out1} = -1.244\ A \tag{31}$$

$$i_{pri\_cout\_rms} = 0.761\ A_{rms} \tag{32}$$

Equation 32 represents the AC current that will be split amongst the primary output capacitors. Therefore, the two 47-µF ceramic capacitors selected for the primary output capacitor bank are expected to have about 380 mA_{rms} current through them and should be rated higher than this.

3.3 Rectifying Diode

The rectifying diode must be rated to handle the reverse bias voltage during the on-time as well as the secondary load current.

The reverse voltage across the diode during the off-time is:

$$V_D = V_{out2} + \left(\frac{N_2}{N_1}\right) \times (V_{in} - V_{out1}) = 3.3\ V + \left(\frac{1}{1}\right) \times (36\ V - 5\ V) = 34.3\ V \tag{33}$$

The forward voltage drop across the diode when it is conducting is also important to consider as it limits the maximum secondary output voltage. Neglecting conduction losses associated with the DCR of the inductor, in order to achieve 3.3 V at the secondary output, the forward voltage drop across the diode when it is fully conducting should be:

$$V_f = \left(\frac{N_2}{N_1}\right) \times V_{out1} - V_{out2} = \left[\left(\frac{1}{1}\right) \times 5\ V\right] - 3.3\ V = 1.7\ V \tag{34}$$

The MURA160 ultra-fast rectifying diode is chosen because of its 1-V forward voltage drop at 500 mA and low junction capacitance. Schottky diodes are commonly used as the secondary rectifier diode due to their low forward voltage drop and fast reverse recovery time. Because this application calls for a higher forward voltage drop to achieve the desired secondary output voltage, the ultra-fast rectifier diode is preferred.

Another easily overlooked yet important parameter is the diode junction capacitance. This junction capacitance forms a resonant LC tank with the leakage inductance from the secondary winding of the coupled inductor which causes high frequency ringing to occur on the switch node when the high-side MOSFET changes state from OFF to ON. This is another reason why an ultra-fast rectifier diode is chosen instead of the typical Schottky diode for this application. The smaller junction capacitance of the ultra-fast diode results in smaller peak overshoot and higher resonant frequency making it easier to filter. This ringing can be mitigated with a simple RC snubber in parallel with the diode. See *Section 3.7* for more information.

3.4 Secondary Output Capacitor

The secondary output capacitor must be able to supply the secondary load current during the on-time of the converter. To calculate the minimum capacitance required, use Equation 35:

$$C_{out2} = \frac{I_{out2} \times D_{max}}{f_{sw} \times \Delta V_{out2}} = \frac{0.5\ A \times 0.5}{400000\ Hz \times 0.033\ V} = 17.8\ uF \tag{35}$$

A 22-µF capacitor rated at 16 V is selected to account for de-rating. An additional 220-nF, high-frequency capacitor rated at 10 V is also selected to reduce high frequency noise on the secondary output.

Once again, the piecewise linear method is used to approximate the rms current through the secondary output capacitor bank in order to determine the rms current ratings of these components.

$$i_{cout2\_rms} = \sqrt{\frac{a^2 + b^2 + a \times b}{3} \times \left(\frac{t_{off}}{T}\right) + \frac{a^2 + a^2 + a \times a}{3} \times \left(\frac{t_{on}}{T}\right)} \tag{36}$$

$$a = -I_{out2} = -0.5\ A \tag{37}$$

$$b = I_{sec\_pk} - I_{out2} = 1.5\ A - 0.5\ A = 1\ A \tag{38}$$

$$i_{cout2\_rms} = 0.645\ A_{rms} \tag{39}$$

3.5 Preload Resistor

A preload resistor can be placed in parallel with the secondary output capacitor bank in order to minimize overshoot above the target output voltage, especially at higher input voltages. A good starting point for this resistor value is to choose a resistor that will discharge around 5 mA of current when at the target output voltage. The exact value of this resistor will need to be experimentally determined based on the given application. The power consumed by this preload resistor can be calculated using:

$$P_{preload} = I^2 R_{preload} \tag{40}$$

The preload resistor should be properly sized in order to properly handle the expected power dissipation.

3.6 Zener Diode

Placing a Zener diode in parallel with the secondary output is another good way to ensure the secondary output voltage stays within a certain range of regulation. The benefit of adding this component is that it will clamp the secondary at the desired voltage, while a preload resistor can be subject to drift due to the magnitude of the input voltage. In this particular application, selecting a Zener with a breakdown voltage of 3.3 V can result in a more tightly regulated secondary output voltage. A resistor can be added in series to the Zener diode to limit current and ensure the power rating of the Zener is not exceeded.

3.7 Snubber Circuit

When the switch node voltage transitions from a high voltage to a low voltage or vice versa, large transient spikes can be reflected from the secondary to the primary side, resulting in spikes on the switch node voltage waveform and primary winding current waveform. These spikes are caused by the resonant LC tank formed by the leakage inductance of the secondary winding and the junction capacitance of the rectifier diode. These spikes can be large enough to exceed the electrical ratings of the converter and result in instability or damage to the device.

To mitigate the risk of these spikes, a simple RC snubber circuit placed in parallel with the secondary rectifying diode can be used. The following are steps to calculate the snubber components are outlined:

Estimate the resonant frequency of the LC tank using the following:

$$f_{tank} = \frac{1}{2\pi \times \sqrt{L_{leakage} \times C_{junction}}} \tag{41}$$

Given a typical leakage inductance of 1% for the 22-µH inductance results in $L_{leakage}$ = 0.22 µH. From the MURA160 data sheet, the junction capacitance during the maximum reverse voltage applied to the diode is 5 pF typical. The approximate f_{tank} = 151 MHz.

Calculate the RC ratio such that the frequency at which the pole is located is as far from the f_{tank} frequency as possible to result in maximum attenuation:

$$f_{snub} = \frac{1}{2\pi \times R_{snub} \times C_{snub}} \tag{42}$$

Selecting R_{snub} = 200 Ω and C_{snub} = 100 pF results in f_{snub} = 1125 Hz, which is approximately five decades away from the f_{tank}.

Determine the best value of C_{snub} to minimize snubber power loss by using the snubber power equation:

$$P_{snub} = C_{snub} V_D^2 f_{sw} \tag{43}$$

$$P_{snub} = (200\ \text{pF}) \times (34\ V)^2 \times 400000\ \text{Hz} \tag{44}$$

$$P_{snub} = 92.4\ \text{mW} \tag{45}$$

This power will be dissipated by the snubber resistor, so the power rating of R_{snub} must be greater than P_{snub}.

4 Experimental Results

4.1 Steady State

The experimental steady state waveforms shown in Figure 4-1 through Figure 4-3 closely resemble those shown in Figure 2-1. A number of interesting observations can be made through a study of the steady state waveforms. As the input voltage is increased, the ringing seen in the secondary turns current waveform also increases. The secondary output voltage ripple is also proportional to the input voltage. Lastly, the peak current through the secondary turns of the coupled inductor is inversely proportional to the input voltage.

All of the following steady state waveforms show the input voltage V_{IN}, the primary side switch voltage V_{sw1}, the secondary output voltage V_{out2}, and the current through the secondary turns of the coupled inductor IL.

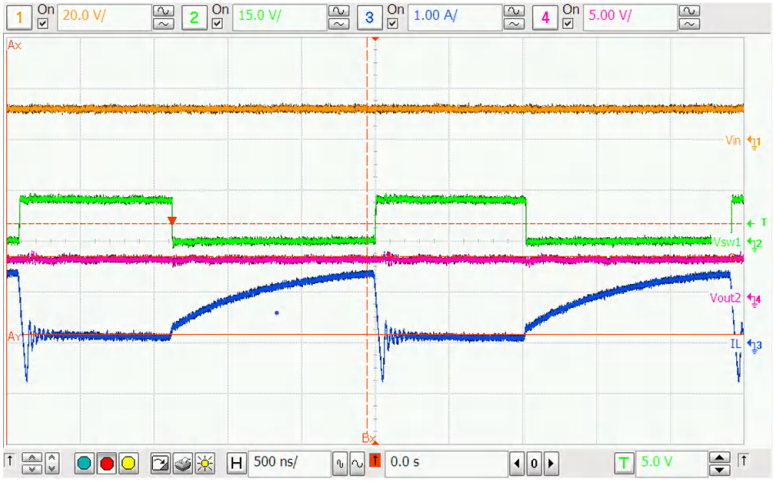

Figure 4-1. 12 V_{IN} Full Load Steady State

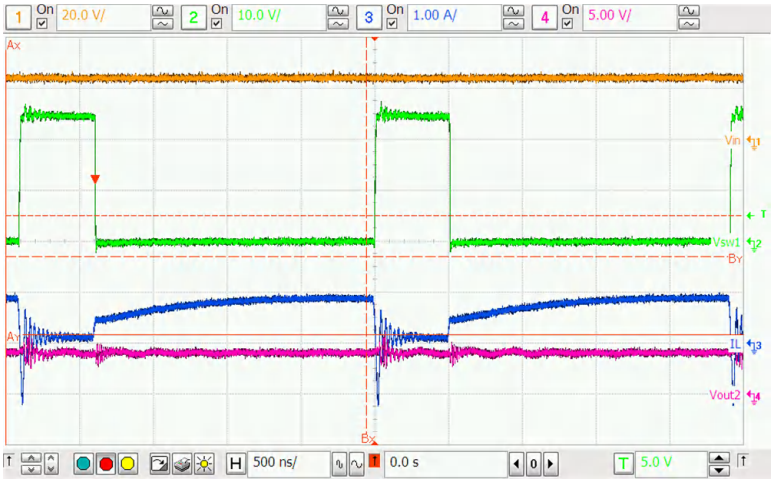

Figure 4-2. 24 V_{IN} Full Load Steady State

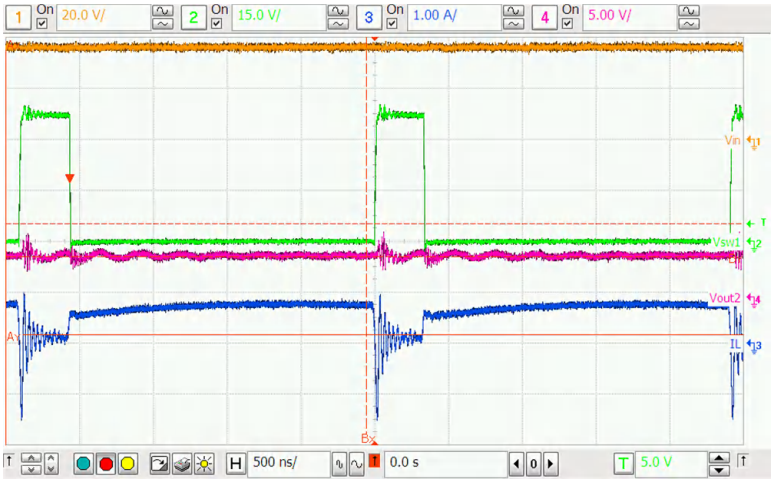

Figure 4-3. 36 V_{IN} Full Load Steady State

4.2 Secondary Output Voltage

Figure 4-4 and Figure 4-5 show how the secondary output voltage ripple increases from no load on either outputs to full load on both outputs for the same input voltage condition. Although not shown here, the secondary output voltage ripple for the case of 12 V_{IN}, I_{OUT2} = 500 mA, and I_{OUT2} = 0 mA is nearly identical to the secondary output voltage ripple waveform shown at full load on both outputs. This represents the worst case of secondary output voltage ripple due to the fact that the secondary output capacitor must supply the entire secondary load current during the device on-time. In contrast, the output voltage ripple is much smaller during the no load condition because the secondary output capacitor only supplies current to the preload resistor.

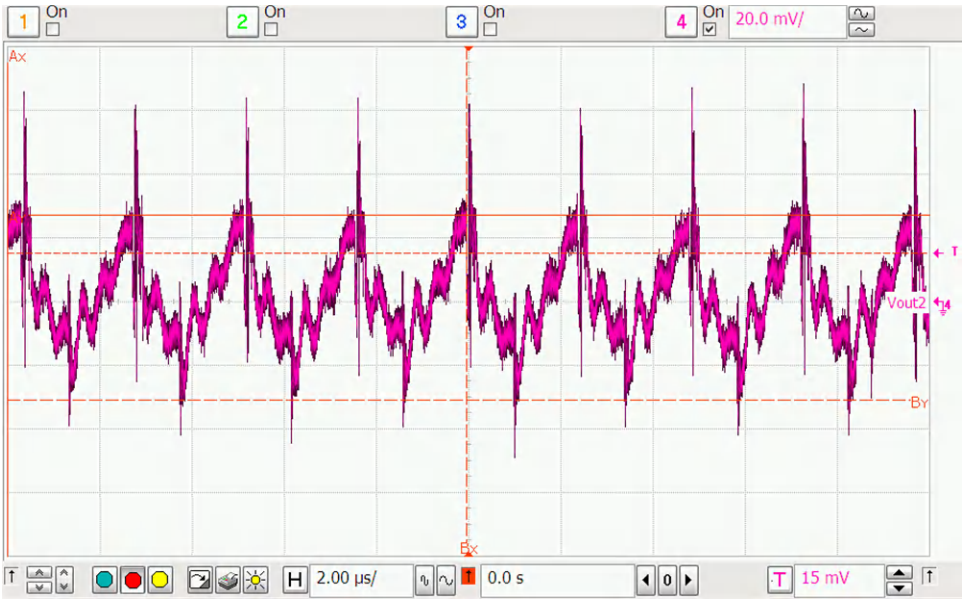

Figure 4-4. Secondary Output Voltage Ripple At Full Load

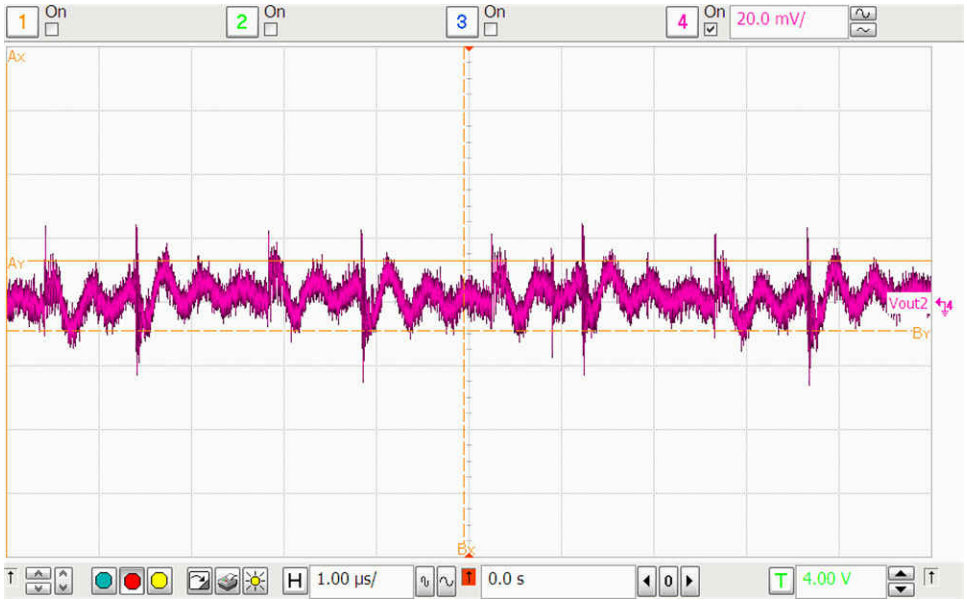

Figure 4-5. Secondary Output Voltage Ripple At No Load

4.3 Load Transient

Load transient performance is a typical way of gauging the performance of a converter. The primary output of the Fly-Buck™ converter shows nearly identical load transient performance to that of a typical non-isolated buck with the same operating conditions. The secondary output load transient performance, however, is worse than that of the primary output because the control loop of the converter does not sense the secondary output voltage and therefore does not respond to changes in it. This means that the secondary output voltage will take longer than the primary output voltage to recover from the same load transient.

Figure 4-6 is the secondary output load transient while the primary output current equals 500 mA and the secondary load is stepped from 0 to 500 mA.

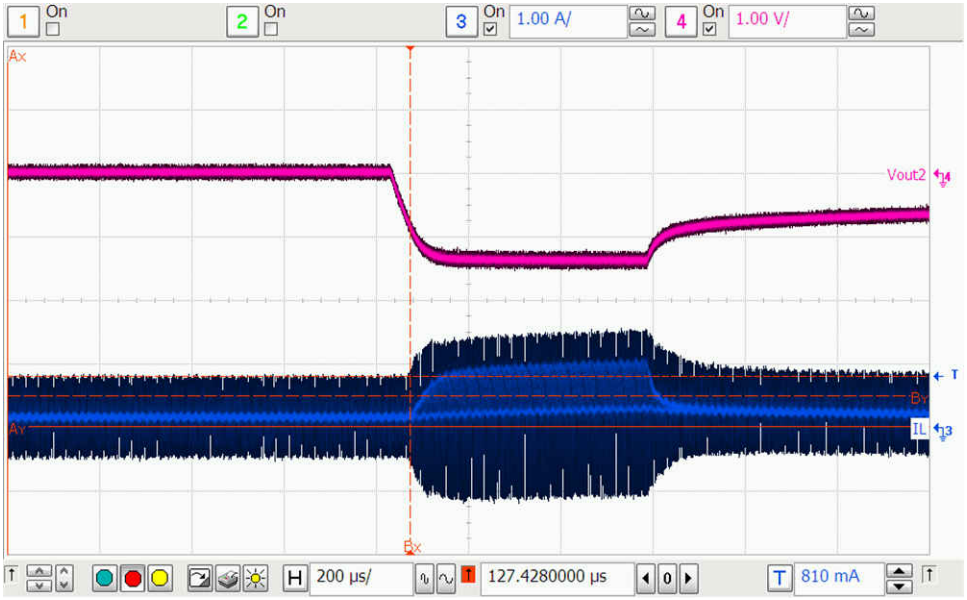

Figure 4-6. 12 V_{IN}, 500 mA1, 0 to 500 mA2 Load Transient

Figure 4-7 shows a zoomed out image of Figure 4-6. It takes the secondary output voltage almost 10 ms to return to within 5% of its desired output voltage.

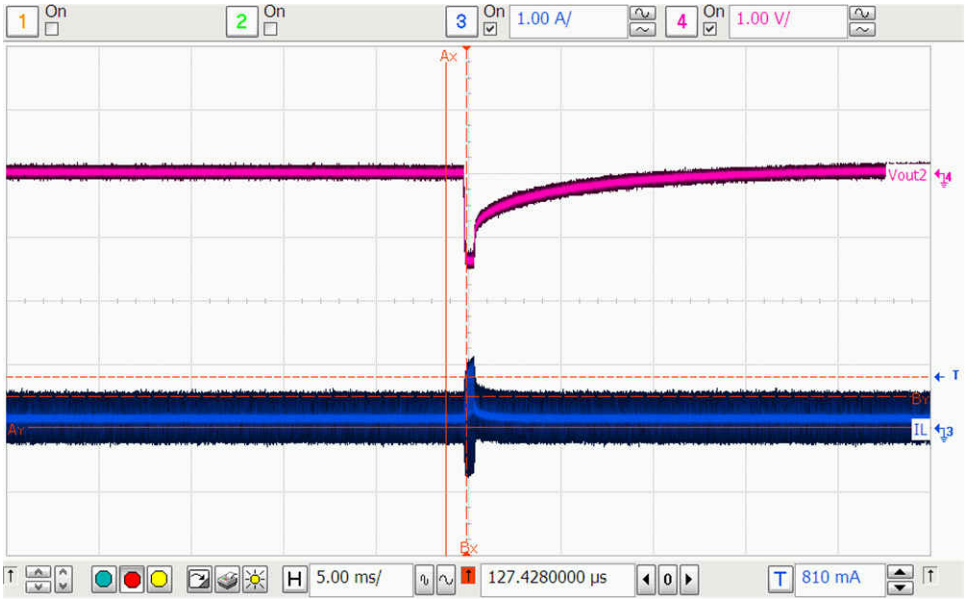

Figure 4-7. 12 V_{IN}, 500 mA1, 0 to 500 mA2 Load Transient Zoomed Out

4.4 Start-up

The typical start-up behavior shows the secondary output voltage tracking the primary output voltage during the soft start sequence.

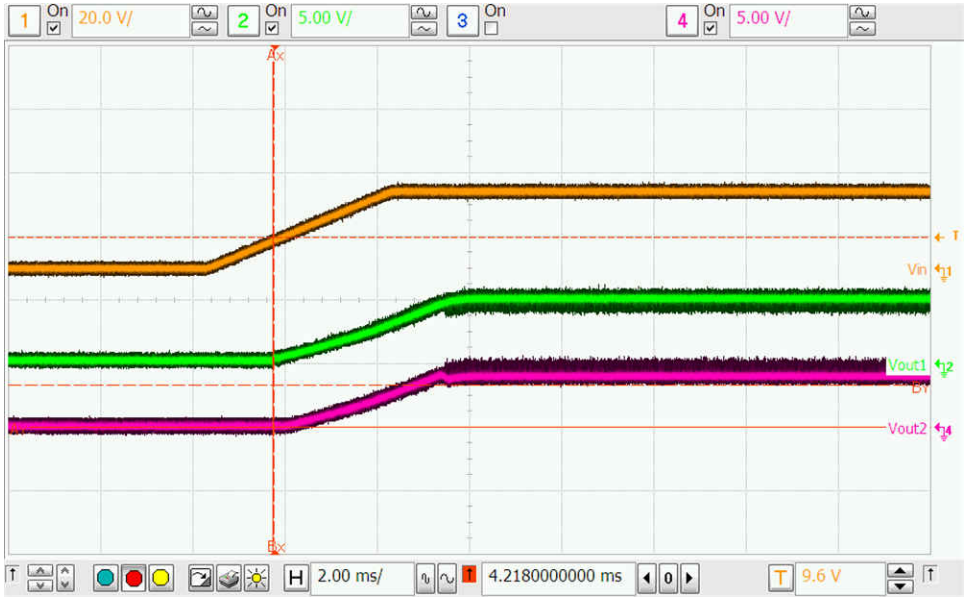

Figure 4-8. 24 V_{IN}, 500 mA1, 500 mA2, 5 V_{OUT1}, 3.3 V_{OUT2}

4.5 Output Current

The following output current measurements are shown in more detail to compare with the calculated output capacitor rms currents.

The ACVrms measurement in Figure 4-12 represents the small signal AC component of the primary or secondary winding current waveforms shown. This small signal component is the current that will flow through the output capacitor bank.

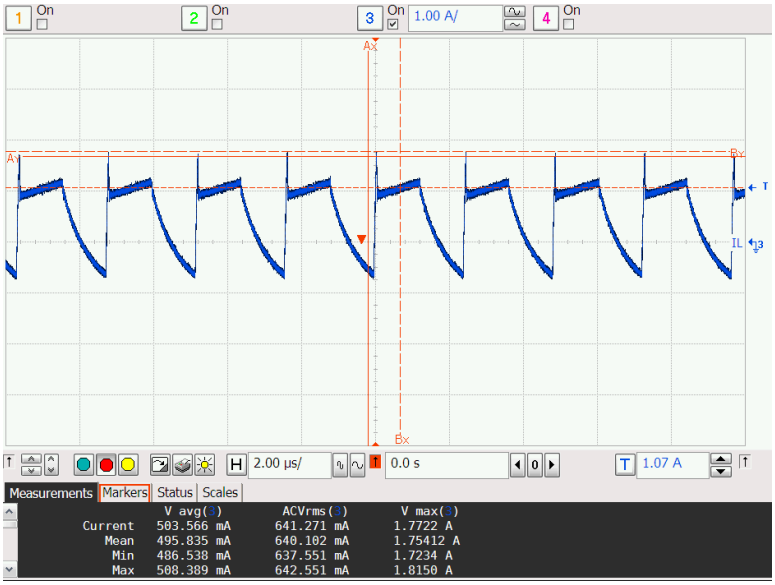

Figure 4-9. Primary winding Current Measurement at 10 V_{IN}

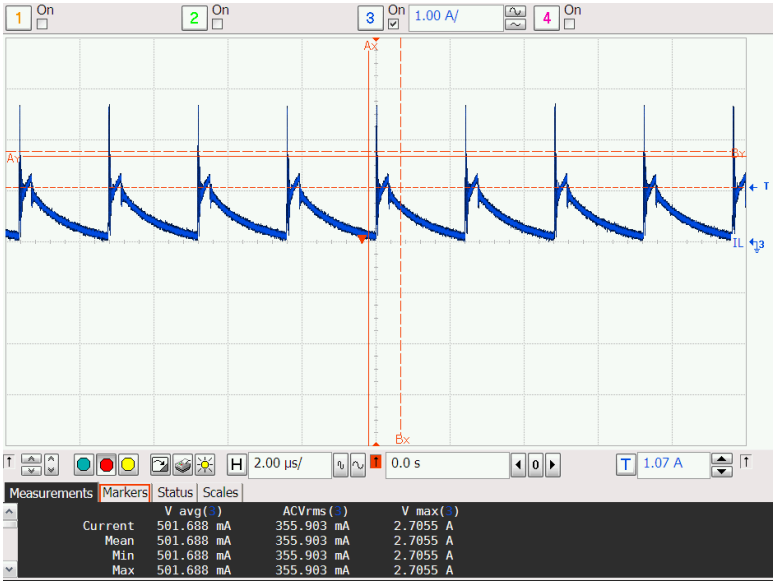

Figure 4-10. Primary winding Current Measurement at 36 V_{IN}

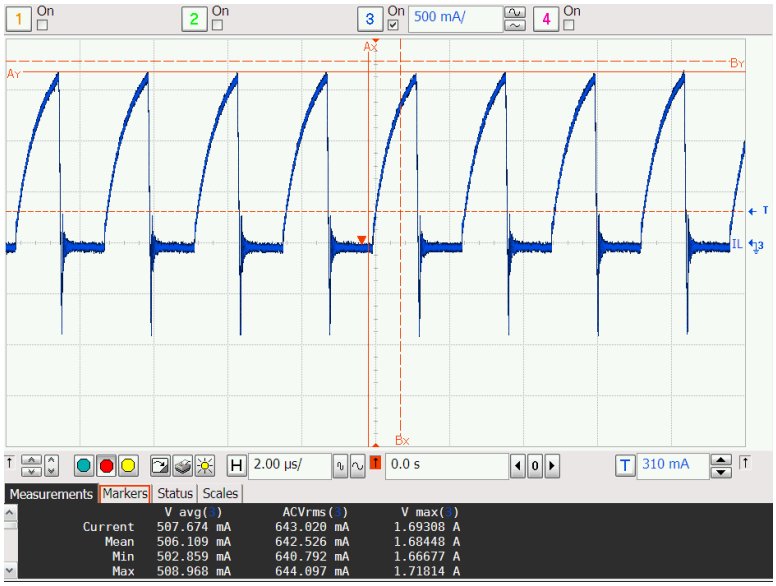

Figure 4-11. Secondary Winding Current Measurement at 10 V_{IN}

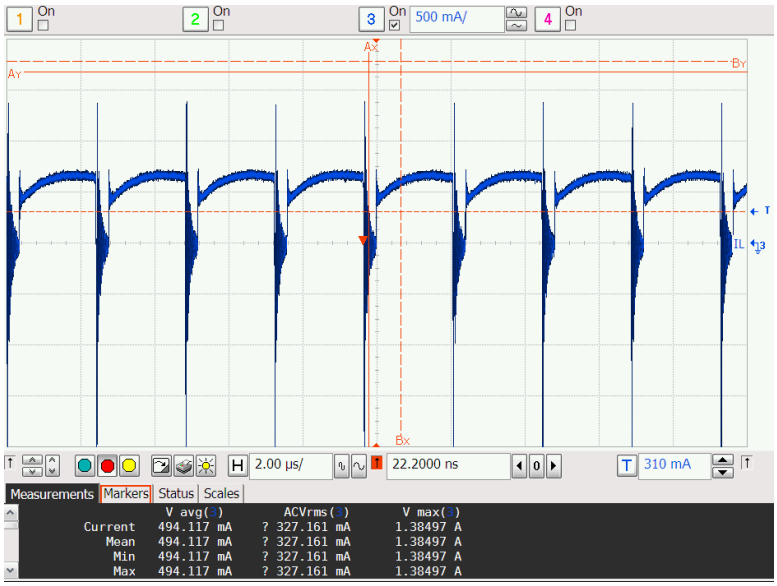

Figure 4-12. Secondary Winding Current Measurement at 36 V_{IN}

5 Conclusion

The LMR36520 buck converter can easily be configured into a simple, low-cost, Fly-Buck™ converter configuration to produce one or multiple isolated secondary outputs. The Fly-Buck™ converter topology favors simple, low-cost, and low-part count design to produce isolated outputs. The regulation accuracy of the isolated outputs can be tuned by using added components such as preload resistors or zener diodes.

6 References

- Texas Instruments, *Designing a Simple and Low Cost Flybuck Solution with the TPS54308* application report.
- Texas Instruments, *LMR36520 SIMPLE SWITCHER® 4.2-V to 65-V, 2-A Synchronous Step-down Converter* data sheet.
- Texas Instruments, *AN-2292 Designing an Isolated Buck (Flybuck) Converter* application report.
- Texas Instruments, *Designing Isolated Rails on the Fly with Fly-Buck Converters* application report.

7 Revision History

Changes from Revision * (October 2020) to Revision A (July 2022)	Page
• Updated *TI* with *Texas Instruments*	1
• Updated *flybuck* to *Fly-Buck™ converter* throughout document	2
• Updated equation formatting throughout document	2
• Updated the primary negative peak inductor current equation	5
• Updated Schottky spelling	10
• Updated the fsnub equation by removing the square root from denominator	11

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