

# **Two Parallel, Synchronous Four-Switch Buck-Boost Converters With Master Slave Method for Higher Power**

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## **ABSTRACT**

The synchronous, four-switch buck-boost controller LM5176 is widely used in automotive start-stop systems, industrial PCs, and a variety of other applications. Paralleling two LM5176 converters is an appealing way to meet a larger power requirement while providing many other benefits, such as enhanced modularity, design flexibility, minimized component ratings, and so forth. The benefits, however, can only be effective if the load currents of each module are equally shared, which is the fundamental difficulty of paralleling supplies.

This application report addresses the use of an active current-sharing architecture that is based on a dedicated master-slave method. Due to an elaborate external circuit with only a few components, the slave can accurately follow the master to deliver the same amount of load current with an error within  $\pm 1.2\%$ . Despite paralleling the converters, the other indexes of the whole system remain satisfactory, including load regulation, load transient, start-up, output ripple, and current limit behavior.

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#### Trademarks

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## 1 Introduction

The LM5176 is a synchronous, four-switch, buck-boost DC/DC controller capable of regulating the output voltage at, above, or below the input voltage. The wide input voltage range of 4 V to 55 V (60-V maximum) makes the controller suitable for automotive start-stop systems, industrial PCs, battery backup systems, point-of-sale (POS) terminals, and a variety of other applications.

One single LM5176 converter can deliver power greater than 200 W because of its synchronous switching topology; however, at a higher power, the increased switching and conduction losses can eventually overwhelm a single converter due to excessive board heating. This overheating makes it necessary to parallel power stages to distribute heat sources, which at the same time provides many other benefits: enhanced modularity, design flexibility, and minimized component ratings. These benefits, however, can only be effective if the load currents of each module are equally shared.

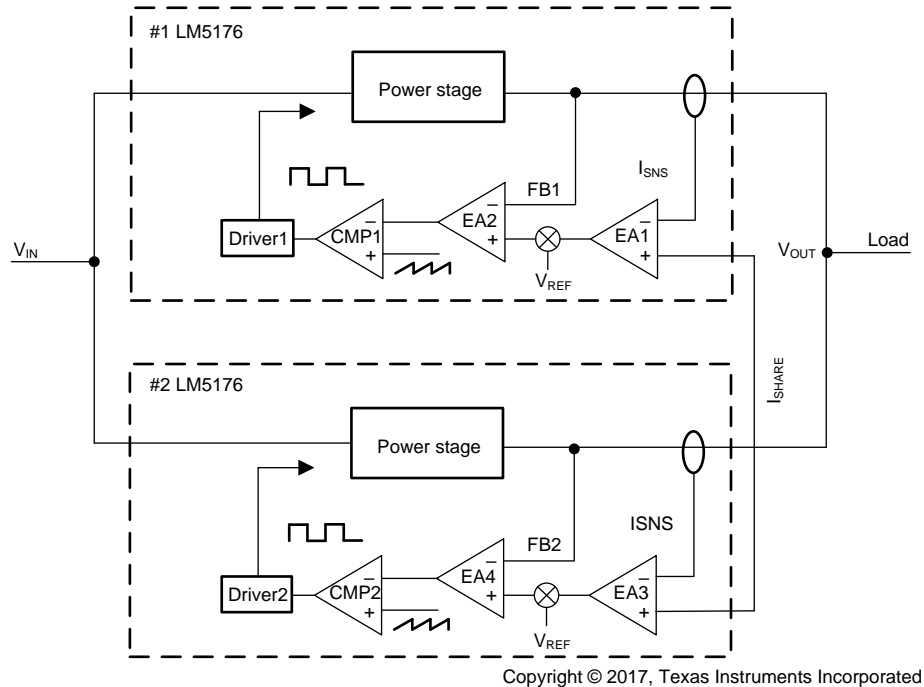
Many sources of literature address different load sharing implementations and often note the trade-off between complexity and accuracy. When using the simplest structure and circuit, the droop-based current sharing method can achieve a comparatively-accurate and even load distribution, at the cost of sacrificing excellent load regulation performance. See *Paralleling Power – Choosing and Applying the Best Technique for Load Sharing* (Balogh 2003) and *Two Parallel, Synchronous, Four-Switch Buck-Boost Converters With Droop Method for Higher Power* for further details.

This application report presents a dedicated, master-slave-based, active-current sharing architecture. With an elaborate external circuit of only a few components, the slave can accurately follow the master to deliver the same amount of load current and with an error that is within  $\pm 1.2\%$ . At the same time, all of the other indexes of the entire system are satisfactory, including load regulation, load transient, start-up, output ripple, and current limit behavior.

## 2 Active Current Sharing for Dedicated Master Slave and its Realization

### 2.1 Active Current Sharing for Dedicated Master Slave

The most accurate way to achieve load sharing is through the means of a closed loop with negative feedback, which also explains the origin of the name "active current sharing". The information for both of the actual load currents and desired load currents must be available to make this approach work. The final goal is to make load currents evenly distributed; therefore, the system must be able to generate the information of average current for all the paralleled power supplies to follow. Figure 1 shows a simplified architecture of the active current-sharing method, where  $I_{\text{SNS}}$  is used to sample actual currents and  $I_{\text{SHARE}}$  serves as the load sharing bus and carries the average current information.



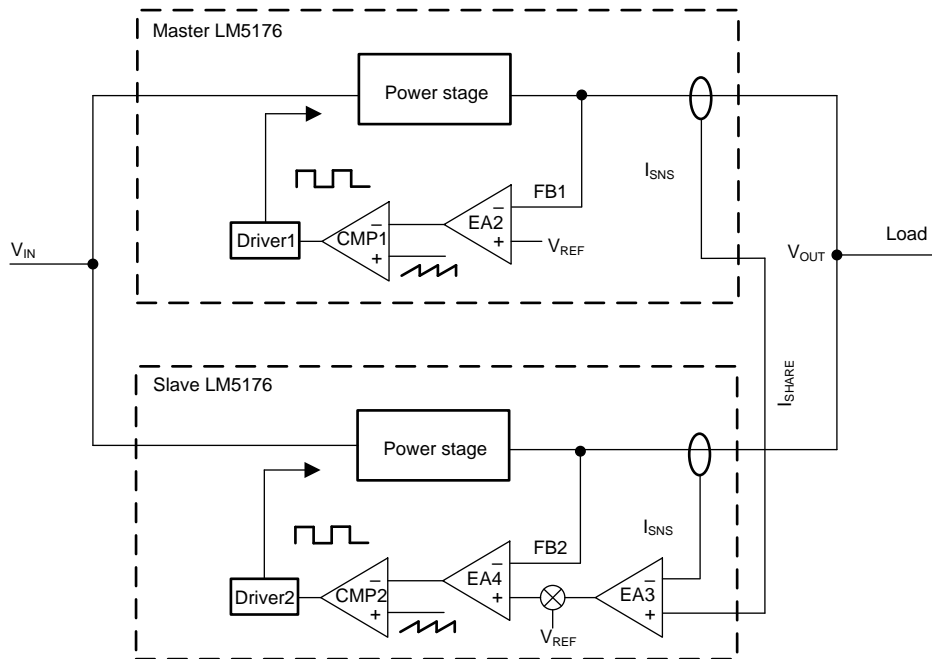
**Figure 1. Simplified Architecture of Active Current Sharing**

As the previous Figure 1 shows, the actual output current of one power supply is compared to the average current represented by the load sharing bus. The error is amplified and can be summed either to the FB pin or to the reference voltage of the voltage error amplifier EA2 (EA4). After this step, the output voltage of each power supply is adjusted to achieve equally-distributed load currents.

The designer can choose from three different solutions to implement the active current-sharing method; however, the dedicated master-slave sharing, as compared to automatic master-slave sharing and democratic load sharing, is an excellent combination of both high accuracy and less complexity.

Figure 2 shows the simplified architecture of the dedicated master-slave sharing. One power supply is the master and the remaining power supply functions as the slave. Only the master controls the average current information, which the load sharing bus represents, and the slave follows the master. Whenever the master load is higher, the slave load adjusts higher by increasing its output voltage and vice versa.

In this case, the load sharing bus is actually the command bus for the slave unit. If the slave can deliver exactly the same current as the master does, the total load perfectly distributes between two modules. Consequently, the signal that the load sharing bus carries is equal to the average current in the system.



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Figure 2. Simplified Architecture of Dedicated Master-Slave Active-Current Sharing

## 2.2 Schematic Realization

Dedicated master-slave active-current sharing involves comparing the load of the slave to the load of the master and then amplifying the error between these two using an error amplifier. Adjust the output voltage of the slave unit by summing the error to either the FB pin or reference pin of the voltage error amplifier. Figure 3 shows an intuitive schematic version, which adjusts the output voltage through the FB pin.

As Figure 3 shows, the output current of the master  $I_M$  is sampled through  $R_{CS1}$  and amplified by the current sense amplifier INA194. The  $R_{F1}$ - $C_{F1}$  network filters the corresponding voltage ( $V_M$ ). The  $V_M$  then serves as the command signal for the slave and is sent to the negative input of the error amplifier LM8261. Similarly,  $V_S$ , which carries the current information of the slave, is sent to the positive input of LM8261. The INA194 device amplifies the error between  $V_M$  and  $V_S$  to  $V_C$ . Use a coupling resistor divider to inject or withdraw a current from the FB pin to adjust the output voltage of the slave lower or higher if its output current  $I_S$  is larger or smaller than that of the master unit  $I_M$ .



If an extreme condition were to occur, the output of LM8261 has the risk of being railed to the  $V_{CC}$  or ground. Carefully select  $R_5$  and  $R_6$  to ensure control of the output voltage of the slave unit. According to the previous [Figure 3](#), the node current calculation for the FB pin is as follows in [Equation 5](#):

$$\frac{V_C - V_{FBs}}{R_5} + \frac{V_{OS} - V_{FBs}}{R_1} = \frac{V_{FBs}}{R_2 \parallel R_6} \quad (5)$$

therefore, write  $V_{OS}$  as follows in [Equation 6](#).

$$V_{OS} = \left( 1 + \frac{R_1}{R_2 \parallel R_6} + \frac{R_1}{R_5} \right) \times V_R - \frac{R_1}{R_5} \times V_C \quad (6)$$

Substitute  $V_C$  with  $V_{CC}$  and ground to obtain two corresponding  $V_{OS}$  values. For a 12-V output condition, with  $R_1$  equal to 280 k $\Omega$  and  $R_2$  equal to 20 k $\Omega$ , select  $R_5$  as 800 k $\Omega$  and  $R_6$  as 400 k $\Omega$  to establish the boundary of  $V_{OS}$  as 12.84 V and 10.27 V.

[Table 1](#) lists all of the component parameters for the dedicated master-slave active-sharing circuit.

**Table 1. Component Parameters for Dedicated Master-Slave Active-Sharing Circuit**

$R_{CS1}$ (m $\Omega$ )	$R_{F1}$ (k $\Omega$ )	$C_{F2}$ ( $\mu$ F)	$R_7$ (k $\Omega$ )	$R_P$ (M $\Omega$ )	$R_5$ (k $\Omega$ )	$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )
2	1	1	1	1	800	280	20
$R_{CS2}$ (m $\Omega$ )	$R_{F2}$ (k $\Omega$ )	$C_{F2}$ ( $\mu$ F)	$R_8$ (k $\Omega$ )	$C_P$ ( $\mu$ $\Omega$ )	$R_6$ (k $\Omega$ )	$R_3$ (k $\Omega$ )	$R_4$ (k $\Omega$ )
2	1	1	1	1	400	280	20

### 3 Test Results

#### 3.1 Load Regulation and Load Distribution

Figure 4 shows the load regulation of the whole system. The variation of the output voltage is within  $\pm 2.5\%$ , which indicates an excellent load regulation performance. Figure 5 shows the test results of a load distributed over an increasing load. Under different input voltage conditions, the output current lines of the master and slave nearly overlap and the error at a 40-A full load is within  $\pm 1.2\%$ .

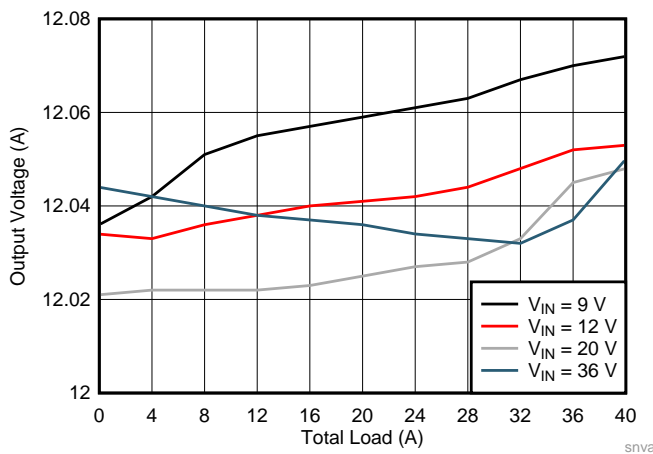


Figure 4. Load Regulation of Parallel Power

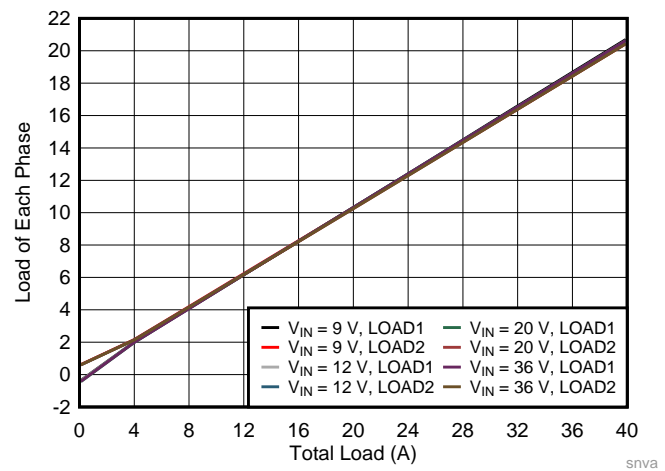


Figure 5. Load Distribution of Two Phases

#### 3.2 SYNC Operation

Use the RT/SYNC pin of the LM5176 device to synchronize the pulse-width modulation (PWM) controller to an external clock. The clocks for two parallel LM5176 converters can either be in-phase or 180° out-of-phase. With in-phase clocks, the current distribution condition is more intuitive.

Figure 6 through Figure 11 show the four switching nodes and inductor current waveforms in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively. The waveforms show that each operation region is stable and the inductor current waveforms of the two phases nearly overlap, which indicates equally-distributed load currents.

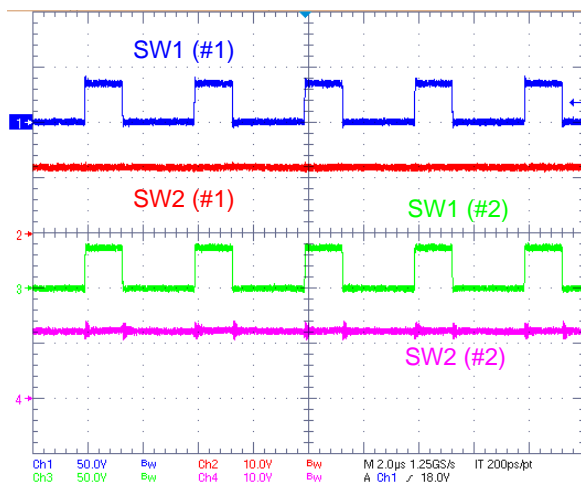


Figure 6. 36-V Buck Region With 40-A Load—Four Switch Nodes

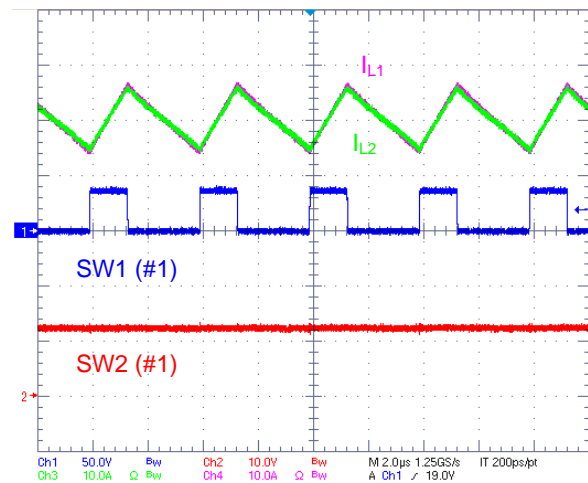


Figure 7. 36-V Buck Region With 40-A Load—Inductor Current Waveforms



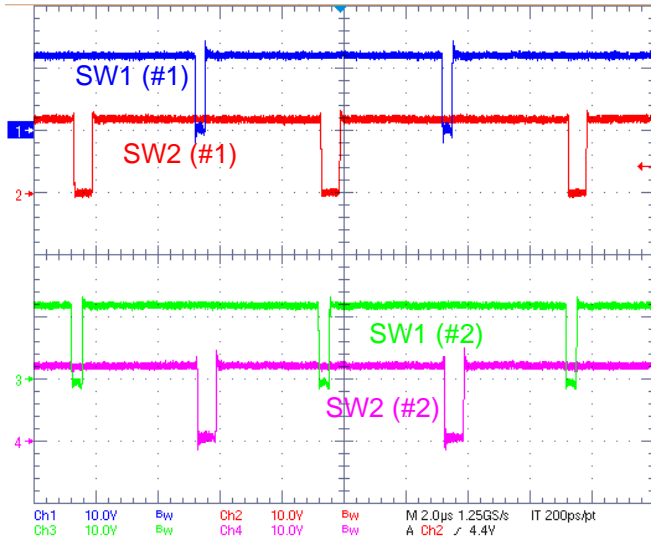


Figure 8. 12-V Buck-Boost Region With 40-A Load—Four Switch Nodes

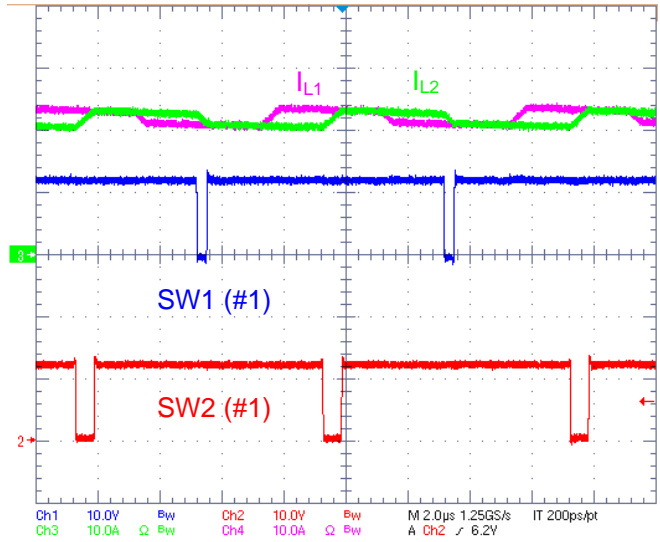


Figure 9. 12-V Buck-Boost Region With 40-A Load—Inductor Current Waveforms

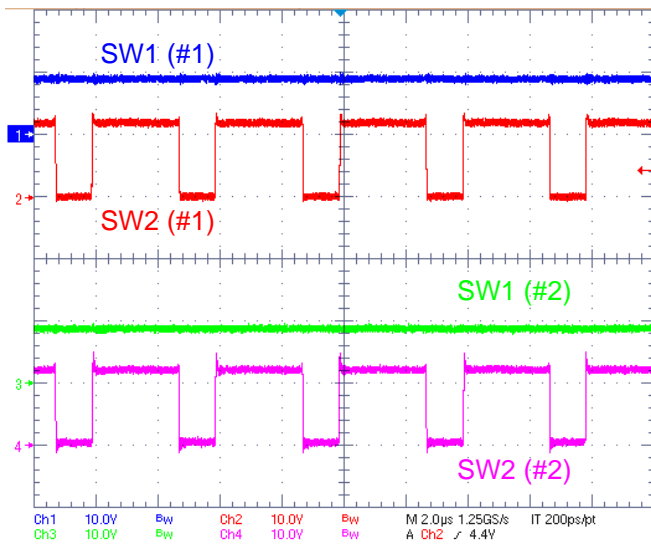


Figure 10. 9-V Boost Region With 40-A Load—Four Switch Nodes

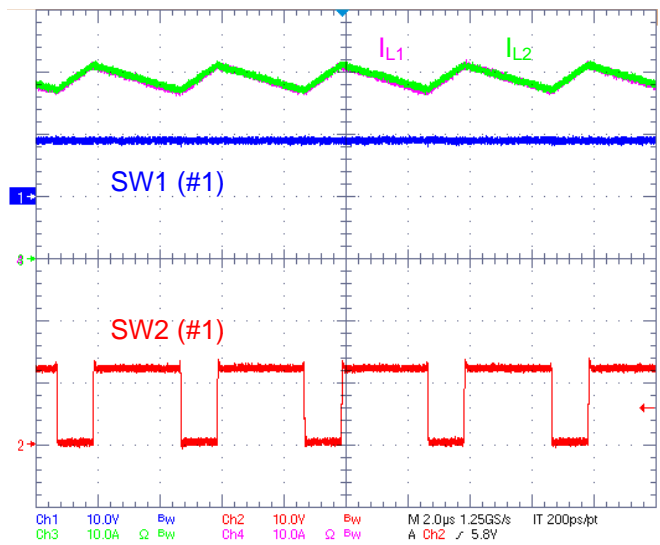
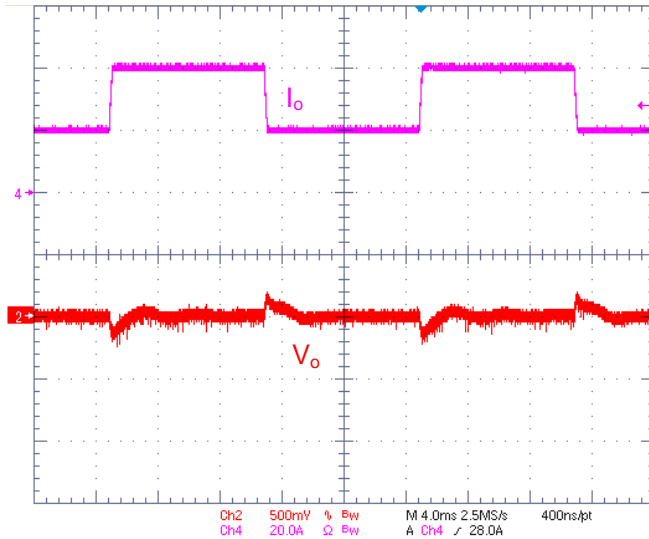
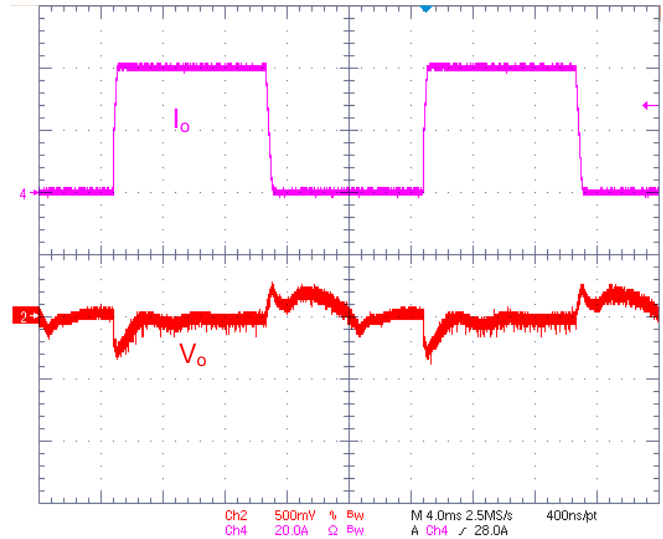


Figure 11. 9-V Boost Region With 40-A Load—Inductor Current Waveforms

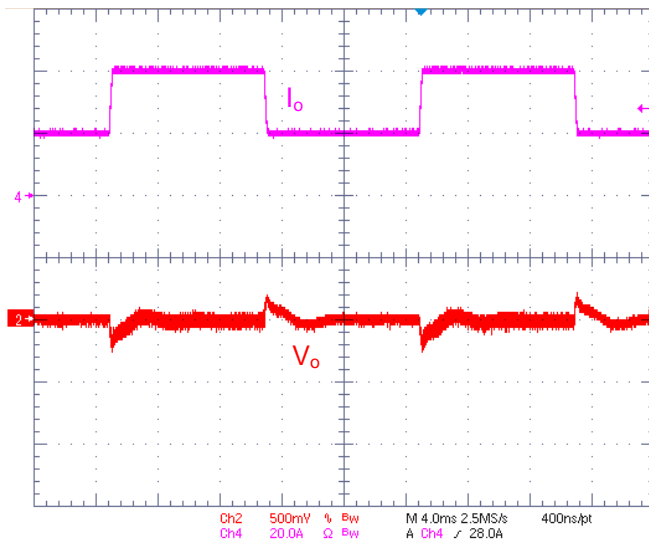
Figure 12 through Figure 17 show the load transient waveforms in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively. The waveforms show two load-step conditions of 20 A to 40 A and 0 A to 40 A.



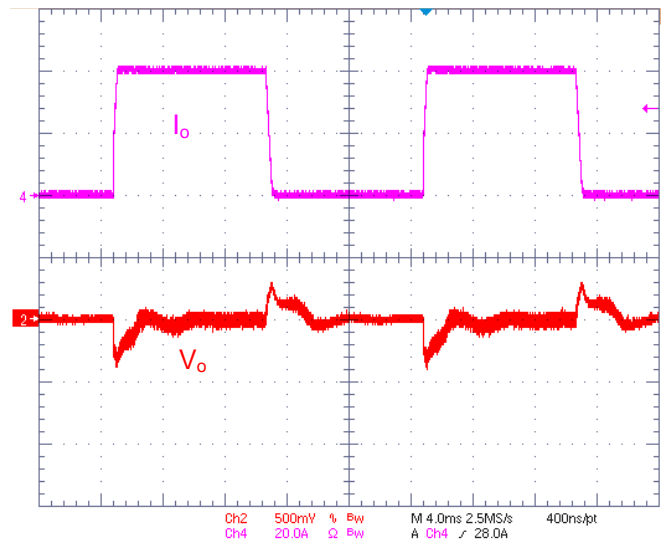
**Figure 12. Load Transient in 36-V Buck Region—With 20-A to 40-A Load Step**



**Figure 13. Load Transient in 36-V Buck Region—With 0-A to 40-A Load Step**



**Figure 14. Load Transient in 12-V Buck-Boost Region—With 20-A to 40-A Load Step**



**Figure 15. Load Transient in 12-V Buck-Boost Region—With 0-A to 40-A Load Step**

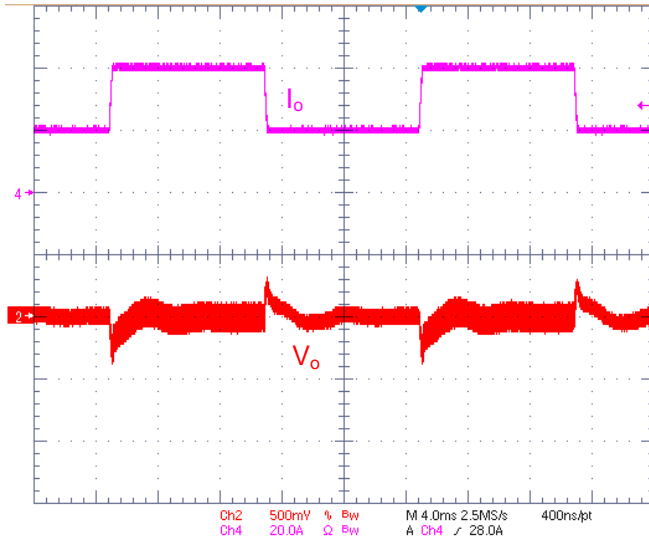


Figure 16. Load Transient in 9-V Boost Region—With 20-A to 40-A Load Step

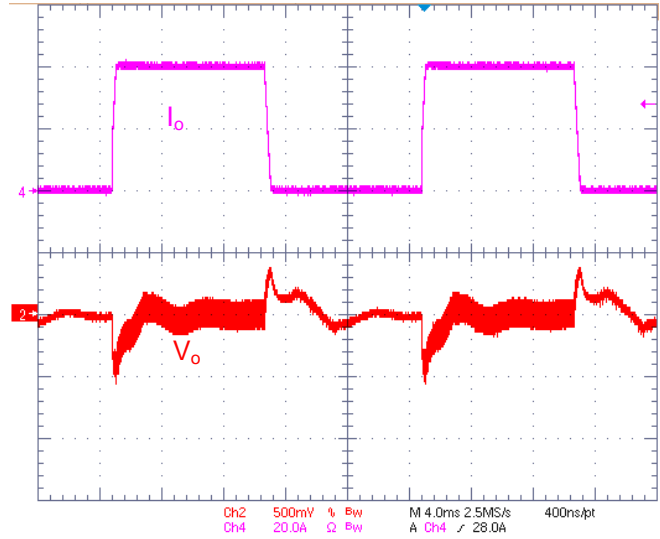


Figure 17. Load Transient in 9-V Boost Region—With 0-A to 40-A Load Step

Figure 18 through Figure 23 show the output ripple waveforms in the 36-V buck, 12-V buck-boost, and 9-V boost region, respectively.

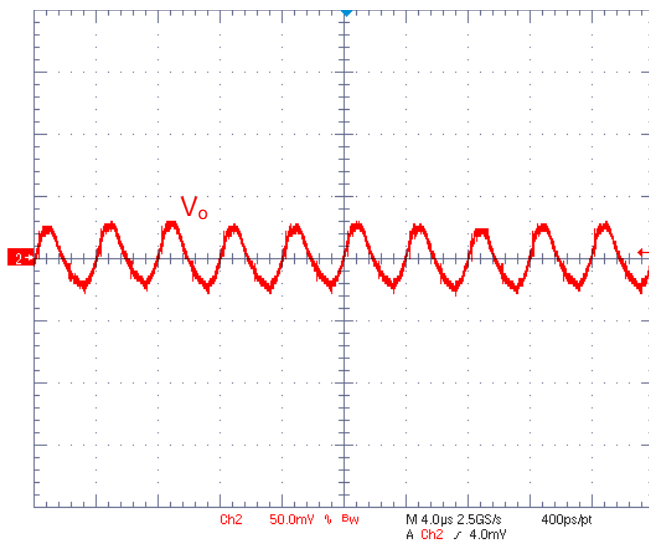


Figure 18. Output Voltage Ripple in 36-V Buck Region—No Load

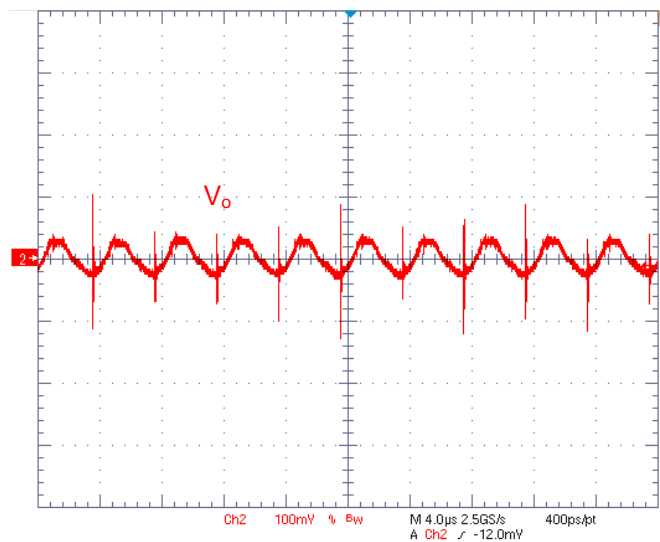


Figure 19. Output Voltage Ripple in 36-V Buck Region—40-A Load

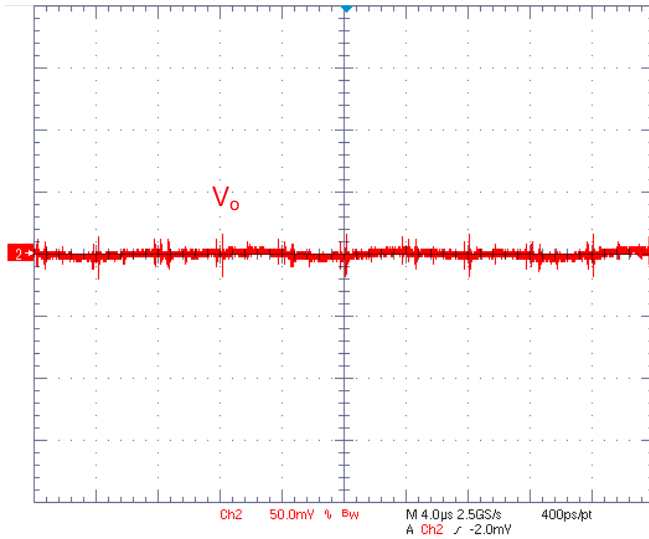


Figure 20. Output Voltage Ripple in 12-V Buck-Boost Region—No Load

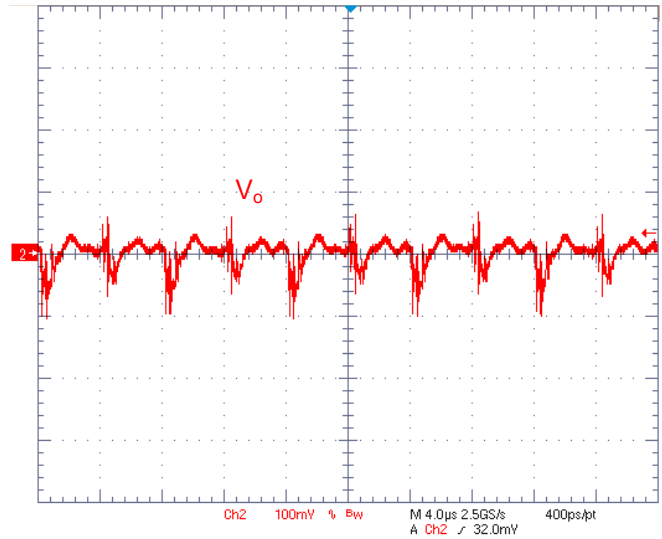


Figure 21. Output Voltage Ripple in 12-V Buck-Boost Region—40-A Load

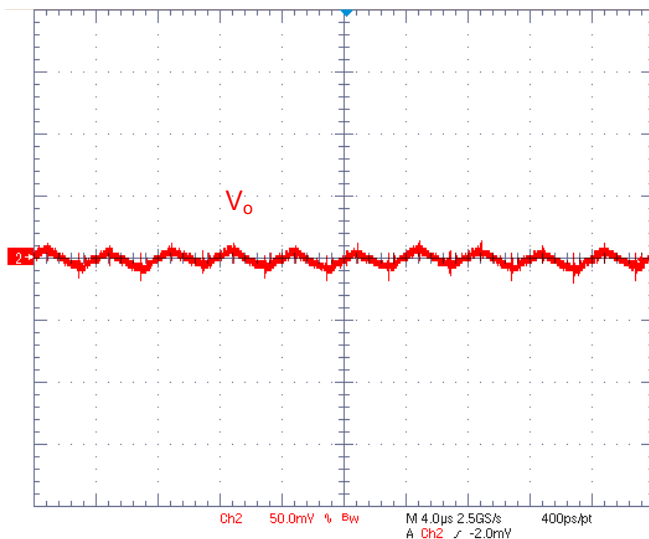


Figure 22. Output Voltage Ripple in 9-V Boost Region—No Load

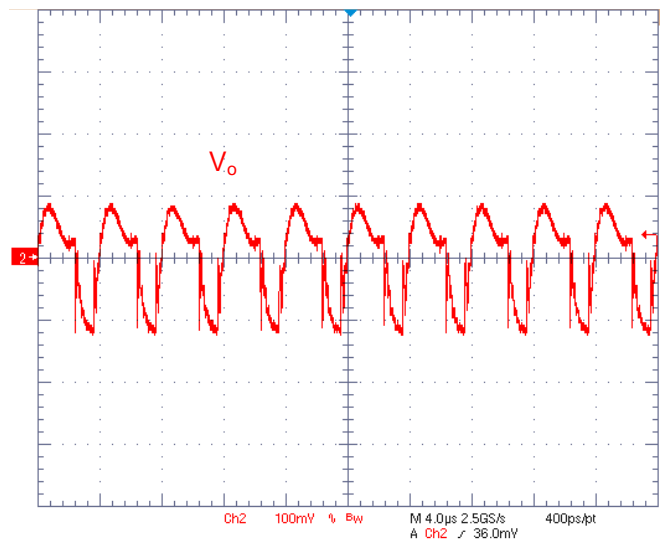


Figure 23. Output Voltage Ripple in 9-V Boost Region—40-A Load

Figure 24 through Figure 29 show the start-up waveforms in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively. The loads are not equally distributed during a certain period of the start-up process due to a sequential order during start-up and the necessary time for a current sharing-circuit to build up and get ready.

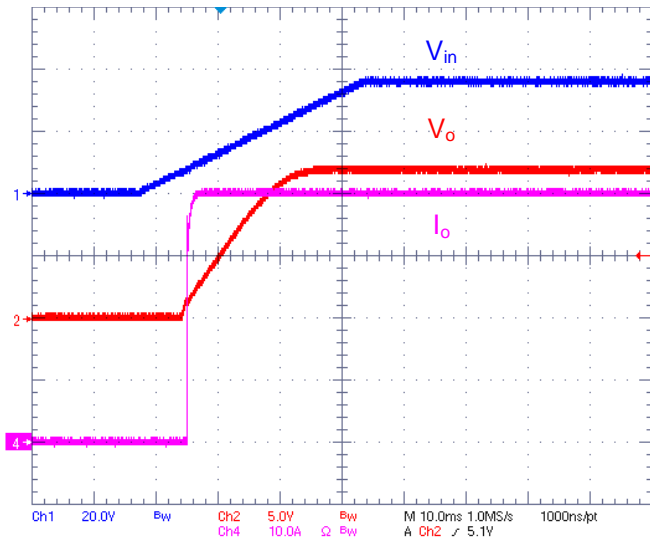


Figure 24. 40-A Start-Up in 36-V Buck Region—Total Output Current Waveform

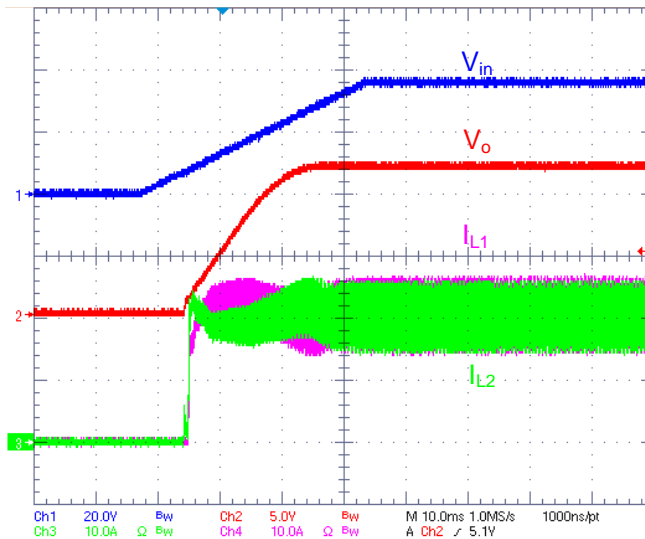


Figure 25. 40-A Start-Up in 36-V Buck Region—Two Phase Inductor Currents

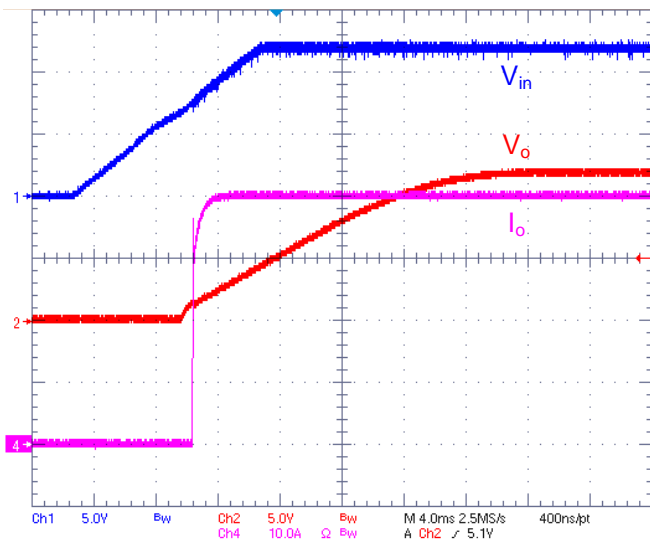


Figure 26. 40-A Start-Up in 12-V Buck-Boost Region—Total Output Current Waveform

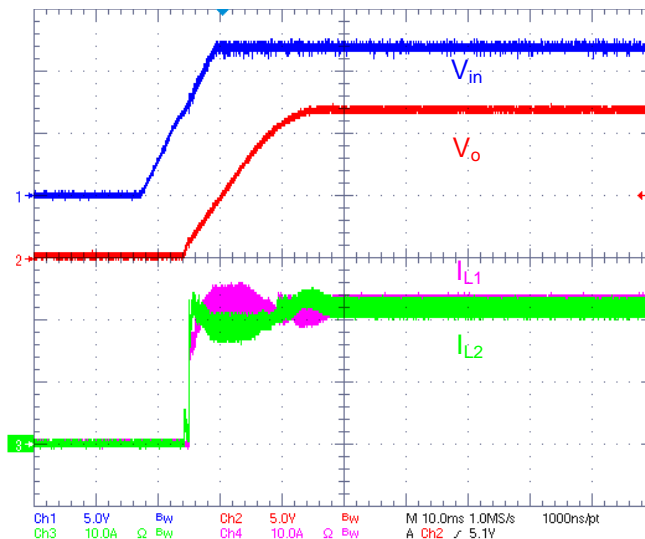


Figure 27. 40-A Start-Up in 12-V Buck-Boost Region—Two Phase Inductor Currents

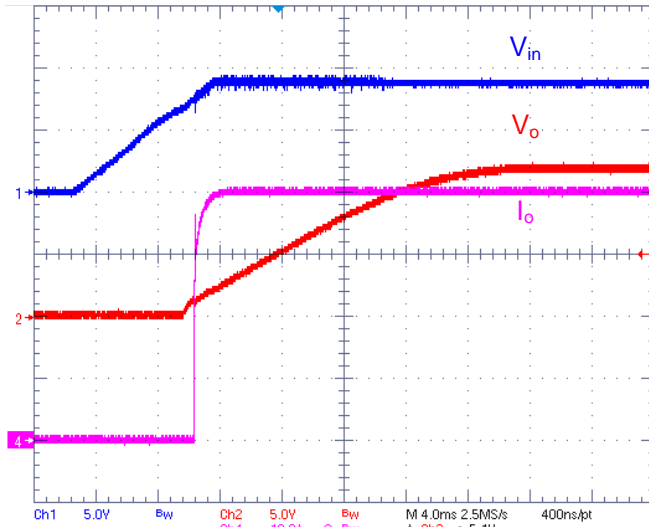


Figure 28. 40-A Start-Up in 9-V Boost Region—Total Output Current Waveform

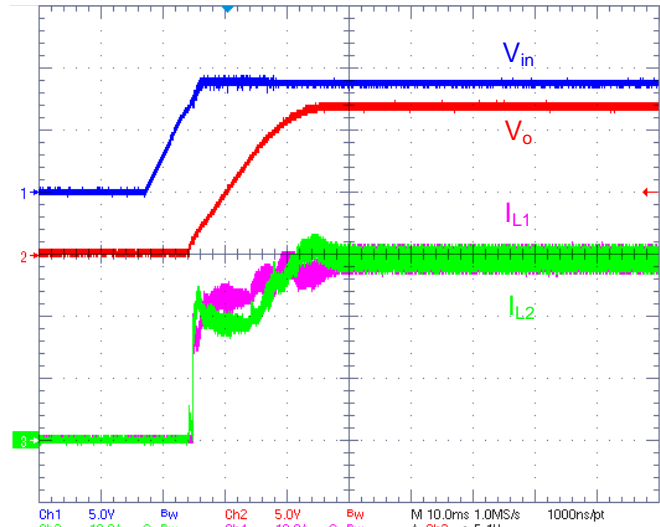


Figure 29. 40-A Start-Up in 9-V Boost Region—Two Phase Inductor Currents

Figure 30 through Figure 35 show the current limit behavior of both hiccup enabled and no hiccup in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively. The 36-V buck does not have a no-hiccup mode, even when it has been enabled, because the average current limit is triggered before the hiccup can occur.

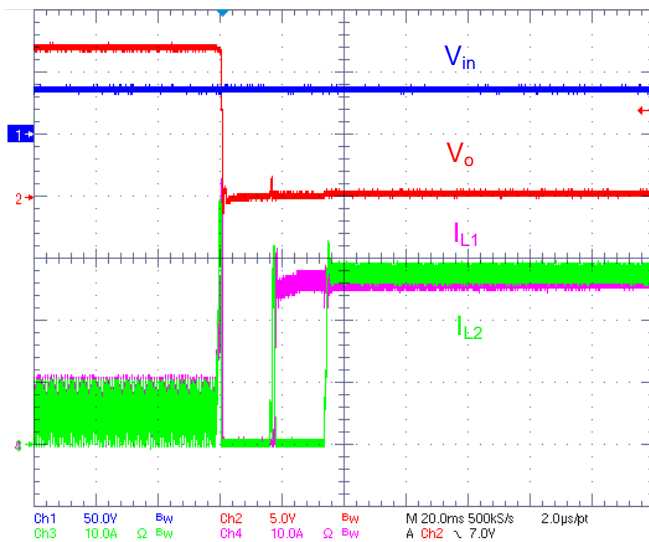


Figure 30. Current Limit Behavior in 36-V Buck Region—Hiccup Enabled

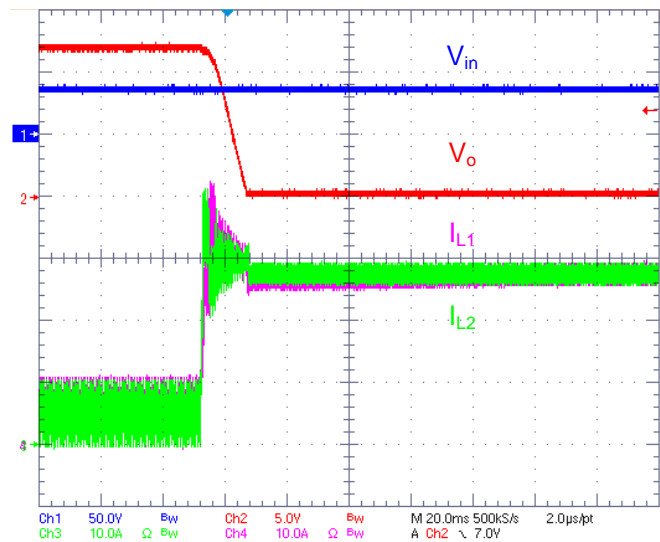


Figure 31. Current Limit Behavior in 36-V Buck Region—No Hiccup

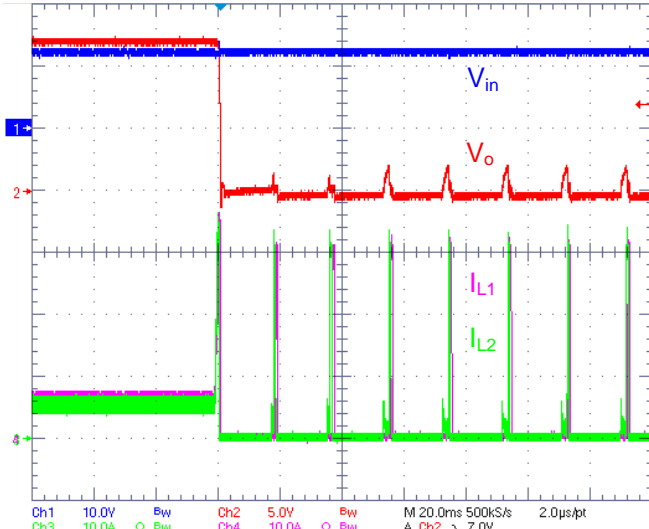


Figure 32. Current Limit Behavior in 12-V Buck-Boost Region—Hiccup Enabled

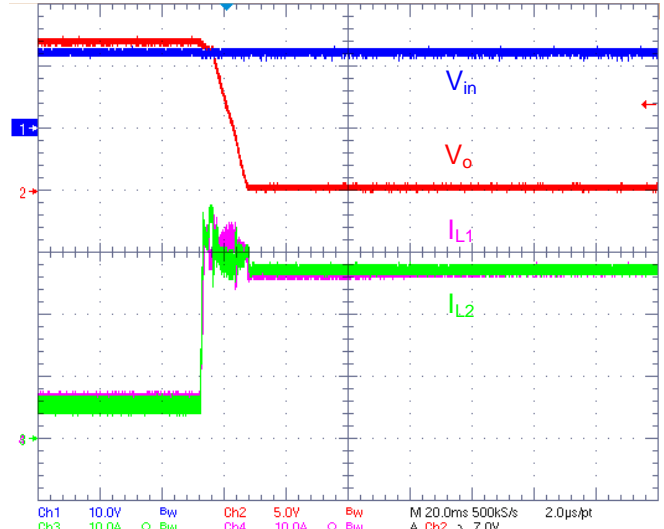


Figure 33. Current Limit Behavior in 12-V Buck-Boost Region—No Hiccup

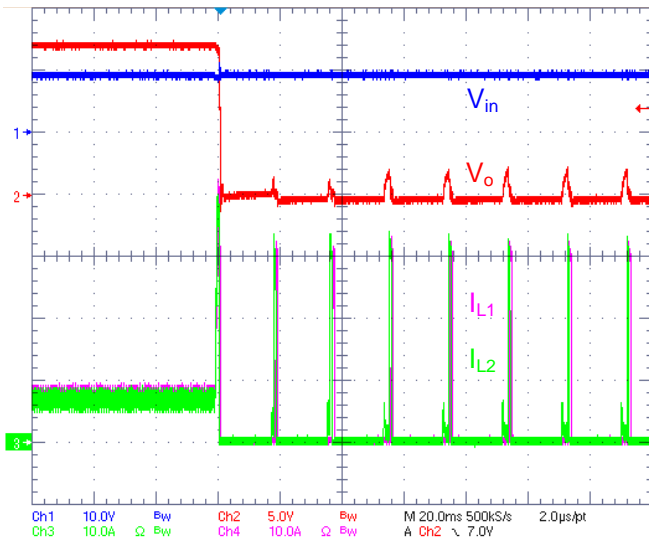


Figure 34. Current Limit Behavior in 9-V Boost Region—Hiccup Enabled

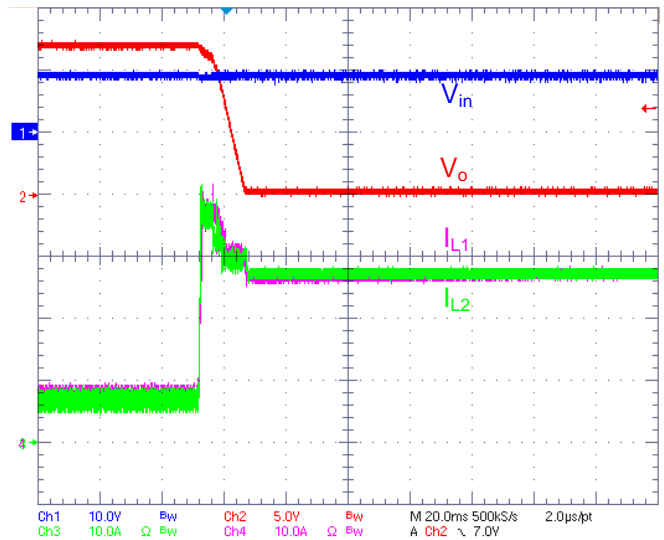
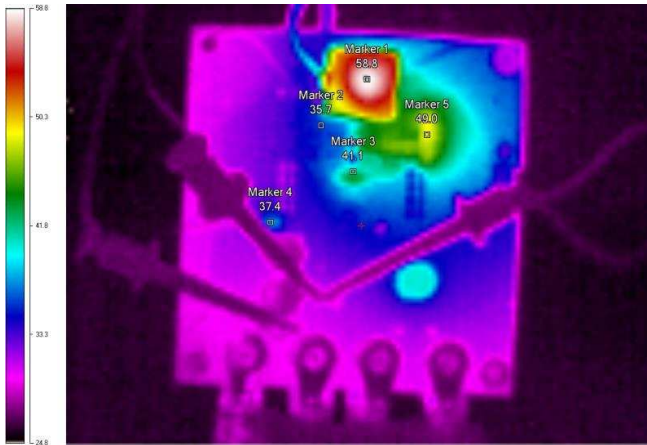
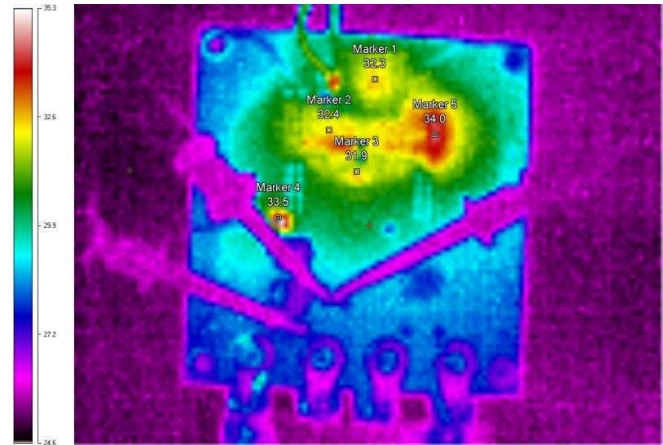


Figure 35. Current Limit Behavior in 9-V Boost Region—No Hiccup

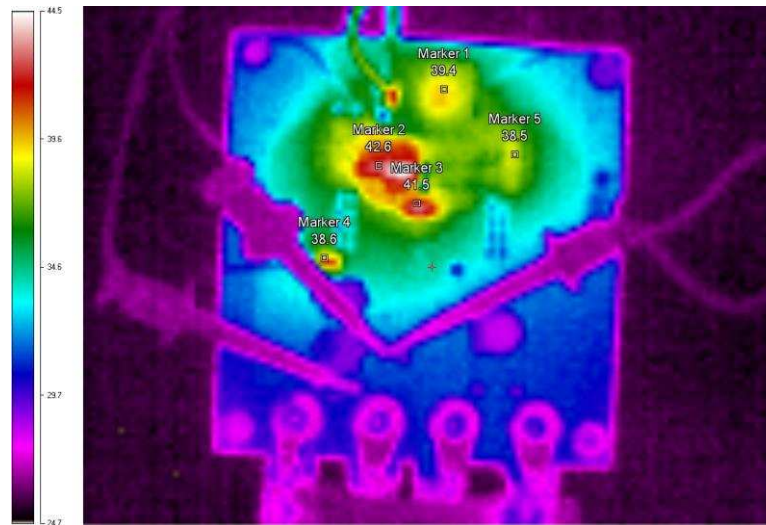
Due to the parallel structure of two LM5176 converters, the heat sources are also distributed. With a 600-CFM airflow, [Figure 36](#) through [Figure 38](#) show the 40-A load thermal condition in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively.



**Figure 36. 40-A Load Thermal Condition in 36-V Buck Region**



**Figure 37. 40-A Load Thermal Condition in 12-V Buck-Boost Region**



**Figure 38. 40-A Load Thermal Condition in 9-V Boost Region**



### 3.3 Interleaved Operation

As previously mentioned, the user can configure two LM5176 converters as 180° out-of-phase, otherwise known as an interleaved architecture. Interleaved architecture provides a better solution for smaller output voltage ripple.

To underscore the discrimination with in-phase operation, Figure 39 through Figure 44 show the four SW nodes and inductor current waveforms in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively.

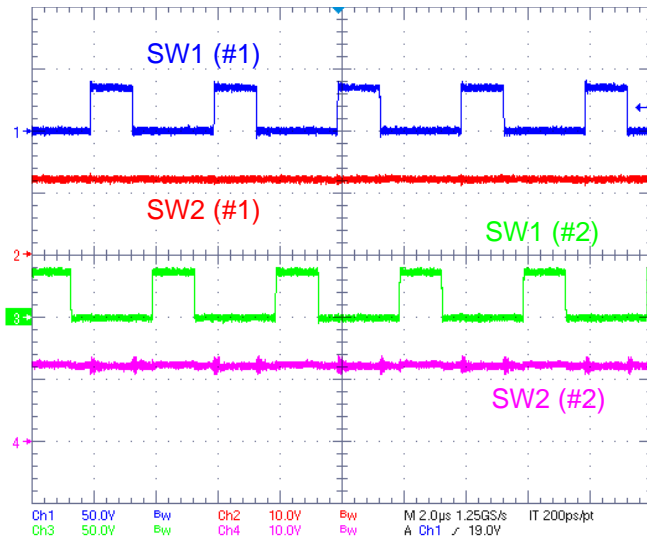


Figure 39. 36-V Buck Region With 40-A Load—Four Switch Nodes

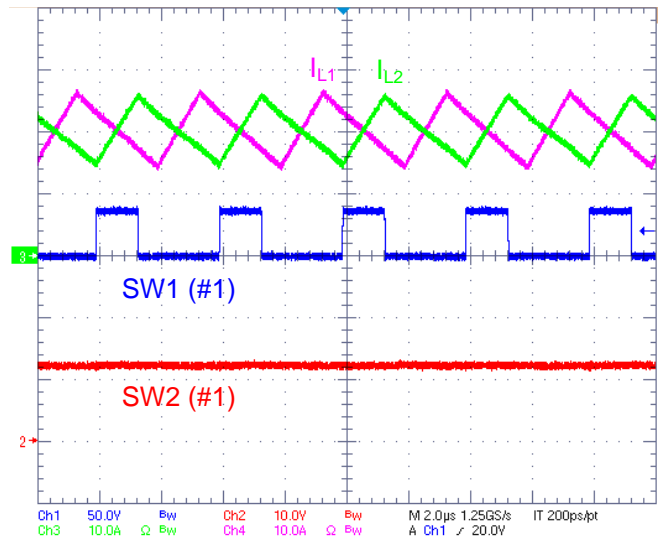


Figure 40. 36-V Buck Region With 40-A Load—Inductor Current Waveforms

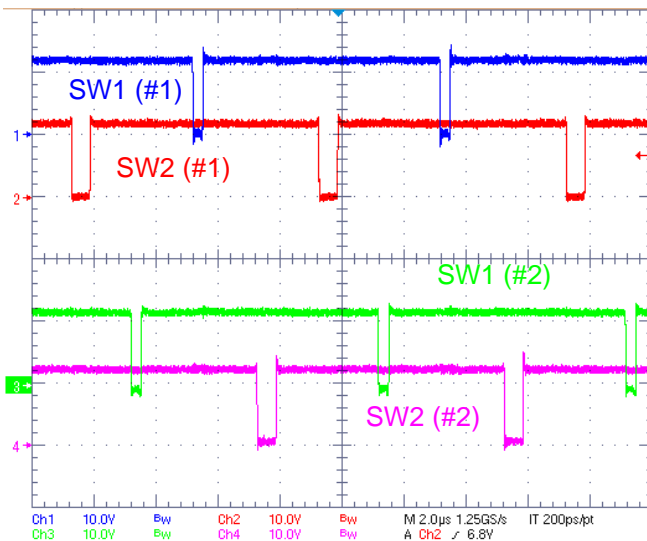


Figure 41. 12-V Buck-Boost Region With 40-A Load—Four Switch Nodes

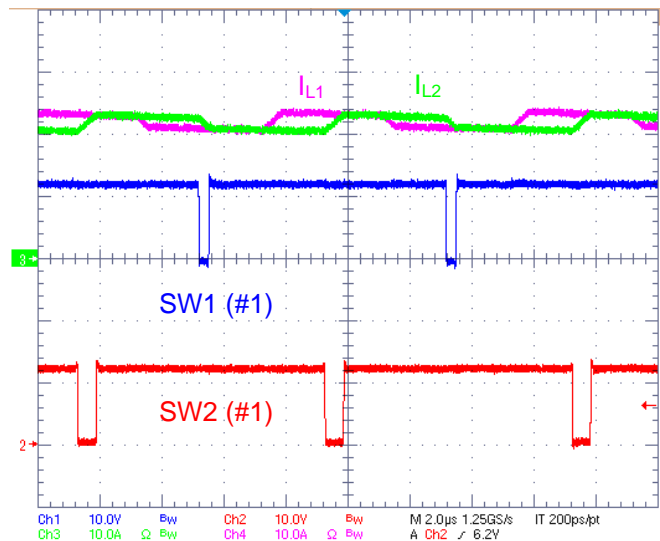


Figure 42. 12-V Buck-Boost Region With 40-A Load—Inductor Current Waveforms

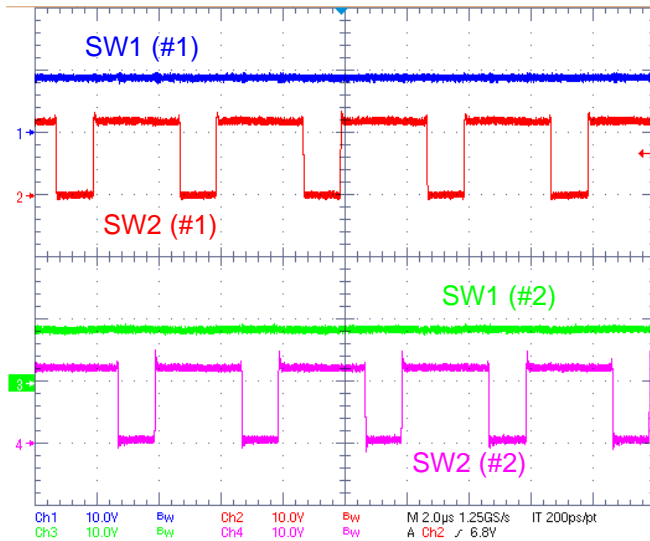


Figure 43. 9-V Boost Region With 40-A Load—Four Switch Nodes

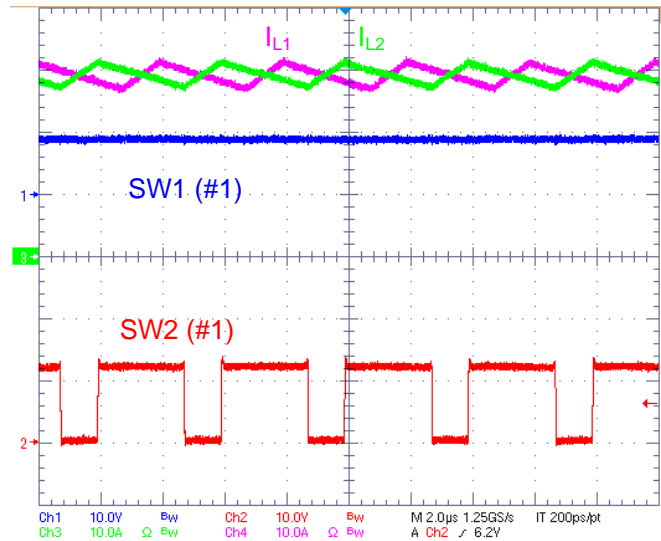


Figure 44. 9-V Boost Region With 40-A Load—Inductor Current Waveforms

Figure 45 through Figure 50 show the output ripple in the 36-V buck, 12-V buck-boost, and 9-V boost regions, respectively. In comparison to Figure 14 through Figure 16, the amplitude of the output voltage ripple is reduced while the frequency is doubled.

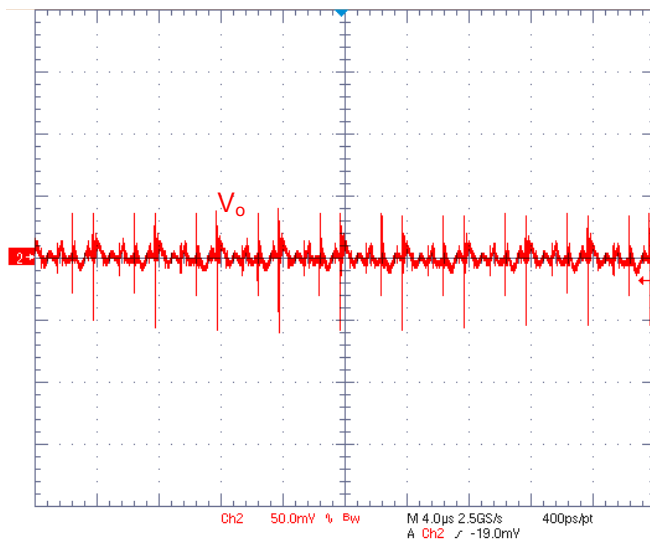


Figure 45. Output Voltage Ripple in 36-V Buck Region—No Load

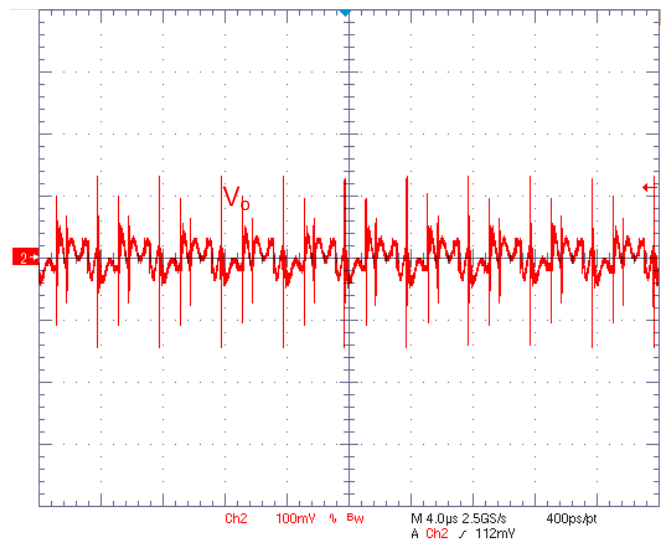


Figure 46. Output Voltage Ripple in 36-V Buck Region—40-A Load

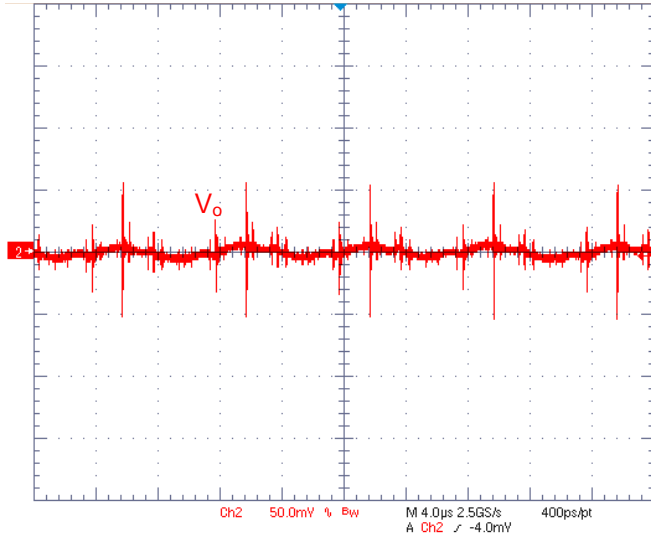


Figure 47. Output Voltage Ripple in 12-V Buck-Boost Region—No Load

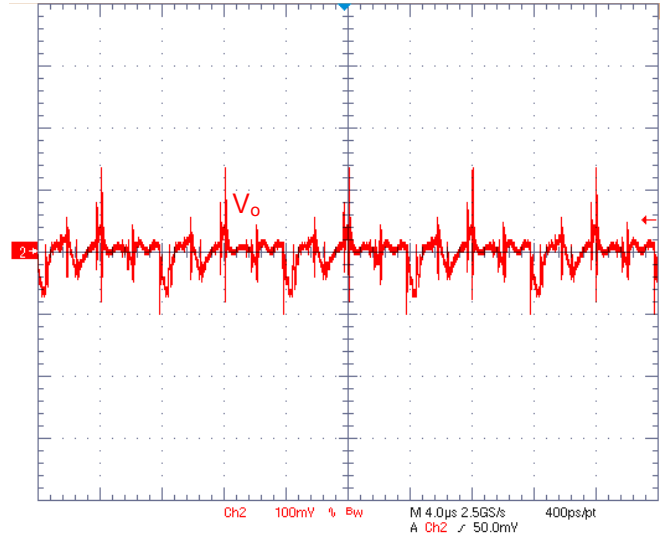


Figure 48. Output Voltage Ripple in 12-V Buck-Boost Region—40-A Load

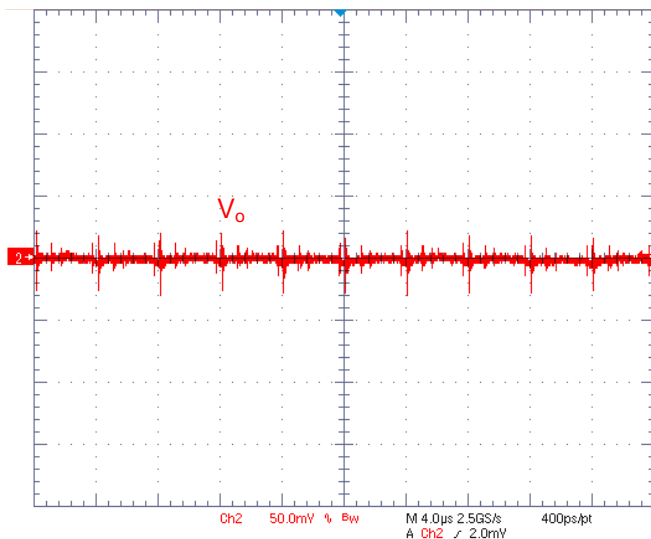


Figure 49. Output Voltage Ripple in 9-V Boost Region—No Load

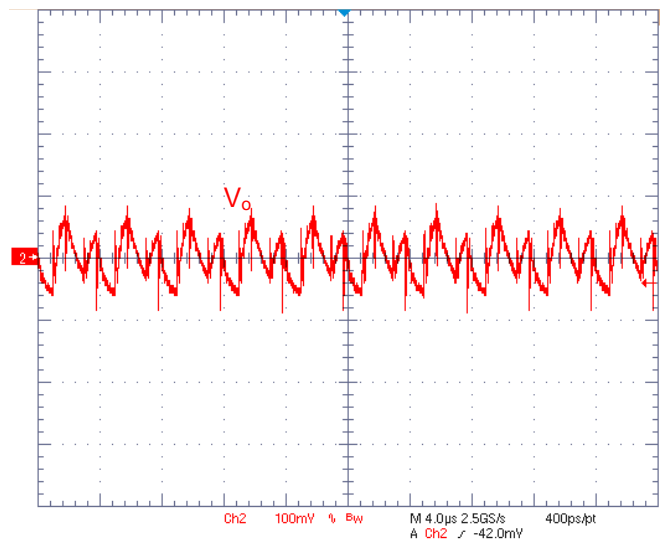


Figure 50. Output Voltage Ripple in 9-V Boost Region—40-A Load

## 4 Conclusion

Unequal load distribution is the fundamental difficulty of parallel power supplies. This application report details a dedicated master-slave-based current-sharing architecture. With an elaborate external circuit of only a few components, the slave can accurately follow the master to deliver the same amount of load current and with an error that is within  $\pm 1.2\%$ . This report also shares the experiment results for parallel LM5176 converters with a 480-W capability, which provide an attractive solution for high-power applications.

## 5 Related Documentation

1. Balogh, Laszlo; *Paralleling Power – Choosing and Applying the Best Technique for Load Sharing*, (2003)
2. Texas Instruments, [Two Parallel, Synchronous, Four-Switch Buck-Boost Converters With Droop Method for Higher Power](#), Application Report (SNVA794)

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