IC package features lead to higher reliability in demanding automotive and communications equipment systems

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Novel DC/DC power package technology not only reduces a power circuit's EMI signature, but also leads to better reliability in high-performance automotive and communications equipment systems. From this standpoint, several IC package attributes such as pinout design and wettable flanks are used to increase reliability and extend product lifetime.

Pinout Design

In general, pinout assignment for a power IC package seeks to avoid having high-impedance signal pins close to high-voltage power pins switching at high frequency. Not only is noise coupling curtailed, but also the effects of parasitic resistive and capacitive paths caused by residual solder flux as well as contaminants arising from the PCB manufacturing process. A problem related to PCB contaminants is likely more evident in operating environments with high ambient temperature and high humidity.

Establishing a distinct separation between high-voltage power pins and low-voltage precision analog signal pins through careful pinout assignment is particularly important for high-voltage applications, such as 48-V Lithium-Ion mild-hybrid EV battery systems.

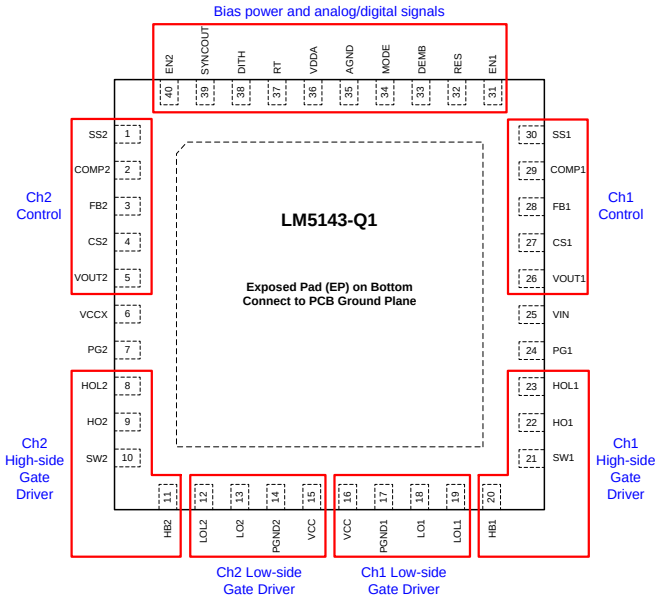

Figure 1. LM5143-Q1 dual-channel synchronous buck controller pinout diagram

Separating power and signal with package pinout also simplifies PCB layout routing and component placement, leading to a compact yet robust design.

Refer to the pinout diagram in Figure 1 as an example of a package with strategic placement for power and signal functionality. This is the LM5143-Q1 from TI, a 65-V multi-phase synchronous buck controller used in automotive ADAS, cluster and body electronics systems.

As shown, the LM5143-Q1 controller has a symmetric pinout structure for each buck regulator channel. The pins related to the power stage gate drives (LO1/2, HO1/2) are located on one side of the package and are physically separated from the small-signal analog pins associated with control and compensation (SS1/2, FB1/2, COMP1/2, CS1/2). The groups of power pins are buffered from critical signal pins by adjacent pins with digital functions (PG1/2) or those with DC voltage applied (VIN, VCCX).

In particular, the high-voltage switch (SW1/2) and bootstrap (HB1/2) pins are located to mitigate the possibility of coupling to adjacent sensitive nodes due to switching at high slew rate (*dv/dt*) and high frequency. Dedicated VCC and PGND pins for each channel reduce the possibility of channel crosstalk and interference, particularly at 50% duty cycle operation when the two channels are interleaved 180° out-of-phase.

Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required in high-volume automotive applications to meet demands for high reliability, safety and robustness. Standard quad-flat no-lead (QFN) and small-outline no-lead (SON) packages do not have solderable or exposed pins and terminals that are easily viewed. It is therefore difficult to assess visually whether or not the package is successfully soldered onto the PCB.

The wettable flank process was developed to resolve the issue of side-lead wetting of leadless packaging. As an example, consider the LM5146-Q1, a 100-V automotive synchronous buck controller. It is available in a 20-pin VQFN package with wettable flanks to provide a visual indicator of solderability. During the PCB assembly process, the solder joint extends from

the underside of the pad up the sidewall, resulting in an enhanced solder joint between the component and PCB. AVI can then assess the existence of acceptable solder joints on all sides of the device, reducing inspection time and manufacturing costs and obviating the need for expensive x-ray inspection equipment.

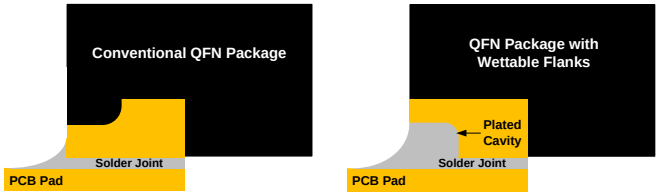

Figure 2. Wettable flank pins with step cut

Figure 2 shows a diagram of a QFN wettable-flank lead-frame package. A toe fillet and complete solder joint between package and PCB provide a reliable solder joint to pass the stringent 100% AVI requirements preferred by the automotive industry.

High-Voltage Clearance Spacing

To understand the concept of high-voltage clearance, consider the package and pin dimensions of the LM5164-Q1 100-V, 1-A synchronous buck converter presented in Figure 3. As shown, the pin pitch of this converter with conventional SOIC-8 package is 1.27 mm, resulting in a pin-to-pin clearance distance of 0.86 mm.

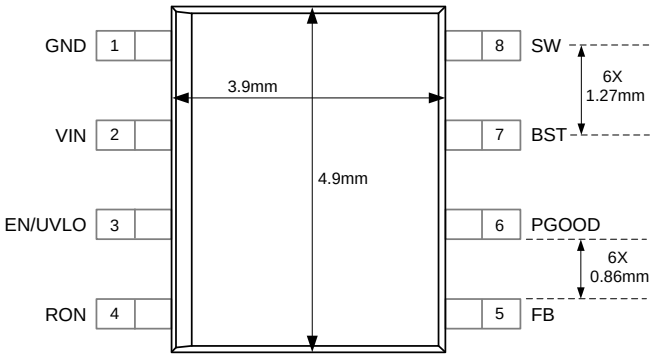

Figure 3. LM5164-Q1 buck converter pinout diagram (top view)

The substantial spacing between high-voltage nodes (such as VIN and GND) means that the LM5164-Q1 power stage PCB layout can satisfy spacing guidelines recommended by IPC-9592B for power conversion circuits with high input voltages — for example, those found in communications wireless infrastructure applications, such as remote radio units (RRU) and active antenna systems (AAS).

Equation 1 defines the uncoated copper-to-copper conductor clearance spacing set by IPC-9592B.

$$D\,[\text{mm}] = \begin{cases} 0.13, & V_{PEAK} < 15\,V \\ 0.25, & 15\,V \le V_{PEAK} < 30\,V \\ 0.1 + 0.01 \cdot V_{PEAK}, & 30\,V \le V_{PEAK} < 100\,V \end{cases} \quad (1)$$

In general, high-voltage clearance in applications with voltages greater than 60 V is best achieved by using leaded packages such as SOIC and HTSSOP.

Table 1. DC/DC controller package details

Device	Topology, $V_{IN(max)}$	Performance Feature	Package, Body Size, Pitch
LM5146-Q1	Sync buck, 100 V	Wettable flanks, optimized pinout, high-voltage spacing	VQFN (20), 3.5 × 4.5 mm, 0.5 mm
LM5116	Sync buck, 100 V	Leaded package, high-voltage spacing	HVSSOP (20), 6.5 × 4.4 mm, 0.65 mm
LM5170-Q1	Sync buck/ boost, 85 V	Leaded package, optimized pinout, high-voltage spacing	HTQFP (48), 7 × 7 mm, 0.5 mm
LM5141-Q1	Sync buck, 65 V	Wettable flanks, optimized pinout	VQFN (24), 4 × 4 mm, 0.5 mm
LM5150-Q1	Boost, 42 V	Wettable flanks, optimized pinout	WQFN (16), 4 × 4 mm, 0.65 mm

Table 2. DC/DC buck converter package details

Device	$V_{IN(max)}$, I_{OUT}	Performance Feature	Package, Body Size, Pitch
LM5164-Q1	100 V, 1 A	Low I_Q, pin spacing	SOIC (8), 4.9 × 3.9 mm, 1.27 mm
LMR36015-Q1	60 V, 1.5 A	HotRod QFN, wettable flanks	VQFN-HR (12), 2 × 3 mm, 0.5 mm
LMR16030	60 V, 3 A	Cost effective, pin spacing	SOIC (8), 4.9 × 3.9 mm, 1.27 mm
LMS3655-Q1	36 V, 5.5 A	HotRod QFN, wettable flanks	VQFN-HR (22), 5 × 4 mm, 0.5 mm
LM73606-Q1	36 V, 6 A	HotRod QFN, wettable flanks	WQFN (30), 6 × 4 mm, 0.5 mm

Table 3. Related TI application notes

SNVA802	Improving RF power amplifier efficiency in 5G radio systems using an adjustable DC/DC buck regulator
SNVA803	Improving EMI for free with careful PCB layout
SNVA806	Powering drones with a wide V_{IN} DC/DC converter

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