How to Design a Boost Converter Using LM5155

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ABSTRACT

The LM5155 is a versatile non-synchronous low-side N-FET controller for switching regulators. The common configurations for the LM5155 include boost, flyback and SEPIC regulators. This design guide focuses on how to configure and design the LM5155 as a boost regulator. This procedure is generic and focuses on selecting the correct components for boost operation. The design example was used to create the LM5155EVM-BST evaluation model and the results are presented in LM5155EVM-BST User's Guide. For typical applications, the LM5155 Boost Controller Quick Start Calculator can be used to efficiently complete the calculations described in this report.

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1 LM5155 Design Example

This design guide follows typical design procedures and calculations to implement a non-synchronous boost controller. The design example uses an unregulated 12V rail (6V - 18V) to produce a regulated 24V of up to 2A load current. A switching frequency of 440kHz is selected to avoid interference in the AM band (530kHz to 1.8MHz). The minimum supply voltage is selected to be 6V, which is similar to many automotive start-stop applications. Section 3 details the component selection based on the general design parameters shown in Table 1.

2 Example Application

Table 1 indicates the parameters for the example application.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{SUPPLY}}$</td>
<td>6V to 18 V</td>
</tr>
<tr>
<td>$V_{\text{LOAD}}$</td>
<td>24V</td>
</tr>
<tr>
<td>$I_{\text{LOAD}}$</td>
<td>2A</td>
</tr>
<tr>
<td>$f_{\text{SW}}$</td>
<td>440kHz</td>
</tr>
<tr>
<td>$\eta$ (estimated efficiency)</td>
<td>90%</td>
</tr>
</tbody>
</table>

3 Calculations and Component Selection

This section covers the equations specific to the LM5155 to implement a boost controller that operates in continuous conduction mode. Component selection is based on the example application described in Table 1.

3.1 Switching frequency

Selecting the proper switching frequency is the first step in the design process. Higher switching frequencies yield a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the total efficiency regulator. Higher efficiency is achieved by selecting a relatively lower switching frequency but requires physically larger components. Harmonics of the switching frequency should be considered in designs that have strict EMC requirements. Equation 1 is used to set the frequency of the oscillator in the LM5155. The example application is selected to have a switching frequency of 440kHz

$$R_T = \frac{2.21 \times 10^{10}}{f_{\text{SW}}} - 955 = \frac{2.21 \times 10^{10}}{440kHz} - 955 = 49.2k\Omega$$

A standard value of 49.9kΩ is chosen for $R_T$.

Note that the internal oscillator of the LM5155 can be synchronized to an external clock as described in the datasheet. The LM5155 has a maximum duty cycle limit that is frequency dependent. See the LM5155 datasheet for details on step-up ratio limitations.

3.2 Inductor Calculation

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the right-half plane zero frequency ($\omega_{Z\text{-RHP}}$) of the control loop. Finding a balance between these three parameters helps simplify the rest of the design process.

- The inductor current ripple ratio is selected to balance the copper loss and core loss of the inductor. As the relative ripple current increases; the core loss increases and the copper loss decreases
- The falling slope of the inductor current should be small enough to prevent sub-harmonic oscillation. A relatively larger inductance value results in a smaller falling slope of the inductor current. This increases the impact internal slope compensation provided by the LM5155.
- The right-half plane zero should be placed at high frequency, allowing a higher crossover frequency of the control loop. As the relative inductance value decrease the right-half plane zero frequency
increases.

A maximum ripple ratio between 30% and 70% results in a good balance between the power loss of the inductor, the down slope of the inductor current and the right-half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33% \((D_{\text{max}, \Delta I_L}=0.33)\). In the case that the application specification does not result in a duty cycle of 33% the maximum supply voltage is used to calculate the maximum ripple ratio. Use Equation 2 to calculate the supply voltage that results in a duty cycle of 33% \((D=0.33)\).

\[
V_{\text{SUPPLY, max}, \Delta I_L} = V_{\text{LOAD}} \cdot (1 - D) = 24V \cdot (1 - 0.33) = 16.08V
\]

where

- \(D_{\text{max}, \Delta I_L}\) is the duty cycle where the maximum inductor ripple current occurs

Knowing \(V_{\text{SUPPLY, max}}\) the desired ripple ratio and the switching frequency, use Equation 3 to calculate the inductor value.

\[
L_{\text{M, calc}} = \frac{V_{\text{SUPPLY}} - \Delta I_L}{I_{\text{SUPPLY}} \cdot \Delta I_L} \cdot D = \frac{16.08V}{2.985A \cdot 0.6 \cdot 440kHz} \cdot 0.33 = 6.734\mu\text{H}
\]

where

- \(D\) is the duty cycle where the maximum inductor ripple current occurs
- \(\Delta I_L\) is the ripple ratio of inductor ripple current to average supply current

A standard value of 6.8\(\mu\text{H}\) is selected for the value of \(L_M\). The maximum peak inductor current occurs when the supply voltage is at the minimum value, \(V_{\text{SUPPLY, min}}\), and the maximum load current \(I_{\text{LOAD, max}}\). The peak inductor current is calculated using Equation 4.

\[
I_{\text{L, peak, max}} = \frac{V_{\text{LOAD}} \cdot I_{\text{OUT}} + 1}{2 \cdot V_{\text{SUPPLY}} \cdot \eta} + \frac{1}{2} \cdot \frac{V_{\text{SUPPLY}} \cdot D}{L_{\text{M}} \cdot f_{SW}} = \frac{24V \cdot 2A}{6V \cdot 0.9} + \frac{1}{2} \cdot \frac{6V \cdot 0.75}{6.8\mu\text{H} \cdot 440kHz} = 9.641A
\]

where

- \(\eta\) is the estimated efficiency at the minimum supply voltage and maximum load current

The peak inductor current is used to properly size the current sense resistor, \(R_S\).

### 3.3 Current Sense Resistor Calculation

Selecting the switch current sense network components is described in the following section. Figure 1 shows the four components that make up the current sense network of the LM5155. \(R_S\) is the current sense resistor. This resistor senses the switch current, and also sets the peak current limit of the inductor current. \(R_F\) and \(C_F\) form a low pass filter. This filter helps minimize high frequency noise on the current sense signal. \(R_{SL}\) sets the external slope compensation and is optional. In some applications where the internal slope compensation is not large enough \(R_{SL}\) will be required.

![Figure 1. LM5155 Current Sense Network](image-url)
3.3.1  Current Sense Resistor and Slope Compensation Resistor Selection

The current sense resistor is selected to avoid current limiting during the minimum supply voltage, $V_{\text{SUPPLY\_min}}$, and the maximum load current, $I_{\text{LOAD\_max}}$. Due to component tolerances and power loss of the regulator, the peak current limit should be set some margin above the calculated peak inductor current. A margin of 20% ($M_{I\_\text{LIMIT}}=0.2$) is a good starting point. Equation 5 is used to calculate the desired peak inductor current limit value. In this design example, $M_{I\_\text{LIMIT}}$ is selected to be 20%.

\[
I_{\text{L\_PEAK\_LIMIT\_SET}} = (1 + M_{I\_\text{LIMIT}}) \cdot I_{\text{L\_PEAK\_MAX}} = (1 + 0.2) \cdot 9.641A = 11.569A
\]

where

- $I_{\text{L\_PEAK\_MAX}}$ is the maximum peak inductor current

Selecting the correct current sense resistor is an iterative process. The first step is to calculate the maximum current sense resistor, assuming that no external slope compensation is required ($R_{\text{SL}} = 0 \, \Omega$), using Equation 6.

\[
R_{\text{S\_MAX}} = 1.66 \frac{V_{\text{SL}} \cdot L \cdot f_{\text{SW}}}{V_{\text{LOAD}} - V_{\text{SUPPLY\_MIN}}} = 1.66 \frac{40mV \cdot 6.8\mu\text{H} \cdot 440kHz}{24V - 6V} = 11.08m\Omega
\]

where

- $V_{\text{SL}}$ is the internal fixed internal slope compensation of the LM5155

Assuming that no external slope compensation is required, the current sense resistor value is calculated using Equation 7.

\[
R_{\text{S\_wo\_sl}} = \frac{V_{\text{CLTH}}}{I_{\text{L\_PEAK\_LIMIT\_SET}}/11.569A} = \frac{100mV}{11.569A} = 8.644m\Omega
\]

where

- $V_{\text{CLTH}}$ is the current limit threshold of the LM5155

If the calculated $R_{\text{S\_wo\_sl}}$ resistance value is less than the $R_{\text{S\_MAX}}$ resistance value, the $R_{\text{S\_wo\_sl}}$ is selected for the current sense resistor value ($R_{\text{S}}$). If the calculated $R_{\text{S\_wo\_sl}}$ resistance value is greater than the calculated $R_{\text{S\_MAX}}$ resistance value, there are two approaches to take; decrease the current sense resistor value or add external slope compensation.

- Decreasing the current sense resistor increases the effectiveness of the internal slope compensation. With no external slope compensation the peak inductor current limit will be constant regardless of the duty cycle. A lower current sense resistor results in a larger inductor peak current limit value, which increases the required saturation current rating of the inductor.

- Adding external slope compensation. The peak inductor current limit varies with supply voltage when external slope compensation is added.

External slope compensation is added by setting $R_{\text{SL}}$ to a non-zero value less than 1kΩ. In applications where external slope compensation is added, $R_{\text{S}}$ is calculated using Equation 8.

\[
R_{\text{S\_w\_sl}} = \frac{L \cdot f_{\text{SW}} \cdot (V_{\text{CLTH}} + D \cdot V_{\text{SLOPE}})}{D \cdot 0.833 \cdot (V_{\text{LOAD}} - V_{\text{SUPPLY\_MIN}}) + I_{\text{L\_PEAK\_LIMIT\_SET}} \cdot L \cdot f_{\text{SW}}}
\]

\[
R_{\text{S\_w\_sl}} = \frac{6.8\mu\text{H} \cdot 440kHz \cdot (100mV + 0.75 \cdot 40mV)}{0.75 \cdot 0.833 \cdot (24V - 6V) + 11.569A \cdot 6.8\mu\text{H} \cdot 440kHz} = 8.481m\Omega
\]

$R_{\text{SL}}$ is calculated using Equation 9.

\[
R_{\text{SL}} = \frac{V_{\text{CLTH}} - I_{\text{L\_PEAK\_LIMIT\_SET}} \cdot R_{\text{S\_w\_sl}}}{\frac{I_{\text{SLOPE}} \cdot D}{30\mu\text{A} \cdot 0.75}} = \frac{100mV - 11.569A \cdot 8.481m\Omega}{30\mu\text{A} \cdot 0.75} = 83.452\Omega
\]

where

- $I_{\text{SLOPE}}$ is the slope compensation source of the LM5155
- $D$ is the duty cycle at the minimum supply voltage
If the calculated $R_{SL}$ value exceeds the maximum value of the 1kΩ, the down slope of the sensed inductor current needs to be reduce. To reduce the down slope of the inductor current, the inductance value of $L_m$ must be increased. If the $L_m$ inductance value is changed the current sense resistor calculations must be recalculated.

For this design example a current sense resistor value is selected to be 8mΩ ($R_S$), which is the nearest standard resistor value to the calculated value in Equation 7. This value is selected to keep from triggering current limit protection during load transients. No external slope compensation is required and $R_{SL}$ is selected to be 0Ω. The peak inductor current limit is calculated using Equation 10

$$I_{L_{PEAK LIMIT}} = \frac{V_{CLTH} - I_{SLOPE} \cdot R_{SL} \cdot D}{R_S} \quad \text{IL_{PEAK LIMIT}} = \frac{100mV - 30\mu A \cdot 0Ω \cdot 0.75}{8\Omega} = 12.5A$$

(10)

The peak inductor current limit is constant, regardless of the supply voltage, because there is no external slope compensation. For this design the inductor saturation current rating must be greater than 12.5A.

### 3.3.2 Current Sense Resistor Filter Calculation

For all designs it is recommended to add the low pass filter to the current sense signal. $R_F$ and $C_F$ implement this low pass filter as shown in Figure 1. The filter is added to help mitigate the impact of the leading edge spike on the current sense signal. $R_F$ is selected to be between 10Ω and 200Ω. For this design $R_F$ is selected to be 100Ω. $C_F$ must be less than the value specified in Equation 11 to ensure proper operation.

$$C_F < \frac{1 - D}{3 \cdot R_F \cdot f_{SW}} = \frac{1 - 0.75}{3 \cdot 100 \cdot 440kHz} = 1.89nF$$

(11)

$C_F$ is selected to be 100pF. Due to the delay of the low pass filter, the current limit is not valid when $V_{SUPPLY}$ is greater than a given voltage calculated in. For this design the current limit is valid for the entire supply voltage range. Equation 12 is used to calculate this value.

$$V_{SUPPLY\_IL\_MAX} = V_{LOAD} \cdot (1 - 2 \cdot C_F \cdot R_F \cdot f_{SW}) = 24V \cdot (1 - 2 \cdot 100pF \cdot 100Ω \cdot 440kHz) = 23.78V$$

(12)

### 3.4 Inductor Selection

$R_S$, the inductor must be selected according to three parameters; calculated inductance value ($L_m$), RMS inductor current at the minimum supply voltage and the peak inductor current limit ($I_{L_{PEAK LIMIT}}$) set by the current sense resistor ($R_S$).

- The inductance value is selected to be 6.8µH. This is a standard value that is produced by most magnetic vendors.
- The RMS current of the inductor can be estimated by calculating the average inductor current ($I_{L_{AVG}}$) and is approximately equal to the average supply current. The average inductor current is estimated to be 8.89A when $V_{SUPPLY} = 6V$. The inductor RMS current rating should be higher than calculated average inductor current and keep the inductor temperature rise to a reasonable level based on the application.
- The saturation current rating of the inductor should be larger than the calculated $I_{L_{PEAK LIMIT}}$ value, 12.5A. If the inductor becomes saturated, proper operation of the regulator is not guaranteed.

For this design example, the inductor is selected to have an inductance value of 6.8µH, 20°C component temperature rise at an RMS of 14A, and a saturation current limit of 21.8A.

### 3.5 Diode Selection

The diode must be rated to handle the average load current, plus some margin, while being able to dissipate the conduction losses. The voltage rating of the diode must be greater than the load voltage, $V_{LOAD}$. Selecting a schottky diode is recommended due to the small reverse recovery time and smaller forward voltage drop with respect to a standard fast recovery diode. For this design a 60V reverse voltage, 10A average forward current schottky diode is selected. The conducted power loss of this diode is calculated in Equation 13.
Calculations and Component Selection

\[
P_{\text{D, con}} = V_F \cdot (1 - D) \cdot I_{\text{SUPPLY}} = 480\text{mV} \cdot (1 - 0.75) \cdot \frac{24\text{V} \cdot 2\text{A}}{6\text{V}} = 0.96\text{W}
\]

where

- \( V_F \) is the forward voltage drop of the diode

\[ (13) \]

### 3.6 MOSFET Selection

MOSFET selection focuses on power dissipation and voltage rating. Power dissipation of MOSFET is composed of two different parts, conduction losses and switching losses. Conduction losses are dominated by the \( R_{\text{DS(ON)}} \) parameter of the MOSFET. Switching losses occur during the rise and fall time of the switch node, when the N-channel MOSFET is turning on and turning off. During the rise time and fall time, current and voltage are present in the channel of the MOSFET. The longer the rise and fall time of the switch node the higher the switching losses. Selecting a MOSFET with minimal parasitic capacitances lowers the switching losses. Ideally, conduction losses and switching losses should be equal during maximum load current and minimum supply voltage. details how to calculate the conduction and switching losses of the MOSFET.

The total gate charge \( (Q_{\text{G, total}}) \) must not be large enough to place the internal VCC regulator into current limit. The \( Q_{\text{G, total}} \) for a given MOSFET should be known. Equation 14 provides the maximum \( Q_{\text{G, total}} \) of the MOSFET.

\[
Q_{\text{G, total}} < \frac{35\text{mA}}{f_{\text{SW}}}
\]

The drain to source break down voltage rating on the MOSFET needs to be higher than the load voltage, plus some margin, due to voltage spike on the switch node. The break down voltage rating should be at least 10V higher than \( V_{\text{LOAD}} \) plus \( V_F \). \( V_F \) is the forward voltage of the rectifying diode.

For this design, a 40V MOSFET with low \( R_{\text{DS(ON)}} \) low threshold voltage is selected.

### 3.7 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. During the on time of the switch, the voltage across the output capacitor bank decreases. The output capacitor is appropriately sized based on the required capacitive voltage ripple during the on-time of the MOSFET.

Using the required \( V_{\text{LOAD}} \) ripple requirement, 100mV, Equation 15 is used to calculate the minimum output capacitance. The maximum on-time of the switch occurs at the minimum supply voltage. In practice, ceramic capacitors are added to reduce the total output capacitor bank ESR, reducing the high frequency load voltage ripple. Electrolytic capacitors provide bulk capacitance that is relatively constant over DC voltage ranges when compared to ceramic capacitors.

\[
C_{\text{OUT, min}} = \frac{I_{\text{LOAD}} \cdot D}{f_{\text{SW}} \cdot \Delta V_{\text{LOAD}}} = \frac{2\text{A} \cdot 0.75}{440\text{kHz} \cdot 100\text{mV}} = 14.206\mu\text{F}
\]

The output capacitor must be rated to handle the ripple current without being damaged or significantly reducing operating life. The maximum output ripple current is estimated using Equation 16. Ceramic capacitors generally have a relatively high RMS ripple current rating and are used to increase the total RMS current rating of the output capacitor bank.

\[
I_{\text{RMS, COUT}} = \sqrt{(1 - D) \cdot \frac{I_{\text{LOAD}}^2 \cdot D}{(1 - D)^2} + \frac{\Delta I^2}{3}} = \sqrt{(1 - 0.75) \cdot \frac{2\text{A}^2 \cdot 0.75}{(1 - 0.75)^2} + \frac{1.504\text{A}^2}{3}} = 3.49\text{A}
\]

For this design, a total output capacitance of 200\( \mu \text{F} \) is selected. The capacitor bank ESR \( (R_{\text{ESR}}) \) is estimated to be around 2m\( \Omega \). The output capacitance and low \( R_{\text{ESR}} \) value help minimize the voltage drop during load transients.
3.8 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. For this design and input capacitance of 100µF is selected. Assuming that low ESR, high quality ceramic capacitor are used, Equation 17 is used to calculate the maximum supply voltage ripple based on input capacitance of 100µF.

\[ \Delta V_{\text{supply}} = \frac{V_{\text{load}}}{32 \cdot L_m \cdot C_{\text{IN}} \cdot f_{\text{sw}}^2} = \frac{24V}{32 \cdot 6.8\mu H \cdot 100\mu F \cdot 440kHz^2} = 5.6mV \] (17)

The supply voltage ripple is a function of the load impedance of the supply voltage power supply. If the impedance of the input supply is large more input capacitance is required to minimize the ripple.

3.9 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating voltage of the regulator. Two levels must be specified; the voltage the LM5155 starts operation (V_{\text{supply(on)}}) and the voltage the LM5155 enters stand-by mode (V_{\text{supply(off)}}). In this example, V_{\text{supply(on)}} voltage is 5.8V and the V_{\text{supply(off)}} is 5.4V. Using Equation 18, the top UVLO resistor (R_{\text{UVLOT}}) is calculated.

\[ R_{\text{UVLOT}} = \frac{0.967 \cdot (V_{\text{supply(on)}} - V_{\text{supply(off)}})}{5\mu A} = \frac{0.967 \cdot 5.8V - 5.5V}{5\mu A} = 21.33k\Omega \] (18)

A standard value of 21kΩ is selected for R_{\text{UVLOT}}. Using Equation 19 the top UVLO resistor (R_{\text{UVLOB}}) is calculated.

\[ R_{\text{UVLOB}} = \frac{1.5V \cdot R_{\text{UVLOT}}}{V_{\text{supply(on)}} - 1.5V} = \frac{1.5V \cdot 21k\Omega}{5.8V - 1.5V} = 7.32k\Omega \] (19)

A standard value of 7.3kΩ is selected for R_{\text{UVLOB}}

3.10 Soft-Start Capacitor Selection

The soft-start capacitor is used to minimize and overshoot on the load voltage during the start-up of the regulator. Equation 20 is used to calculate the minimum recommended soft-start capacitor value.

\[ C_{\text{SS}} > \frac{10\mu A \cdot V_{\text{load}} \cdot C_{\text{OUT}}}{I_{\text{load}}} = \frac{10\mu A \cdot 24V \cdot 200\mu F}{2A} = 24nF \] (20)

For this design a CSS value of 100nF is selected to minimize any overshoot on the load voltage during start-up.

3.11 Feedback Resistor Selection

The feedback resistors (R_{\text{FBT}}, R_{\text{FBB}}) set the regulated load voltage by comparing the scaled voltage to the internal voltage reference. To help limit the bias current of the feedback resistor divider, R_{\text{FBT}} is selected to be 47kΩ. Equation 21 is used to calculate the value of R_{\text{FBB}}.

\[ R_{\text{FBB}} = \frac{R_{\text{FBT}}}{V_{\text{reference}}} - 1 \cdot \frac{24V}{1V} - 1 = 2.04k\Omega \] (21)

R_{\text{FBB}} is selected to be 2kΩ

3.12 Control Loop Compensation

There are many different strategies to set the crossover frequency of the control loop, and placing the pole and zero of the error amplifier. In this section a general technique is described to adequately stabilize the control loop for a peak current mode controlled boost regulator in continuous conduction mode operation. A type II compensation network is implemented as show in Figure 2. Type II compensation provides a programmable low frequency zero and programmable high frequency pole. For a detailed model of the control loop see Section 5. The loop compensation selection process is broken down into a number of distinct steps described in the following sections.
### 3.12.1 Select the Loop Crossover Frequency ($f_{CROSS}$)

The crossover frequency of the loop is either selected to be $1/10$th the switching frequency or $1/5$th the right-half plane zero frequency, whichever is lower. Equation 22 shows the calculation for $1/10$th the switching frequency. Equation 23 shows how to calculate the $1/5$th the right half plane zero frequency.

$$f_{CROSS} = \frac{f_{SW}}{10} = \frac{10}{440kHz} = 44kHz$$

$$f_{CROSS} = \frac{f_{Z\_RHP}}{5} = \frac{R_{LOAD} \cdot (D')^2}{5 \cdot 2 \cdot \pi \cdot L_m} = \frac{12\Omega \cdot (0.25)^2}{5 \cdot 2 \cdot \pi \cdot 6.8\mu H} = 3.5kHz$$

where

- $D'$ is $(1 - D)$ for the minimum supply voltage
- $R_{LOAD}$ is the load resistance equal to $V_{LOAD}/I_{LOAD}$

The crossover frequency is selected to be $1/5$th the right half plane zero frequency, 3.5kHz

### 3.12.2 Determine Required $R_{COMP}$

The $R_{COMP}$ value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Knowing the desired loop crossover frequency, 3.5kHz, $R_{COMP}$ is calculated using Equation 24.

$$R_{COMP} = \frac{2 \cdot \pi \cdot C_{OUT} \cdot R_{LOAD} \cdot f_{CROSS}^2 \cdot G_{COMP} \cdot g_m \cdot V_{SUPPLY\_min}}{V_{COMP}} = \frac{2 \cdot \pi \cdot 200\mu F \cdot 8\Omega \cdot 24V \cdot 3.5kHz}{G_{COMP} \cdot g_m \cdot 6V} = 11.93k\Omega$$

where

- $g_m$ is the transconductance of the error amplifier, 2mA/V
- $G_{COMP}$ is COMP to PWM gain, 0.142V/V

$R_{COMP}$ is selected to be 11.3kΩ. Decreasing the $R_{COMP}$ resistance value lowers the crossover frequency but helps ensure the control loop remains stable over the specified supply voltage range.

### 3.12.3 Determine Required $C_{COMP}$

The $R_{COMP}$ resistor and $C_{COMP}$ capacitor set the low frequency zero of the compensation network resulting in a phase boost. Placement of this zero frequency largely impacts the transient response of the control loop. A good strategy is placing the zero directly in between the crossover frequency ($f_{CROSS}$) and the low frequency pole of the plant. Equation 25 places the low frequency zero of error amplifier $a$ the geometric mean of $f_{CROSS}$ and low frequency pole of the plant ($\omega_{\_LF}$). For this design the desired zero location is 682Hz.

$$f_{Z\_EA} = \sqrt{f_{CROSS} \cdot \frac{2}{2\pi \cdot C_{OUT} \cdot R_{LOAD}}} = \sqrt{3.5kHz \cdot \frac{2}{2\pi \cdot 200\mu F \cdot 12\Omega}} = 682Hz$$

With the zero frequency selected, Equation 26 produces the value of $C_{COMP}$.
\[ C_{\text{COMP}} = \sqrt{\frac{C_{\text{OUT}} \cdot R_{\text{LOAD}}}{4 \cdot \pi \cdot R_{\text{COMP}}^2 \cdot f_{\text{CROSS}}}} = \sqrt{\frac{200 \mu \text{F} \cdot 12 \Omega}{4 \cdot \pi \cdot 11.3 \text{k} \Omega^2 \cdot 3.5 \text{kHz}}} = 20.64 \text{nF} \]  

\[ (26) \]

\[ C_{\text{COMP}} \text{ is chosen to be 22nF.} \]

### 3.12.4 Determine Required \( C_{\text{HF}} \)

The \( C_{\text{HF}} \) capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin achieved. It is recommended to set the pole frequency between or between the RHP zero \( (\omega_{Z_{RHP}}) \) and half the switching frequency. Equation 27 is used to calculate the value of \( C_{\text{HF}} \).

\[ C_{\text{HF}} = \frac{C_{\text{COMP}} \cdot L_{\text{M}}}{C_{\text{COMP}} \cdot D^2 \cdot R_{\text{OUT}} \cdot R_{\text{COMP}} - L_{\text{M}}} = \frac{22 \text{nF} \cdot 6.8 \mu \text{H}}{22 \text{nF} \cdot 0.5^2 \cdot 12 \Omega \cdot 11.3 \text{k} \Omega - 6.8 \mu \text{H}} = 200 \text{pF} \]

\[ (27) \]

\[ C_{\text{HF}} \text{ is chosen to be 220pF.} \]

### 3.13 Efficiency Estimation

The total loss of the boost converter \( (P_{\text{TOTAL}}) \) can be expressed as the sum of the losses in the device \( (P_{\text{IC}}) \), MOSFET power losses \( (P_{\text{Q}}) \), diode power losses \( (P_{\text{D}}) \), inductor power losses \( (P_{\text{L}}) \), and the loss in the sense resistor \( (P_{\text{RS}}) \).

\[ P_{\text{TOTAL}} = P_{\text{IC}} + P_{\text{Q}} + P_{\text{D}} + P_{\text{L}} + P_{\text{RS}} [\text{W}] \]

\[ (28) \]

\[ P_{\text{IC}} \text{ can be separated into gate driving loss} (P_{\text{G}}) \text{ and the losses caused by quiescent current} (P_{\text{IQ}}). \]

\[ P_{\text{IC}} = P_{\text{G}} + P_{\text{IQ}} [\text{W}] \]

\[ (29) \]

Each power loss is approximately calculated as follows:

\[ P_{\text{G}} = O_{\text{G}\text{(@ VCC)}} \times V_{\text{BIAS}} \times F_{\text{SW}} [\text{W}] \]

\[ (30) \]

\[ P_{\text{IQ}} = V_{\text{BIAS}} \times I_{\text{BIAS}} [\text{W}] \]

\[ (31) \]

\[ I_{\text{BIAS}} \text{ values in each mode can be found in the LM5155 datasheet.} \]

\[ P_{\text{Q}} \text{ can be separated into switching loss} (P_{\text{Q(SW)}}) \text{ and conduction loss} (P_{\text{Q(COND)}}). \]

\[ P_{\text{Q}} = P_{\text{Q(SW)}} + P_{\text{Q(COND)}} [\text{W}] \]

\[ (32) \]

Each power loss is approximately calculated as follows:

\[ P_{\text{Q(SW)}} = 0.5 \times (V_{\text{LOAD}} + V_{F}) \times I_{\text{SUPPLY}} \times (t_{R} + t_{F}) \times F_{\text{SW}} \]

\[ (33) \]

\[ t_{R} \text{ and } t_{F} \text{ are the rise and fall times of the low-side N-channel MOSFET device.} \]

\[ I_{\text{SUPPLY}} \text{ is the input supply current of the boost converter.} \]

\[ P_{\text{Q(COND)}} = D \times I_{\text{SUPPLY}}^2 \times R_{\text{DS(ION)}} [\text{W}] \]

\[ (34) \]

\[ R_{\text{DS(ION)}} \text{ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the} \]

\[ R_{\text{DS(ION)}} \text{ increase due to self-heating.} \]

\[ P_{\text{D}} \text{ can be separated into diode conduction loss} (P_{\text{VF}}) \text{ and reverse recovery loss} (P_{\text{RR}}). \]

\[ P_{\text{D}} = P_{\text{VF}} + P_{\text{RR}} [\text{W}] \]

\[ (35) \]

Each power loss is approximately calculated as follows:

\[ P_{\text{VF}} = (1 - D) \times V_{F} \times I_{\text{SUPPLY}} [\text{W}] \]

\[ (36) \]

\[ P_{\text{RR}} = V_{\text{LOAD}} \times Q_{\text{RR}} \times F_{\text{SW}} [\text{W}] \]

\[ (37) \]

\[ Q_{\text{RR}} \text{ is the reverse recovery charge of the diode and is specified in the diode datasheet. Reverse recovery} \]

\[ \text{characteristics of the diode strongly affect efficiency, especially when the load voltage is high.} \]

\[ P_{\text{L}} \text{ is the sum of DCR loss} (P_{\text{DCR}}) \text{ and AC core loss} (P_{\text{AC}}). \text{ DCR is the DC resistance of inductor which is} \]

\[ \text{mentioned in the inductor data sheet.} \]

\[ P_{\text{L}} = P_{\text{DCR}} + P_{\text{AC}} [\text{W}] \]

\[ (38) \]
Each power loss is approximately calculated as follows:

\[
P_{\text{DCR}} = I_{\text{SUPPLY}}^2 R_{\text{DCR}} \text{[W]} \tag{39}
\]
\[
P_{\text{AC}} = K \times \Delta I \times F_{\text{SW}} \alpha \text{[W]} \tag{40}
\]
\[
\Delta I = \frac{V_{\text{SUPPLY}} \times D \times 1}{F_{\text{SYNC}}} \times \frac{L_{M}}{R_{G}} \tag{41}
\]

\( \Delta I \) is the peak-to-peak inductor current ripple. \( K, \alpha, \) and \( \beta \) are core dependent factors which can be provided by the inductor manufacturer.

\( P_{\text{RS}} \) is calculated as follows:

\[
P_{\text{RS}} = D \times I_{\text{SUPPLY}}^2 \times R_{S} \text{[W]} \tag{42}
\]

Efficiency of the power converter can be estimated as follows:

\[
\text{Efficiency} = \frac{V_{\text{LOAD}} \times I_{\text{LOAD}}}{P_{\text{TOTAL}} + V_{\text{LOAD}} \times I_{\text{LOAD}}} \times 100\% \tag{43}
\]

4 Component Selection Summary

Please see the *LM5155EVM-BST User's Guide* for more testing results.
Figure 4. Efficiency vs $I_{\text{OUT}}$

Figure 5. Control Loop Response $V_{\text{SUPPLY}} = 12V$, $I_{\text{LOAD}} = 2A$

Figure 6. Load Step: $I_{\text{LOAD}}$ 1A to 2A, $V_{\text{SUPPLY}} = 12V$

Figure 7. Thermal Image: $V_{\text{SUPPLY}} = 6V$, $I_{\text{LOAD}} = 2A$
Figure 8. LM5155EVM-BST Schematic
Table 2. List of Materials

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR</th>
<th>QTY.</th>
<th>SPECIFICATION</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rr</td>
<td>1</td>
<td>RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW060349K9FKEA</td>
</tr>
<tr>
<td>RREF</td>
<td>1</td>
<td>RES, 22.0 k, 1%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603FR-0722KL</td>
</tr>
<tr>
<td>RFB</td>
<td>1</td>
<td>RES, 2.43 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW06032K43K4FKEA</td>
</tr>
<tr>
<td>LMI</td>
<td>1</td>
<td>Shielded, Composite, 1.2 uH, 26.3 A, 0.0025 ohm, AEC-Q200 Grade 1, SMD</td>
<td>Coilcraft</td>
<td>XAL1060-122MEB</td>
</tr>
<tr>
<td>Rs</td>
<td>1</td>
<td>RES, 0.003, 1%, 3 W, AEC-Q200 Grade 0, 2512 WIDE</td>
<td>Susumu Co Ltd</td>
<td>KRL6432E-M-R003-F-T1</td>
</tr>
<tr>
<td>RsL</td>
<td>1</td>
<td>RES, 0, 5%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603JR-070RL</td>
</tr>
<tr>
<td>COUT1</td>
<td>3</td>
<td>CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, 1210</td>
<td>TDK</td>
<td>C3225X7R147925AB</td>
</tr>
<tr>
<td>COUT2 (Bulk)</td>
<td>1</td>
<td>CAP, Polymer Hybrid, 100 uF, 50 V, +/- 20%, 28 ohm, 10x10 SMD</td>
<td>Panasonic</td>
<td>EEH2C1H101P</td>
</tr>
<tr>
<td>CNT1</td>
<td>6</td>
<td>CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1210</td>
<td>MuRata</td>
<td>GRM32ER71H106KA12L</td>
</tr>
<tr>
<td>CNT2 (Bulk)</td>
<td>1</td>
<td>CAP, Polymer Hybrid, 100 uF, 50 V, +/- 20%, 28 ohm, 10x10 SMD</td>
<td>Panasonic</td>
<td>EEH2C1H101P</td>
</tr>
<tr>
<td>Q1</td>
<td>1</td>
<td>MOSFET, N-CH, 60 V, 100 A, AEC-Q101, SOT669</td>
<td>Nexperia</td>
<td>BUK9Y6R0-60E.115</td>
</tr>
<tr>
<td>D1</td>
<td>1</td>
<td>Schottky, 60 V, 10 A, AEC-Q101, CFP15</td>
<td>Nexperia</td>
<td>PME600V100EPDZ</td>
</tr>
<tr>
<td>RCOMP</td>
<td>1</td>
<td>RES, 22 k, 1%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603FR-072K21L</td>
</tr>
<tr>
<td>CCOMP</td>
<td>1</td>
<td>CAP, CERM, 0.047 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603</td>
<td>MuRata</td>
<td>GCM188R71E473K3A7D</td>
</tr>
<tr>
<td>CHF</td>
<td>1</td>
<td>CAP, CERM, 2200 pF, 25 V, +/- 10%, X7R, 0603</td>
<td>MuRata</td>
<td>GRM188R71E222K01D</td>
</tr>
<tr>
<td>RUVL0T</td>
<td>1</td>
<td>RES, 24.9 k, 1%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603FR-0724K9L</td>
</tr>
<tr>
<td>RUVL0B</td>
<td>1</td>
<td>RES, 76.8 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW060376K8FKEA</td>
</tr>
<tr>
<td>RUVL0S</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>CFB</td>
<td>1</td>
<td>CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603</td>
<td>TDK</td>
<td>C1608X7R104K080AA</td>
</tr>
<tr>
<td>DS</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>RG</td>
<td>1</td>
<td>RES, 0, 5%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603JR-070RL</td>
</tr>
<tr>
<td>CG</td>
<td>1</td>
<td>CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0603</td>
<td>Kemet</td>
<td>C0603C101FSACTU</td>
</tr>
<tr>
<td>RC</td>
<td>1</td>
<td>RES, 100, 1%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603FR-07100RL</td>
</tr>
<tr>
<td>RSM</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>CSM</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>RBAS</td>
<td>1</td>
<td>RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>Panasonic</td>
<td>ERJ-3GEOYR00V</td>
</tr>
<tr>
<td>CBAS</td>
<td>1</td>
<td>CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0603</td>
<td>Samsung Electro-Mechanics</td>
<td>CL0B103KB8NCNC</td>
</tr>
<tr>
<td>VC</td>
<td>1</td>
<td>CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603</td>
<td>MuRata</td>
<td>GCM188R71C0105MA64D</td>
</tr>
<tr>
<td>RG</td>
<td>1</td>
<td>RES, 24.9 k, 1%, 0.1 W, 0603</td>
<td>Yageo America</td>
<td>RC0603FR-0724K9L</td>
</tr>
</tbody>
</table>

5 Small Signal Frequency Analysis

This section provides detailed equations used to model the control loop when the LM5155 is configured as a boost regulator. These equations are only valid when the regulator is operating in continuous conduction mode. The simplified formulas allow for quick evaluation of the control loop, but lose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

5.1 Boost Regulator Modulator Modeling

These equations model the plant of a peak current mode boost regulator in continuous conduction mode.
Table 3. Control Loop Equations

<table>
<thead>
<tr>
<th>Modulator Equations</th>
<th>Simplified Formula</th>
<th>Comprehensive Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulator Transfer</td>
<td>$\hat{V}<em>\text{LOAD}(s) = A_M \left( 1 + \frac{s}{\omega_Z</em>{\text{ESR}}} \right) \left( 1 + \frac{s}{\omega_{Z_{\text{RHP}}}} \right)$</td>
<td>$\hat{V}<em>\text{COMP}(s) = A_M \left( 1 + \frac{s}{\omega_Z</em>{\text{ESR}}} \right) \left( 1 + \frac{s}{\omega_{Z_{\text{RHP}}}} \right)$</td>
</tr>
<tr>
<td>Function</td>
<td></td>
<td>(44)</td>
</tr>
<tr>
<td>Modulator DC Gain</td>
<td>$A_M = G_{\text{COMP}} \frac{R_{\text{LOAD}}}{A_{\text{CS}} \cdot R_S} \times \frac{D'}{2}$</td>
<td>(45)</td>
</tr>
<tr>
<td>RHP Zero</td>
<td>$\omega_{Z_{\text{RHP}}} = \frac{R_{\text{LOAD}} (D')^2}{L_M}$</td>
<td></td>
</tr>
<tr>
<td>ESR Zero</td>
<td>$\omega_{Z_{\text{ESR}}} = \frac{1}{C_{\text{OUT}} \cdot R_{\text{ESR}}}$</td>
<td>(46)</td>
</tr>
<tr>
<td>Low Frequency Pole</td>
<td>$\omega_{p_{\text{LF}}} = \frac{2}{C_{\text{OUT}} \cdot R_{\text{LOAD}}}$</td>
<td>(47)</td>
</tr>
<tr>
<td>Sub-Harmonic Double</td>
<td>Not Considered</td>
<td>$\omega_n = \pi \cdot f_{\text{sw}}$</td>
</tr>
<tr>
<td>Pole</td>
<td></td>
<td>(49)</td>
</tr>
<tr>
<td>Quality Factor</td>
<td>Not Considered</td>
<td>$Q = \frac{1}{\pi \left[ D' \cdot \left( 1 + \frac{s_n}{s_h} \right) - \frac{1}{2} \right]}$</td>
</tr>
<tr>
<td>Slope Compensation</td>
<td>Not Considered</td>
<td>$s_n = (V_{\text{SLOPE}} + l_{\text{SLOPE}} \cdot R_{\text{SL}}) \cdot f_{\text{sw}}$</td>
</tr>
<tr>
<td>Sensed Rising</td>
<td>Not Considered</td>
<td>$s_n = \frac{V_{\text{SUPPLY}} \cdot R_S \cdot A_{\text{CS}}}{L_M}$</td>
</tr>
<tr>
<td>Inductor Slope</td>
<td></td>
<td>(53)</td>
</tr>
</tbody>
</table>

5.2 Compensation Modeling

These equations model a type II compensation network implemented using a transconductance error amplifier.

Table 4. Compensation Modeling Equations

<table>
<thead>
<tr>
<th>Feedback Equations</th>
<th>Simplified Formula</th>
<th>Comprehensive Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback Transfer</td>
<td>$\hat{V}<em>\text{COMP}(s) = -A</em>{\text{FB}} \left( 1 + \frac{s}{\omega_{Z_{\text{EA}}}} \right)$</td>
<td>$\hat{V}<em>\text{LOAD}(s) = \left( 1 + \frac{s}{\omega</em>{p_{\text{EA}}}} \right) \cdot s$</td>
</tr>
</tbody>
</table>
Table 4. Compensation Modeling Equations (continued)

<table>
<thead>
<tr>
<th>Feedback Equations</th>
<th>Simplified Formula</th>
<th>Comprehensive Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback DC Gain</td>
<td>$A_{FB} = \frac{R_{FBB} \cdot g_m}{(R_{FBB} + R_{FBT}) \cdot C_{COMP}}$</td>
<td>$A_{FB} = \frac{R_{FBB} \cdot g_m}{(R_{FBB} + R_{FBT}) \cdot (C_{COMP} + C_{HF})}$</td>
</tr>
<tr>
<td>Low Frequency Zero</td>
<td>$\omega_{Z_EA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$</td>
<td>$\omega_{Z_EA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$</td>
</tr>
<tr>
<td>High Frequency Pole</td>
<td>$\omega_{P_EA} = \frac{1}{R_{COMP} \cdot C_{HF}}$</td>
<td>$\omega_{P_EA} = \frac{C_{COMP} + C_{HF}}{R_{COMP} \cdot C_{COMP} \cdot C_{HF}}$</td>
</tr>
<tr>
<td>Mid-band Gain</td>
<td>$G_{MID} = \frac{R_{COMP} \cdot R_{RFBB} \cdot g_m}{(R_{FBB} + R_{FBT})}$</td>
<td>$G_{MID} = \frac{C_{COMP} \cdot R_{COMP} \cdot R_{RFBB} \cdot g_m}{(C_{HF} + C_{COMP}) \cdot (R_{FBB} + R_{FBT})}$</td>
</tr>
</tbody>
</table>

5.3 Open Loop Modeling

These equations model the open loop transfer function of the control loop.

Table 5. Open Loop Modeling Equations

<table>
<thead>
<tr>
<th>Open Loop Equations</th>
<th>Simplified Formula</th>
<th>Comprehensive Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open Loop Transfer Function</td>
<td>$T(s) = A_m \cdot A_{FB} \cdot \left(1 + \frac{s}{\omega_{Z_LF}}\right) \cdot \left(1 - \frac{s}{\omega_{Z_HF}}\right) \cdot \left(1 + \frac{s}{\omega_{P_EA}}\right) \cdot \left(1 - \frac{s}{\omega_{P_EA}}\right)$</td>
<td>$T(s) = A_m \cdot A_{FB} \cdot \left(1 + \frac{s}{\omega_{Z_LF}}\right) \cdot \left(1 - \frac{s}{\omega_{Z_HF}}\right) \cdot \left(1 + \frac{s}{\omega_{P_EA}}\right) \cdot \left(1 - \frac{s}{\omega_{P_EA}}\right)$</td>
</tr>
<tr>
<td>Crossover Frequency</td>
<td>$f_{CROSS} = \frac{G_{COMP} \cdot V_{SUPPLY} \cdot g_m \cdot R_{COMP}}{2\pi \cdot A_{CS} \cdot R_{CS} \cdot C_{OUT} \cdot V_{LOAD}^2}$</td>
<td>Use Bode Plot</td>
</tr>
</tbody>
</table>
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