Application Note

How to Design an Isolated Flyback Using the LM5155

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ABSTRACT

The LM5155 is a versatile non-synchronous low-side, N-FET controller for switching regulators. the common configurations for the LM5155 include boost regulators, flyback regulators and SEPIC regulators. This design guide focuses on how to configure and design the LM5155 as an isolated flyback regulator. The procedure is generic and focuses on selecting the correct components for stable flyback operation. The design example follows the application specifications of the LM5155EVM-FLY evaluation module, the results are presented in the LM5155EVM-FLY User's Guide. For typical applications the LM5155 Flyback Controller Quick Start Calculator can be used to efficiently complete the calculations described in this report.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

This design guide follows typical design procedures and calculations to implement an isolated nonsynchronous flyback controller operating in continuous conduction mode. The design example uses an unregulated 24V rail (18V-36V) to produce a regulated 5 V of up to 4 A load current. A non-isolated auxiliary winding of 10V is selected to power the LM5155, lowering power dissipation in the LM5155. The switching frequency of 250kHz is selected to help minimize switching losses and conduction losses of the switching MOSFET. Section 3 details the component selection based on the general design parameters shown in Table 2-1.

2 Example Application

Table 2-1 indicates the design parameters for the example application.

Table 2-1. Design Parameters

Parameter	
V_{SUPPLY}	18 V to 36 V
V_{LOAD}	5 V
I_{LOAD}	4 A
V_{AUX}	10 V
I_{AUX}	20mA
P_{OUT_total}	20.2W
f_{SW}	250kHz

3 Calculations and Component Selection

This section covers the equations specific to the LM5155 to implement an isolated flyback controller that operates in continuous conduction mode. Component selection is based on the example application described in Table 2-1.

3.1 Switching Frequency

Selecting the switching frequency is the first step in the design process. Higher switching frequencies yield a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the efficiency of the regulator. Higher efficiency is achieved by selecting a relatively lower switching frequency but requires physically larger components. Harmonics of the switching frequency should be considered in designs that have strict EMC requirements. Equation 1 is used to set the frequency of the internal oscillator of the LM5155. The example application is selected to have a switching frequency of 250kHz.

$$R_T = \frac{2.21 \times 10^{10}}{f_{SW}} - 955 = \frac{2.21 \times 10^{10}}{250kHz} - 955 = 87.44k\Omega \quad (1)$$

A standard value of 86.6kΩ is chosen for R_T.

Note that the internal oscillator of the LM5155 can be synchronized to an external clock as described in the data sheet. The LM5155 has a maximum duty cycle limit that is frequency dependent. See the LM5155 data sheet for details on the maximum duty cycle limit.

3.2 Transformer Selection

In a flyback regulator, selecting the proper transformer for any application is a critical step. The first decision is to select the correct switching type of operation for the application, discontinuous conduction mode (DCM) or continuous conduction mode (CCM). CCM is selected for this design to minimize the primary side RMS currents, maximize full load efficiency while minimizing load voltage ripple.

3.2.1 Maximum Duty Cycle and Turns Ratio Selection

In CCM operation the duty cycle of the low side switch is calculated using Equation 2.

$$D = \frac{\frac{N_P}{N_S} \cdot |V_{LOAD}|}{V_{SUPPLY} + \frac{N_P}{N_S} \cdot |V_{LOAD}|} \quad (2)$$

where

- N_P is the number of turns on the primary side winding and assumed to be 1
- N_S is the number of turns on the secondary side winding.

The maximum duty cycle occurs when the supply voltage is at the minimum value. By selecting the maximum duty cycle, the number of turns on the secondary winding is calculated. Selecting the duty cycle to be less than 50% brings two main benefits. First, it reduces the need for slope compensation which is required for stable operation when the duty cycle is greater than 50% in CCM operation. For some wide input voltage designs limiting the duty cycle below 50% might not be possible. The LM5155 provides programmable slope compensation for such designs. Second, the right-half plane zero of the modulator is pushed to high frequencies, helping to improve the load transient response and simplifying the control loop compensation calculations. For this design the maximum duty cycle (D_{MAX}) is selected to be 40%. The number of turns on the secondary winding is calculated using Equation 3

$$N_{S\_calc} = \frac{(|V_{LOAD}|) \cdot (1 - D_{MAX}) \cdot N_P}{V_{SUPPLY\_min} \cdot D_{MAX}} = \frac{(|5V|) \cdot (1 - 0.4) \cdot 1}{18V \cdot 0.4} = 0.417 \quad (3)$$

N_S is selected to be 0.5 turns. Selecting N_S to be 0.5 turns the turns ratio to achieved in the fewest number of full turns. In this example the minimum number of turns is 2 on the primary winding and 1 turn on the secondary winding. With N_S selected, Equation 4 is used to calculate the maximum duty cycle.

$$D_{MAX} = \frac{\frac{N_P}{N_S} \cdot |V_{LOAD}|}{V_{SUPPLY\_min} + \frac{N_P}{N_S} \cdot |V_{LOAD}|} = \frac{\frac{1}{0.5} \cdot |5V|}{18V + \frac{1}{0.5} \cdot |5V|} = 0.357 \quad (4)$$

D_{MAX} is calculated to be approximately 35.7%, below the target maximum duty cycle of 40%. The number of turns on the auxiliary winding is calculated using Equation 5

$$N_{AUX\_calc} = N_S \cdot \frac{|V_{AUX}|}{|V_{LOAD}|} = 0.5 \cdot \frac{|10V|}{|5V|} = 1 \quad (5)$$

where

- V_{AUX} is the auxiliary winding voltage

3.2.2 Primary Winding Inductance Selection

Three main parameters are considered when selecting the inductance value of primary winding: primary winding current ripple ratio (IL_{RR}), falling slope of the transformer current and the right half plane zero frequency (ω_{Z_RHP}) of the control loop. Finding a balance between these three parameters helps to simplify the rest of the design process.

- The primary winding ripple current ripple ratio is selected to balance the copper loss and core loss of the transformer. As the relative ripple current increases; the core losses increase and the copper losses decrease.
- The falling slope of the transformer current should be small enough to prevent sub-harmonic oscillation in applications with a duty cycle greater than 50%. A relatively larger inductance value of the primary winding results in a smaller falling slope. The LM5155 provides fixed internal slope compensation as well as programmable slope compensation for these applications.

- The right half plane zero should be placed at high frequency, allowing for a higher crossover frequency of the control loop. As the relative inductance value of the primary winding decreases the right half plane zero frequency increases.

A maximum ripple ratio between 30% and 70% results in a good balance of the total power loss of the transformer, matching the down slope of the transformer current to the internal slope compensation and the increasing the right half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In CCM operation, the maximum primary winding ripple current occurs when the supply voltage is at the maximum value. The primary winding inductance value for CCM operation is calculated using Equation 6.

$$L_{M\_calc} = \frac{N_P^2 \cdot V_{SUPPLY\_max}^2 \cdot V_{LOAD}^2}{IL_{RR} \cdot f_{SW} \cdot P_{OUT\_total} \cdot \left(N_S \cdot V_{SUPPLY\_max} + N_P \cdot |V_{LOAD}|\right)^2}$$
$$L_{M\_calc} = \frac{1^2 \cdot 36V^2 \cdot 5V^2}{0.6 \cdot 250kHz \cdot 20.2W \cdot \left(0.5 \cdot 36V + 1 \cdot |5V|\right)^2} = 20.6\mu H \quad (6)$$

where

- IL_{RR} is the ripple ratio
- V_{SUPPLY_max} is the maximum supply current
- P_{OUT_total} is the maximum power delivered by the flyback regulator

The primary winding inductance is selected to be 21µH. The primary winding ripple current and primary winding peak current are calculated using Equation 7 and Equation 8, respectively. The peak primary winding current occurs at the minimum supply voltage.

$$\Delta IL_M = \frac{V_{SUPPLY} \cdot D}{L_M \cdot f_{SW}} = \frac{18V \cdot 0.357}{21\mu H \cdot 250kHz} = 1.224A \quad (7)$$

$$IL_{PEAK} = \frac{P_{OUT\_total}}{V_{SUPPLY\_min} \cdot D} + \frac{\Delta IL_M}{2} = \frac{20.2W}{18V \cdot 0.357} + \frac{1.224A}{2} = 3.75A \quad (8)$$

IL_{PEAK} is used to properly size the current sense resistor. Table 3-1 summarizes the key parameters of selected transformer.

Table 3-1. Selected Transformer Parameters

Parameter	Value
Turns Ratio (N_P:N_S:N_{AUX})	1:0.5:1 (2:1:2)
Primary winding inductance (L_M)	21 µH
Primary winding saturation current (I_{SAT})	6 A

3.3 Current Sense Resistor Calculations

Selection of the current sense network components is described in this section. Figure 3-1 shows the four components that make up the current sense network of the LM5155. R_S is the current sense resistor. This resistor senses the switch current for the control loop, and sets the peak current limit value. R_F and C_F form a low pass filter. This filter helps reduce the impact of any high frequency noise on the current sense signal. R_{SL} sets the external slope compensation and is optional. In some applications the internal slope compensation of the LM5155 will not be sufficient and R_{SL} will be required.

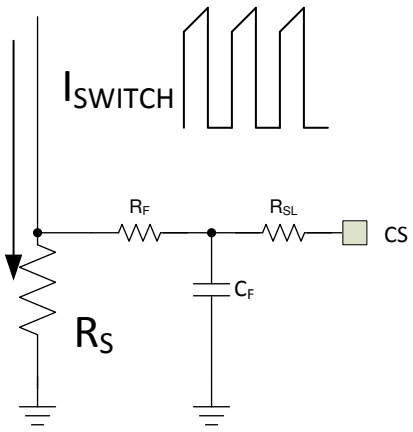

Figure 3-1. LM5155 Current Sense Network

3.3.1 Current Sense Resistor and Slope Compensation Resistor Selection

The current sense resistor is selected to avoid triggering peak current limit protection when the minimum supply voltage is present, V_{SUPPLY_min}, and supplying the maximum output power, P_{OUT_total}. Due to component tolerances and inefficiencies of the regulator, the peak current limit is set some margin above the calculated peak current of the transformer primary winding. A margin of 20% to 30% (M_{I_LIMIT}=0.2-0.3) is a good starting point. Equation 9 is used to calculate the desired peak switch current limit value. In this design example, M_{I_LIMIT} is selected to be 30%.

$$IL_{PEAK\_LIMIT\_SET} = \left(1 + M_{I\_LIMIT}\right) \cdot IL_{PEAK\_MAX} = \left(1 + 0.3\right) \cdot 3.75A = 4.88A \tag{9}$$

Selecting the correct current sense resistor is an iterative process. The first step is calculating the maximum current sense resistor value, assuming that no external slope compensation is required (R_{SL} = 0Ω). The maximum current sense resistor value is selected using Equation 10.

$$R_{S\_MAX} = 1.66 \frac{V_{SL} \cdot L_M \cdot f_{SW}}{\frac{N_P}{N_S} \cdot \left|V_{LOAD}\right|} = 1.66 \frac{40mV \cdot 21\mu H \cdot 250kHz}{\frac{1}{0.5} \cdot \left|5V\right|} = 34.9m\Omega \tag{10}$$

where

- V_{SL} is the internal fixed internal slope compensation of the LM5155

Assuming that no external slope compensation is required, the current sense resistor value is calculated using Equation 11.

$$R_{S\_wo\_sl} = \frac{V_{CLTH}}{IL_{PEAK\_LIMIT\_SET}} = \frac{100mV}{4.88A} = 20.48m\Omega \tag{11}$$

where

- V_{CLTH} is the current limit threshold of the LM5155

If the calculated $R_{S\_wo\_sl}$ resistance value is less than the R_{S_MAX} resistance value, then $R_{S\_wo\_sl}$ is selected for the current sense resistor value (R_S). If the calculated $R_{S\_wo\_sl}$ resistance value is greater than the calculated R_{S_MAX} resistance value, there are two approaches to take; decrease the current sense resistor value or add external slope compensation.

- Decreasing the current sense resistor value increases the effectiveness of the internal slope compensation. With no external slope compensation the peak inductor current limit will be constant regardless of the duty cycle when using the LM5155. A lower current sense resistor value results in a larger switch peak current limit value, which increases the required saturation current rating of the primary winding.
- Adding external slope compensation. The peak inductor current limit varies with supply voltage when external slope compensation is added to the current sense network.

External slope compensation is added by setting R_{SL} to a non-zero value, but less than 1kΩ. In applications where external slope compensation is required, R_S is calculated using Equation 12.

$$R_{S\_w\_sl} = \frac{L_M \cdot N_S \cdot f_{sw} \cdot \left(V_{CLTH} + D \cdot V_{SLOPE}\right)}{D \cdot 0.833 \cdot N_P \cdot \left|V_{LOAD}\right| + IL_{PEAK\_LIMIT\_SET} \cdot L_M \cdot N_S \cdot f_{SW}}$$
$$R_{S\_w\_sl} = \frac{21\mu H \cdot 0.5 \cdot 250kHz \cdot \left(100mV + 0.357 \cdot 40mV\right)}{0.357 \cdot 0.833 \cdot 1 \cdot \left|5V\right| + 4.88A \cdot 21\mu H \cdot 0.5 \cdot 250kHz} = 20.97m\Omega \quad (12)$$

R_{SL} is calculated using Equation 13.

$$R_{SL} = \frac{V_{CLTH} - IL_{PEAK\_LIMIT\_SET} \cdot R_{S\_w\_sl}}{I_{SLOPE} \cdot D} = \frac{100mV - 4.88A \cdot 20.06m\Omega}{30\mu A \cdot 0.357} = -223.4\Omega \quad (13)$$

where

- I_{SLOPE} is the slope compensation current source of the LM5155
- D is the duty cycle at the minimum supply voltage

If the calculated R_{SL} value is negative, the internal slope compensation is adequate and the additional slope compensation is not required. If the calculated R_{SL} value exceeds the maximum value of the 1kΩ, the down slope of the sensed current needs to be reduce. To reduce the down slope of the primary winding current, the primary winding inductance value of L_M must be increased. If the primary winding inductance value is changed the current sense resistor calculations must be redone.

Following the design procedure, a current sense resistor value is selected to be 20mΩ (R_S), which is the nearest standard resistor value to the calculated value in Equation 14. No external slope compensation is required and R_{SL} is selected to be 0Ω. The peak current limit of the transformer primary winding is calculated using Equation 14.

$$IL_{PEAK\_LIMIT} = \frac{V_{CLTH} - I_{SLOPE} \cdot R_{SL} \cdot D}{R_S} = IL_{PEAK\_LIMIT} = \frac{100mV - 30\mu A \cdot 0\Omega \cdot 0.375}{20m\Omega} = 5A \quad (14)$$

where

- D is they duty cycle at the minimum supply voltage

The peak current limit of the transformer primary winding is constant, regardless of the supply voltage, because there is no added external slope compensation. The saturation current rating of the transformer primary winding is 6A, and is adequate for the selected R_S value of 20mΩ.

3.3.2 Current Sense Resistor Filter Selection

For all designs is it recommended to add a low pass filter to the current sense signal. R_F and C_F implement this low pass filter as shown in Figure 3-1. The filter is added to help mitigate the impact of the leading edge spike on the current sense signal. R_F is selected to be between 10Ω and 200Ω. For this design R_F is selected to be 100Ω. C_F must be less than the value specified in Equation 15 to ensure proper operation.

$$C_F < \frac{1 - D}{3 \cdot R_F \cdot f_{SW}} = \frac{1 - 0.357}{3 \cdot 100\Omega \cdot 250kHz} = 1.89nF \quad (15)$$

C_F is selected to be 470pF.

3.4 MOSFET Selection

MOSFET selection for a flyback controller focuses on power dissipation and voltage rating. Power dissipation of MOSFET is composed of two different parts, conduction losses and switching losses. Conduction losses are dominated by the $R_{DS(ON)}$ resistance of the MOSFET. Switching losses occur during the rise time and fall time of the switch node, when the N-channel MOSFET is turning on and turning off. During the rise time and fall time, current through the MOSFET channel and a large voltage drop across the drain to source are present,

resulting in power dissipation. The longer the rise and fall time of the switch node the higher the switching losses. Selecting a MOSFET with minimal parasitic capacitances decreases the switching losses.

The total gate charge (Q_{G_total}) must be small enough to keep the internal VCC regulator from entering current limit. The Q_{G_total} for a given MOSFET can be found in the component data sheet. Equation 16 provides the maximum total gate charge of the MOSFET for the selected switching frequency. The Q_{G_total} of the selected MOSFET is 35nC.

$$Q_{G\_total} < \frac{35mA}{f_{SW}} \tag{16}$$

The RMS current of the MOSFET is estimated using Equation 17. By estimating the switch RMS current, a MOSFET with an adequately small $R_{DS(ON)}$ value is selected.

$$I_{MOS\_RMS} = \sqrt{D \cdot \left(\left(\frac{P_{OUT\_total}}{V_{SUPPLY\_min} \cdot D} \right)^2 + \frac{\Delta IL_M^2}{12} \right)} = \sqrt{0.357 \cdot \left(\left(\frac{20.2W}{18V \cdot 0.357} \right)^2 + \frac{1.224^2}{12} \right)} = 1.89A \tag{17}$$

The $R_{DS(ON)}$ of the selected MOSFET is 8.7mΩ.

The drain to source break down voltage rating on the MOSFET needs to be higher than the reflected secondary side voltage plus the maximum input voltage as calculated in Equation 18.

$$V_{DS} > \left(\frac{N_P}{N_S} V_{LOAD} \right) + V_{SUPPLY\_max} = \left(\frac{1}{0.5} \cdot 5V \right) + 36V = 46V \tag{18}$$

Due to the parasitic leakage inductance of the primary winding, the switch node voltage rings well above the value calculated in Equation 18. To overcome the ringing on the switch node a voltage clamp can be added. Designing this clamp is not described in this application report. For this design a MOSFET with a voltage rating of 100 V is selected.

3.5 Diode Selection

The diode on the secondary side must have a reverse voltage rating greater than the reflected voltage for the primary transformer winding to the secondary winding plus the secondary load voltage. The reverse voltage of the secondary diode is calculated in Equation 19.

$$V_{D\_reverse} = \left(\frac{N_S}{N_P} \cdot V_{SUPPLY\_max} \right) + V_{LOAD} = \left(\frac{0.5}{1} \cdot 36V \right) + 5V = 23V \tag{19}$$

Due to leakage inductance, there is a negative spike when the primary side switch is being turned off. A snubber needs to be added across the diode to help minimize this voltage spike. Even if a snubber is added, some voltage margin must be added to the value calculated in Equation 20. For this application, a diode with a reverse voltage rating of 40 V is selected.

The average current of the secondary side diode is estimated using Equation 20.

$$I_{D\_AVG} = I_{LOAD} = 5A \tag{20}$$

The diode must be able to conduct the value calculated in Equation 20 with some margin. For the design, the selected diode is capable of conducting 10 A of average forward current.

3.6 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. A practical way to size the output capacitor is based on the required load transient specification. The load transient specification is related to the control loop crossover frequency. For this estimate it is expected that the control loop cross over frequency is set to 1/5th the right half plane zero frequency. This right half plane zero frequency is calculated using Equation 21.

$$f_{CROSS} = \frac{f_{Z\_RHP}}{5} = \frac{N_P^{\ 2}}{N_S^{\ 2}} \cdot \frac{\frac{V_{LOAD}^{\ 2}}{P_{OUT\_total}} \cdot \left(D'\right)^2}{5 \cdot 2 \cdot \pi \cdot L_M} = \frac{1^2}{0.5^2} \cdot \frac{\frac{5^2}{20.2W} \cdot (1-0.357)^2}{5 \cdot 2 \cdot \pi \cdot 21\mu H} = 8.68kHz \quad (21)$$

For this design example, the load transient specification indicates that the load voltage should not overshoot or undershoot more than 100mV during a load transient from 50% load current (2 A) to 100% load current (4 A) occurs. Equation 22 is used to calculate the estimated load capacitance to achieve the specified load transient load voltage ripple requirements.

$$C_{LOAD\_min} = \frac{\Delta I_{LOAD}}{2\pi \cdot f_{CROSS} \cdot \Delta V_{LOAD}} = \frac{2A}{2\pi \cdot 8.6kHz \cdot 100mV} = 366\mu F \quad (22)$$

where

- ΔI_{LOAD} is the difference in the load current conditions (4 A - 2 A)
- ΔV_{LOAD} is the specified overshoot voltage specification and undershoot voltage specification

In this design C_{LOAD} is selected to be 540µF.

3.7 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. For this design, the input voltage ripple is designed to be less than 50mV when the supply voltage is at the minimum value. Equation 23 is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN\_min} = \frac{\frac{P_{OUT\_total}}{V_{SUPPLY\_min}} \cdot (1-D)}{\Delta V_{SUPPLY} \cdot f_{SW}} = \frac{\frac{20.2W}{18V} \cdot (1-0.357)}{50mV \cdot 250kHz} = 57.7\mu F \quad (23)$$

The input capacitor is selected to be 100µF. Ceramic capacitors are added to help lower the ESR of the input capacitor bank.

3.8 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating supply voltage of the regulator. Two levels must be specified; the voltage the LM5155 starts operation ($V_{SUPPLY(ON)}$) and the voltage the LM5155 enters stand-by mode ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 17 V and the $V_{SUPPLY(OFF)}$ is 16 V. Using Equation 24, the top UVLO resistor (R_{UVLOT}) is calculated.

$$R_{UVLOT} = \frac{0.967 \cdot V_{SUPPLY(ON)} - V_{SUPPLY(OFF)}}{5\mu A} = \frac{0.967 \cdot 17V - 16V}{5\mu A} = 86.66k\Omega \quad (24)$$

R_{UVLOT} is selected to be 100kΩ. R_{UVLOB} is calculated using Equation 25.

$$R_{UVLOT} = \frac{1.5V \cdot R_{UVLOT}}{V_{SUPPLY(ON)} - 1.5V} = \frac{1.5V \cdot 100k\Omega}{17V - 1.5V} = 9.67k\Omega \quad (25)$$

R_{UVLOB} is selected to be 9.67kΩ.

3.9 Control Loop Compensation

In this section, a general technique is described to stabilize the control loop for a peak current mode controlled flyback regulator in continuous conduction mode operation. Figure 3-2 shows circuit that implements the isolated feedback path. To maintain the voltage isolation between the primary side and secondary side an optocoupler is used. In Figure 3-2 the FB pin of the LM5155 is tied to ground. C_{OPTO} is the parasitic capacitance of the optocoupler. This value is dependent upon the selected R_{PULLUP} value and can be estimated using the optocoupler data sheet. Assuming the C_{COMP} is much larger than C_{OPTO}, helps to simplify the loop calculations. However, a pole is formed by R_{PULLUP} and C_{OPTO} which is considered for accurate loop modeling. For a detailed model of the isolated feedback transfer function see Table 5-2.

There are many different strategies to set the crossover frequency of the control loop, and correctly place the poles and zeros of the feedback path to achieve stable operation. The loop compensation selection process is broken down into a number of simplified steps described in the following sections.

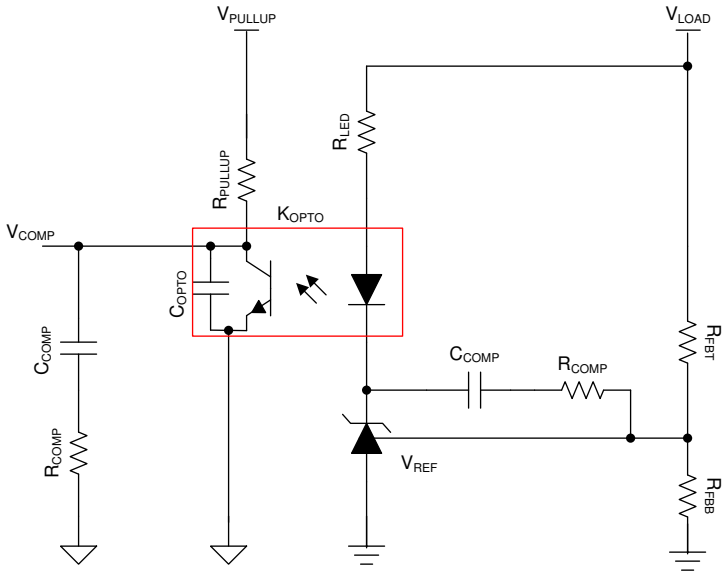

Figure 3-2. Isolated Feedback

3.9.1 Feedback Resistor Selection

To implement the circuit shown in Figure 3-2, a voltage reference must first be selected. The TLV431 is selected due to the low reference voltage of 1.24 V. For higher load voltage designs is it acceptable to use the TL431, with a reference voltage of 2.5 V. The load voltage of this designs is 5 V, selecting a reference voltage of 1.24 V allows for more headroom to ensure the voltage reference is properly biased. The top feedback resistor, R_{FBT}, is selected to be 30 kΩ in this design. Equation 26 is used to calculate the lower feedback resistor, R_{FBB}.

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{LOAD}}{V_{REF}} - 1} = \frac{30k\Omega}{\frac{5V}{1.24V} - 1} = 9.89k\Omega \tag{26}$$

R_{FBB} is selected to be the standard value of 9.78kΩ.

3.9.2 R_{PULLUP} Selection

A resistor between V_{PULLUP} and V_{COMP} is suggested to implement the feedback circuit. This pull-up voltage can vary depending on the auxiliary winding voltage or can be the VCC voltage of the LM5155. For this design the V_{PULLUP} rail is connected to the auxiliary winding of 10 V. Equation 27 is used to calculate the minimum R_{PULLUP} value.

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP\_max}}{I_{COMP\_clamp}} = \frac{10V - 2.5V}{1.6mA} = 4.66k\Omega \tag{27}$$

R_{PULLUP} is selected to be 4.99 kΩ.

3.9.3 Optocoupler Selection

When selecting a optocoupler a few major parameters need to be considered: current transfer ratio (CTR), diode voltage drop on the secondary side, and the capacitance of the BJT on the primary side. In the following equations CTR is synonymous with k_{OPTO}, the diode drop with V_D and the BJT capacitance with C_{OPTO} in Figure 3-2.

- The CTR varies drastically based on the selected component. There can be as large as 600% variance in the CTR value over operating conditions. Due to this large tolerance in CTR, the loop compensation component

selection needs to account for the minimum CTR value and maximum CTR value. In this design the CTR of the selected optocoupler is 100% to 200%.

- The diode voltage drop impacts the selection of the R_{LED} value. The diode drop need to be small enough to allow the voltage reference to be supplied with adequate voltage to ensure operation. The diode drop of the selected optocoupler is 1.4V.
- The pull-up resistor (R_{PULLUP}) and the parasitic capacitance (C_{OPTO}) form a pole, limiting the maximum crossover frequency of the control loop. Once the pull-up resistor is selected the capacitance of the optocoupler is calculated from the optocoupler data sheet. The selected optocoupler the capacitance is calculated to be approximately 3.3nF. The cross over frequency should be less than the pole, which is roughly 9.66kHz for this design.

Table 3-2 summarizes the key parameters of the selected optocoupler.

Table 3-2. Selected Optocoupler parameters

Parameter	Value
k_{OPTO_min}	100%
k_{OPTO_max}	200%
V_D	1.4V
C_{OPTO}	3.3nF
$V_{CE(sat)}$	200mV

3.9.4 R_{LED} Selection

The resistor in series with the optocoupler diode, R_{LED}, directly affects the mid-band gain of control loop. Equation 28 is used to calculated the maximum value of R_{LED} ensuring that V_{COMP} voltage on the primary side can be pulled to the saturation voltage of the optocoupler BJT, $V_{CE(sat)}$.

$$R_{LED} < \frac{(V_{LOAD} - V_{REF} - V_D) \cdot R_{PULLUP} \cdot K_{OPTO\_min}}{V_{PULLUP} - V_{CEsat}} = \frac{(5V - 1.24V - 1.4V) \cdot 4.99k\Omega \cdot 1}{10V - 200mV} = 1.2k\Omega \quad (28)$$

R_{LED} is selected to be 1 kΩ.

3.9.5 Crossover Frequency Selection

The crossover frequency of the loop is selected to be 1/5th the right half plane zero frequency, and less than the pole set by the BJT capacitance and the pull-up resistor. Equation 29 details how to calculate the 1/5th the right half plane zero frequency.

$$f_{CROSS} = \frac{f_{Z\_RHP}}{5} = \frac{N_P^2}{N_S^2} \cdot \frac{\frac{V_{LOAD}^2}{P_{OUT\_total}} \cdot (D')^2}{5 \cdot 2 \cdot \pi \cdot L_M} = \frac{1^2}{0.5^2} \cdot \frac{\frac{5^2}{20.2W} \cdot (1 - 0.357)^2}{5 \cdot 2 \cdot \pi \cdot 21\mu H} = 8.68kHz \quad (29)$$

The crossover frequency (f_{CROSS}) is selected less than 1/5th the right half plane zero frequency. To allow for component tolerances over temperature and process, a crossover frequency of 6kHz is selected.

3.9.6 Determine Required R_{COMP}

The R_{COMP} value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Decreasing the R_{COMP} resistance value lowers the crossover frequency but helps ensure the control loop remains stable over the specified supply voltage range. Knowing the desired loop crossover frequency, 6 kHz, R_{COMP} is calculate using Equation 30.

$$R_{COMP} = \frac{N_S}{N_P} \cdot \frac{2 \cdot \pi \cdot C_{LOAD} \cdot R_S \cdot f_{CROSS} \cdot R_{LED}}{G_{COMP} \cdot K_{OPTO\_max} \cdot (1 - D)} = \frac{0.5}{1} \cdot \frac{2 \cdot \pi \cdot 540\mu F \cdot 20m\Omega \cdot 6kHz \cdot 1k\Omega}{0.142 \cdot 2 \cdot (1 - 0.357)} = 1.15k\Omega \quad (30)$$

R_{COMP} is selected to be 1 kΩ.

3.9.7 Determine Required C_{COMP}

The R_{COMP} resistor and C_{COMP} capacitor set a low frequency zero of the compensation network, providing a phase boost. Placement of this zero frequency largely impacts the transient response of the control loop. A good strategy to help ensure adequate phase margin is to place the zero at geometric mean of the crossover frequency (f_{CROSS}) and the low frequency pole of the modulator. Equation 31 places the low frequency zero of error amplifier a the geometric mean of f_{CROSS} and low frequency pole of the plant (ω_{P_LF}).

$$C_{COMP} = \sqrt{\frac{C_{LOAD} \cdot V_{LOAD}^{2}}{2 \cdot \pi \cdot R_{COMP}^{2} \cdot f_{CROSS} \cdot (1 + D)}} = \sqrt{\frac{540\mu F \cdot 5V^{2}}{2 \cdot \pi \cdot 1k\Omega^{2} \cdot 6kHz \cdot (1 + 0.217)}} = 120nF \quad (31)$$

where

- D is the duty cycle at the maximum supply voltage (0.217)

For this design C_{COMP} is selected to be 220 nF to help ensure extra phase margin.

4 Component Selection Summary

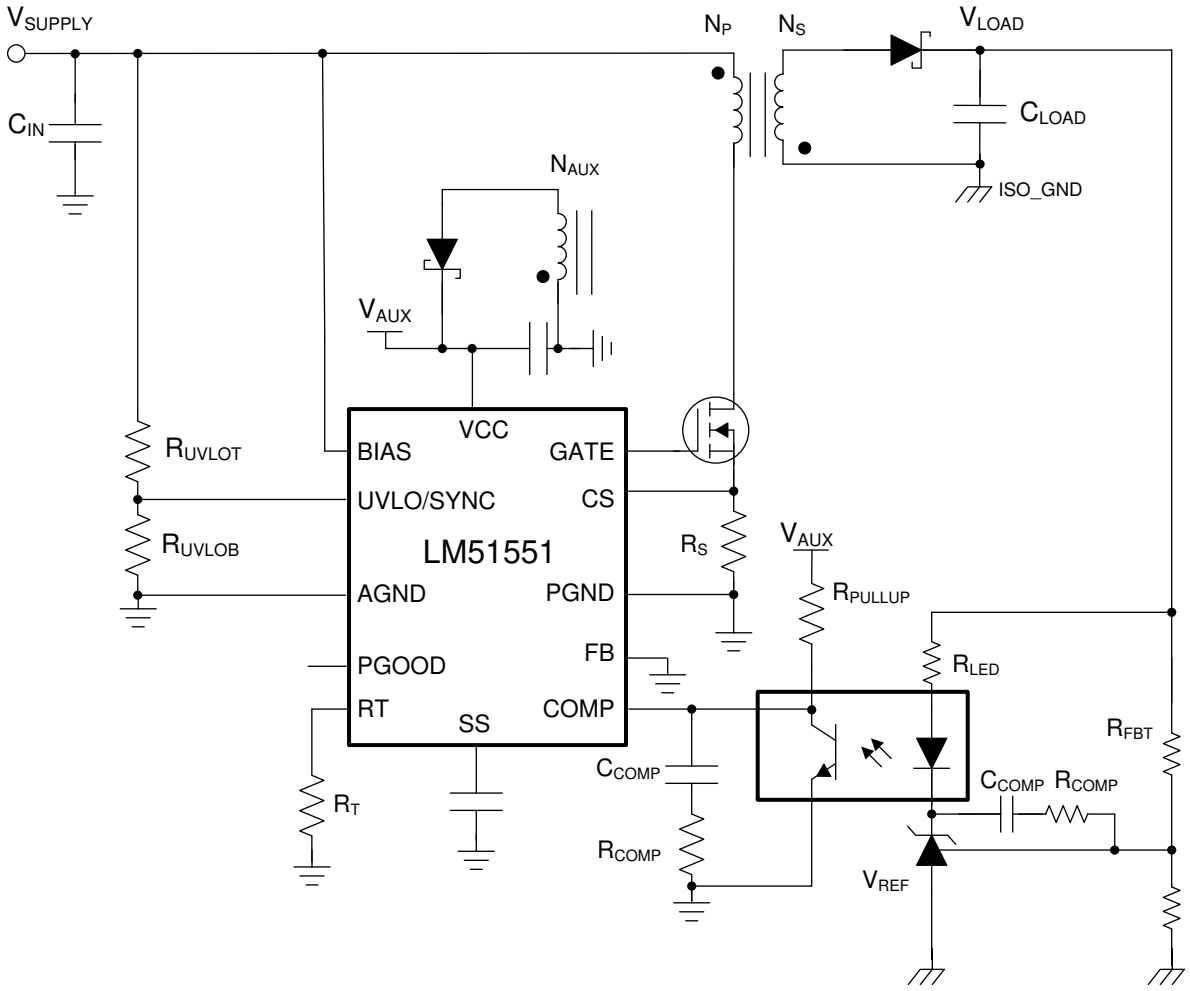

Figure 4-1. Application Circuit

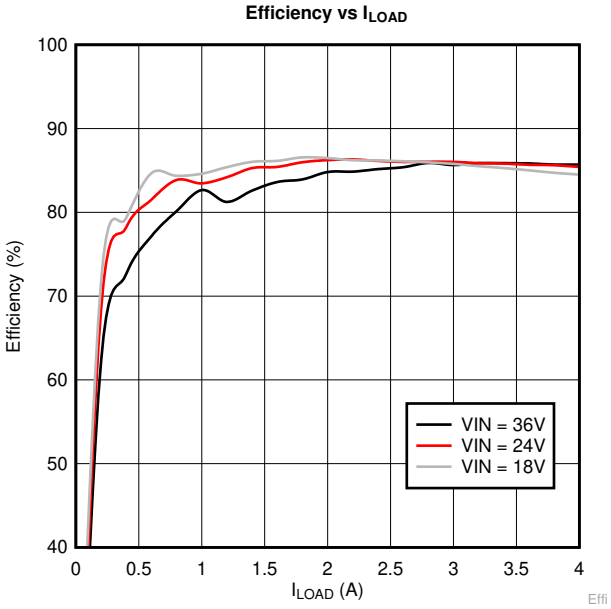

Figure 4-2. Efficiency vs. I_{LOAD}

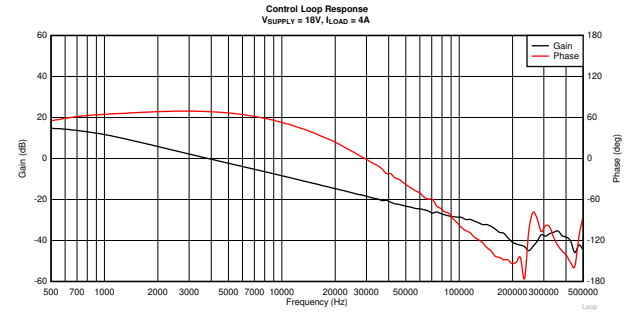

Figure 4-3. Control Loop Response V_{SUPPLY} = 18 V, I_{LOAD} = 4 A

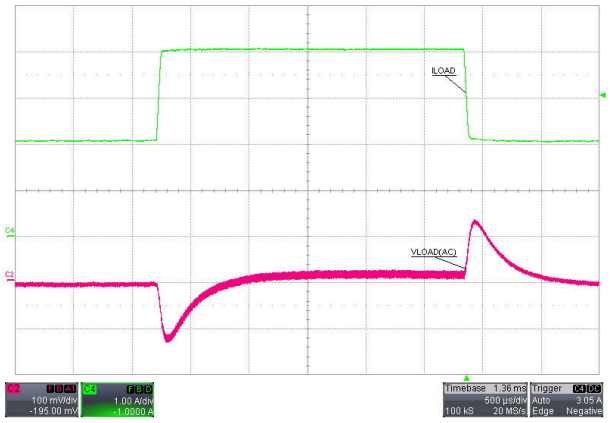

Figure 4-4. Load Step: I_{LOAD} 2 A to 4 A, V_{SUPPLY} = 18 V

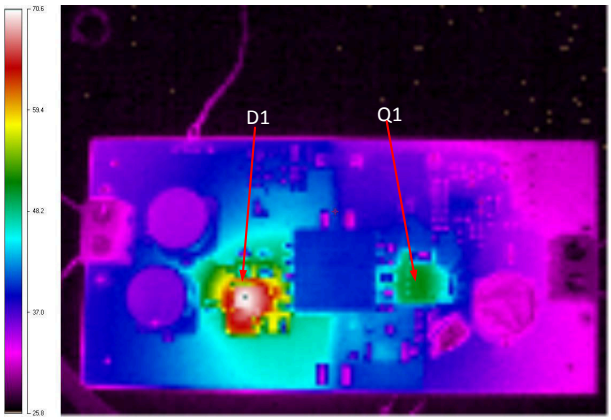

Figure 4-5. Thermal Image: V_{SUPPLY} = 18 V, I_{LOAD} = 4 A

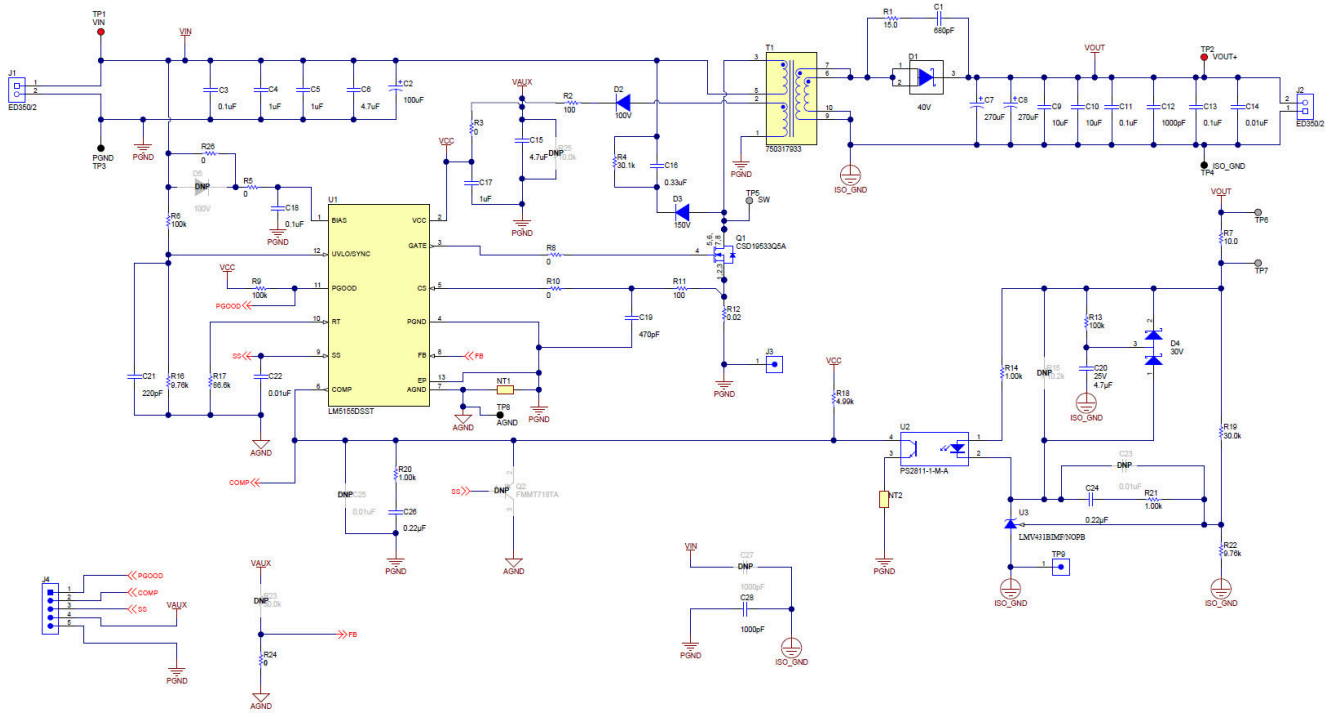

Figure 4-6. LM5155EVM-FLY Schematic

Table 4-1. List of Components

Item	Qty	Value	Description	Package Ref	Part Number	Mfr
C1	1	680pF	CAP, CERM, 680 pF, 100 V, +/- 10%, X7R, 0603	0603	GRM188R72A681KA01D	MuRata
C2	1	100uF	CAP, Polymer Hybrid, 100 uF, 50 V, +/- 20%, 28 ohm, 10x10 SMD	10x10	EEHZC1H101P	Panasonic
C3	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 20%, X7R, 0805	0805	08055C104MAT2A	AVX
C4, C5	2	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	08055C105KAT2A	AVX
C6	1	4.7uF	CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, 1206	1206	C3216X7R1H475K160AC	TDK
C7, C8	2	270uF	CAP, Aluminum Polymer, 270 uF, 25 V, +/- 20%, 0.027 ohm, D10xL12.7mm SMD	D10xL12.7mm	PCV1E271MCL1GS	Nichicon
C9, C10	2	10uF	CAP, CERM, 10 uF, 25 V,+/- 10%, X7R, 1210	1210	885012209028	Wurth Elektronik
C11, C13	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	0603	C1608X7R1E104K080AA	TDK
C12	1	1000pF	CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E102KA01D	MuRata
C14	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71H103KA37D	MuRata
C15	1	4.7uF	CAP, CERM, 4.7 uF, 35 V, +/- 10%, X5R, 0603	0603	GRM188R6YA475KE15D	MuRata
C16	1	0.33uF	CAP, CERM, 0.33 uF, 100 V, +/- 10%, X7R,		C3216X7R2A334K130AA	TDK
C17	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71C105MA64D	MuRata
C18	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H104K080AA	TDK
C19	1	470pF	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H471KA01D	MuRata
C20	1	4.7uF	CAP, CERM, 4.7 µF, 25 V,+/- 10%, X6S, AEC-Q200 Grade 2, 0603	0603	GRT188C81E475KE13D	MuRata
C21	1	220pF	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C221J5GACTU	Kemet
C22	1	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	0603	GRM188R71C103KA01D	MuRata
C24, C26	2	0.22uF	CAP, CERM, 0.22 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CL10B224KO8VPNC	Samsung
C28	1	1000pF	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1812	1812	1812GC102K1A	AVX
D1	1	40V	Diode, Schottky, 40 V, 10 A, AEC-Q101, TO-277A	TO-277A	SS10P4-M3/87A	Vishay-Semiconductor
D2	1	100V	Diode, Switching, 100 V, 0.2 A, SOD-323	SOD-323	MMDL914-TP	Micro Commercial Components
D3	1	150V	Diode, Superfast Rectifier, 150 V, 1 A, SMA	SMA	ES1C-13-F	Diodes Inc.
D4	1	30V	Diode, Schottky, 30 V, 0.2 A, SOT-323	SOT-323	BAT54SWT1G	Fairchild Semiconductor
H1, H2, H3, H4	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1, J2	2		Terminal Block, 5mm, 2-pole, TH	TH, 2-Leads, Body 10x9mm, Pin Spacing 5mm	ED350/2	On-Shore Technology

Table 4-1. List of Components (continued)

Item	Qty	Value	Description	Package Ref	Part Number	Mfr
J3, TP9	2		TEST POINT SLOTTED .118", TH	Test point, TH Slot Test point	1040	Keystone
J4	1		Header, 2.54mm, 5x1, Tin, TH	Header, 2.54mm, 5x1, TH	PEC05SAAN	Sullins Connector Solutions
Q1	1	100V	MOSFET, N-CH, 100 V, 13 A, DQJ0008A (VSONP-8)	DQJ0008A	CSD19533Q5A	Texas Instruments
R1	1	15.0	RES, 15.0, 1%, 0.5 W, 1210	1210	ERJ-14NF15R0U	Panasonic
R2, R11	2	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1000V	Panasonic
R3	1	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R4	1	30.1k	RES, 30.1 k, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW251230K1FKEG	Vishay-Dale
R5, R8, R10, R24, R26	5	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R6, R9, R13	3	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R7	1	10.0	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEA	Vishay-Dale
R12	1	0.02	RES, 0.02, 1%, 1 W, 0612	0612	PRL1632-R020-F-T1	Susumu Co Ltd
R14	1	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1001V	Panasonic
R16, R22	2	9.76k	RES, 9.76 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06039K76FKEA	Vishay-Dale
R17	1	86.6k	RES, 86.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060386K6FKEA	Vishay-Dale
R18	1	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K99FKEA	Vishay-Dale
R19	1	30.0k	RES, 30.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730KL	Yageo
R20, R21	2	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
T1	1	21uH	Transformer, 21 uH, SMT	13.97x18.25 mm	750317933	Wurth Elektronik
TP1, TP2	2		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP3, TP4, TP8	3		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP5	1		PC Test Point, SMT	PC Test Point, SMT	5017	Keystone
U1	1		2.2-MHz Wide Input Nonsynchronous Boost, Sepic, Flyback Controller, DSS0012B (WSON-12)	DSS0012B	LM5155DSST	Texas Instruments
U2	1		Optocoupler, 2.5 kV, 100-200% CTR, SMT	PS2811-1	PS2811-1-M-A	California Eastern Laboratories
U3	1		Low-Voltage (1.24V) Adjustable Precision Shunt Regulators, 3-pin SOT-23, Pb-Free	DBZ0003A	LMV431BIMF/NOPB	Texas Instruments

5 Small Signal Frequency Analysis

This section provides detailed equations used to model the control loop when the LM5155 is configured as an isolated flyback regulator. These equations are only valid when the regulator is operating in continuous conduction mode. The simplified formulas allow for quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

5.1 Flyback Regulator Modulator Modeling

These equations model the plant of a peak current mode flyback regulator in continuous conduction mode.

Table 5-1. Control Loop Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n^2}\right)}$
Modulator DC Gain	$A_M = G_{COMP} \cdot \frac{N_P}{N_S} \frac{V_{LOAD}^2}{P_{OUT}} \frac{(1-D)}{(1+D)A_{CS}\cdot R_S}$	
RHP Zero	$\omega_{Z\_RHP} = \frac{\frac{N_P^2}{N_S^2}\cdot\frac{V_{LOAD}^2}{P_{OUT}}(1-D)^2}{L_M \cdot D}$	
ESR Zero	$\omega_{Z\_ESR} = \frac{1}{C_{LOAD}\cdot R_{ESR}}$	
Low Frequency Pole	$\omega_{P\_LF} = \frac{1+D}{C_{LOAD}\cdot\frac{V_{LOAD}^2}{P_{OUT}}}$	
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi \cdot f_{sw}$
Quality Factor	Not Considered	$Q = \frac{1}{\pi\left[D'\cdot\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$
Slope Compensation	Not Considered	$s_e = \left(V_{SLOPE}+I_{SLOPE}\cdot R_{SL}\right)\cdot f_{sw}$
Sensed Rising Inductor Slope	Not Considered	$s_n = \frac{V_{SUPPLY}\cdot(1-D)\cdot R_S\cdot A_{CS}}{L_M}$

5.2 Compensation Modeling

These equation model the isolate compensation network shown in Figure 3-2.

Table 5-2. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\hat{v}_{COMP}(s)}{\hat{v}_{LOAD}(s)} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Z1\_EA}}\right)\left(1+\frac{s}{\omega_{Z2\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$	$\frac{\hat{v}_{COMP}(s)}{\hat{v}_{LOAD}(s)} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Z1\_EA}}\right)\left(1+\frac{s}{\omega_{Z2\_EA}}\right)}{s\cdot\left(k_1\cdot s^2+k_2\cdot s+1\right)}$
Feedback DC Gain	$A_{FB} = \frac{K_{OPTO}\cdot R_{PULLUP}}{R_{LED}\cdot R_{FBT}\cdot C_{COMP}}$	
First Low Frequency Zero	$\omega_{Z1\_EA} = \frac{1}{(R_{COMP}+R_{FBT})\cdot C_{COMP}}$	
Second Low Frequency Zero	$\omega_{Z2\_EA} = \frac{1}{R_{COMP}\cdot C_{COMP}}$	
Low Frequency pole	$\omega_{P\_EA} = \frac{1}{(R_{COMP}+R_{PULLUP})\cdot C_{HF}}$	N/A
K1	Not Considered	$k_1 = C_{COMP}\cdot C_{OPTO}\cdot R_{COMP}\cdot R_{PULLUP}$
K2	Not Considered	$k_2 = C_{COMP}\cdot(R_{COMP}+R_{PULLUP})+C_{OPTO}\cdot R_{PULLUP}$
Mid-band Gain	$G_{MID} = \frac{K_{OPTO}\cdot R_{COMP}}{R_{LED}}$	$G_{MID} = \frac{K_{OPTO}\cdot R_{COMP}\cdot(R_{FBT}+R_{COMP})}{R_{LED}\cdot R_{FBT}\cdot(R_{COMP}+R_{PULLUP})}$

6 Revision History

Changes from Revision * (February 2019) to Revision A (January 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated equation	10

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