Application Report
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Using the TPSM53602/3/4 for Negative Output, Inverting Buck Boost Application

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ABSTRACT

The TPSM53604 is a 5 x 5.5 mm^2, 4-A rated, synchronous step-down power module that features a wide operating input range from 3.8 V to 36 V with adjustable output voltage range from 1 V to 7 V. This application report shows how the conventional evaluation board for the TPSM53604 can be configured for an inverting buck boost (IBB) application to produce a negative output voltage. This application note also provides the typical level-shifter circuitry needed to utilize the auxiliary functions of the power module in an IBB topology. Note that the TPSM53602 and TPSM53603 are lower current rated pin-to-pin compatible devices to the TPSM53604. For more information on inverting buck boost conversion, refer to the *Working with inverting buck-boost converters* application report for more details.

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1 Inverting Buck-Boost Topology

1.1 Concept

In a standard buck configuration the positive connection (V_{OUT}) is connected to the internal inductor, and the return connection is connected to the device ground.

In the IBB configuration, SYS_GND is connected to device V_{OUT} and the device return is now the negative output voltage (-VOUT). This shift in topology allows the output voltage to be inverted with respect to the input voltage.

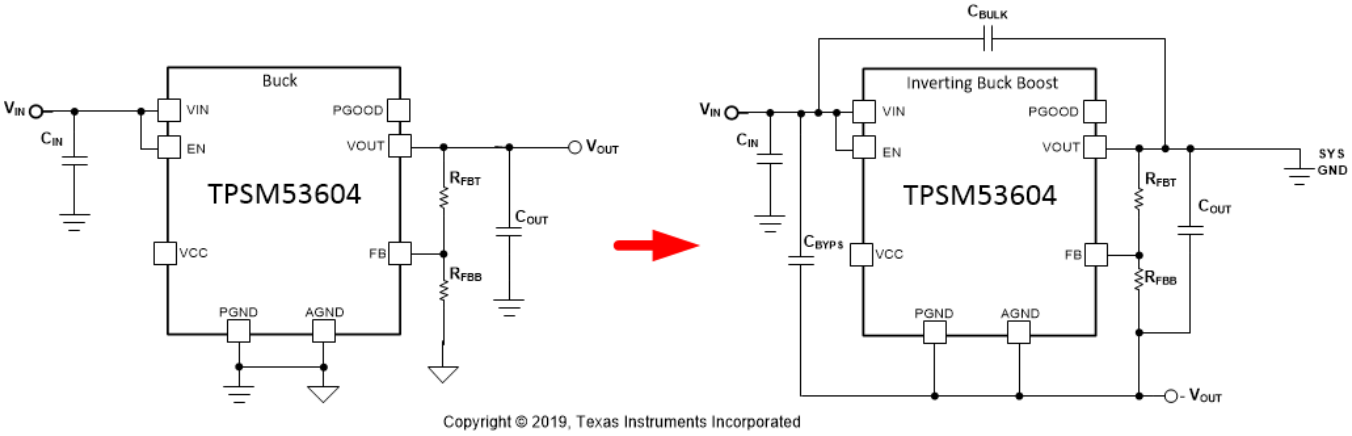

Figure 1. Converting From Buck to Inverting Buck Boost Topology

1.2 Output Current Calculations

By changing the buck configuration into an IBB configuration, the average inductor current is affected. The output current capability in the IBB topology is less than the buck configuration. The maximum achievable current is calculated by the following:

I_{OUT} (IBB) = I_{L_max} × (1 – D)

- I_{L_max} is the maximum rated inductor current
- D is the operating duty cycle

(1)

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2:

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN}) \times \eta} \quad (2)$$

NOTE: V_{OUT} in Equation 2 is represented with a negative value.

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. A conservative value efficiency of 70% is used for calculating the duty cycle. Use Equation 1 and Equation 2 to calculate the recommended maximum output current. For example a 24-V input voltage, –5-V output voltage application using the TPSM53604 power module results in a maximum output current of 3 A.

Table 1. Maximum Output Current Calculation for TPSM53604

V_{OUT} (V)	V_{IN} (V)	IL_max	D	I_{OUT} (A)
-1.2	24	4	0.068	3.7
-1.8	24	4	0.099	3.6
-2.5	24	4	0.134	3.4
-3.3	24	4	0.172	3.3
-5	24	4	0.246	3

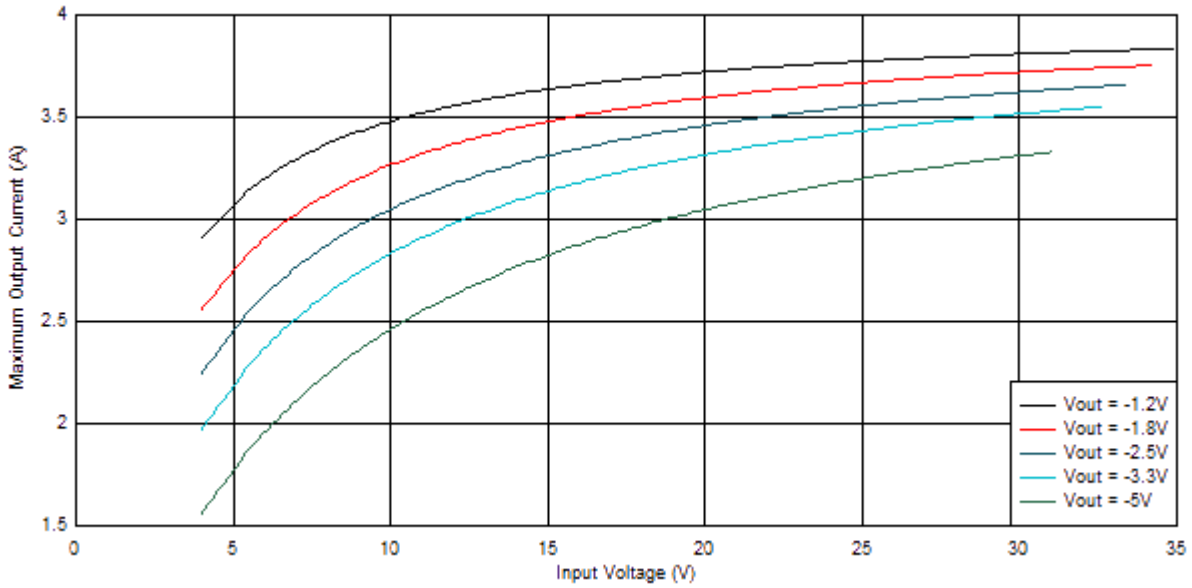

Figure 2. Recommended Maximum Output Current for TPSM53604

Table 2. Maximum Output Current Calculation for TPSM53603

V_{OUT} (V)	V_{IN} (V)	IL_max	D	I_{OUT} (A)
-1.2	24	3	0.068	2.8
-1.8	24	3	0.099	2.7
-2.5	24	3	0.134	2.6
-3.3	24	3	0.172	2.48
-5	24	3	0.246	2.26

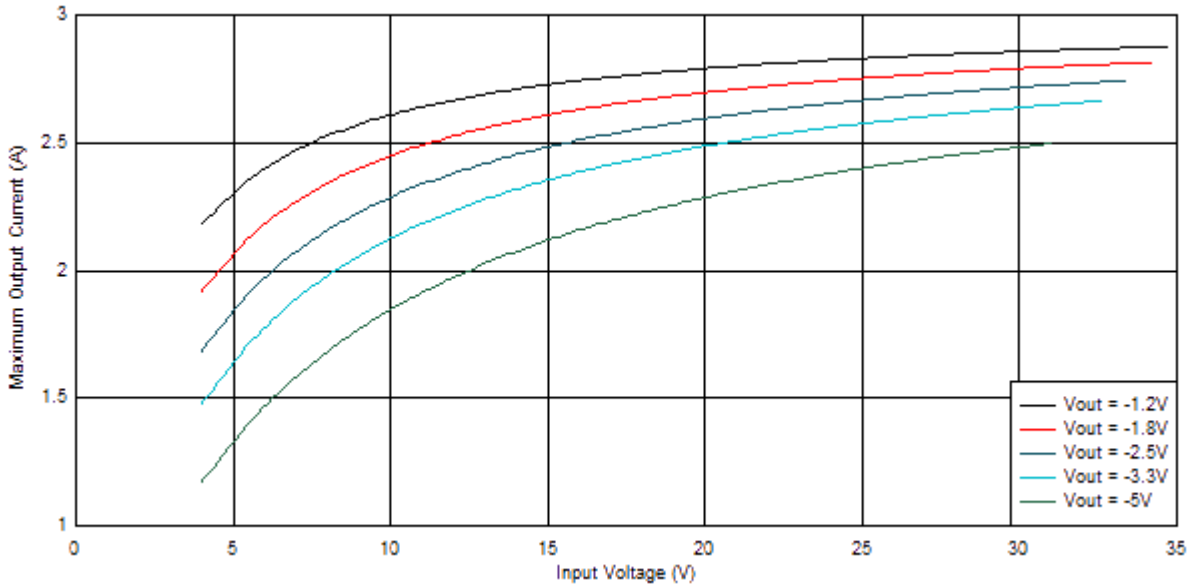

Figure 3. Recommended Maximum Output Current for TPSM53603

Table 3. Maximum Output Current Calculation for TPSM53602

V_{OUT} (V)	V_{IN} (V)	IL_max	D	I_{OUT} (A)
-1.2	24	2	0.068	1.86
-1.8	24	2	0.099	1.8
-2.5	24	2	0.134	1.73
-3.3	24	2	0.172	1.65
-5	24	2	0.246	1.5

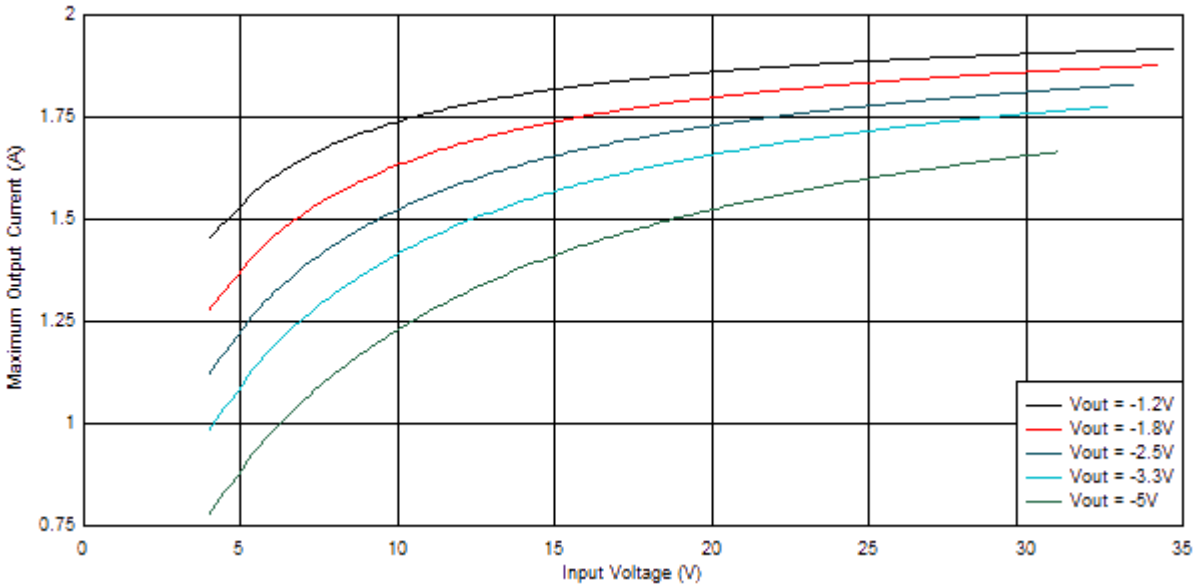

Figure 4. Recommended Maximum Output Current for TPSM53602

1.3 V_{IN} and V_{OUT} Range In Inverting Configuration

When configured in an IBB topology, the input voltage across the module is V_{IN} to V_{OUT} effectively limiting the input voltage range. The TPSM53604 has an input voltage range from 3.8 V to 36 V + V_{OUT}, where V_{OUT} is a negative value. For example, for an output voltage of –7 V the maximum input voltage is 29 V. The output voltage range in this topology is –1 V to –7 V.

2 Design Considerations

2.1 Additional Bypass Capacitor and Schottky Diode

Use a ceramic bypass capacitor, C_{BYPS}, with a minimum capacitance of 10 µF. The voltage rating must be taken into consideration because this capacitor will experience stress equal to the full voltage range between V_{IN} and V_{OUT}.

In order for the sytem to be stable, there must be an input power supply capacitor to help dampen the high-frequency noise that can couple onto the circuit. An electrolytic capacitor with moderate ESR helps dampen any input supply ringing caused by long power leads. When using the TPSM53604EVM, C_{BULK} capacitor must be added across V_{IN} and SYS_GND.

Consider that the inclusion of the C_{BYPS} capacitor introduces an AC path from V_{IN} to V_{OUT} and might worsen the transient response. When V_{IN} is applied to the circuit, this dV/dt across the bypass capacitor creates a current that must return to ground to complete the loop. This current might flow through the internal low-side body diode of the MOSFET and the inductor to return to ground. For this case, it is recommended to have a Schottky diode between $-V_{OUT}$ and SYS GND. If large line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

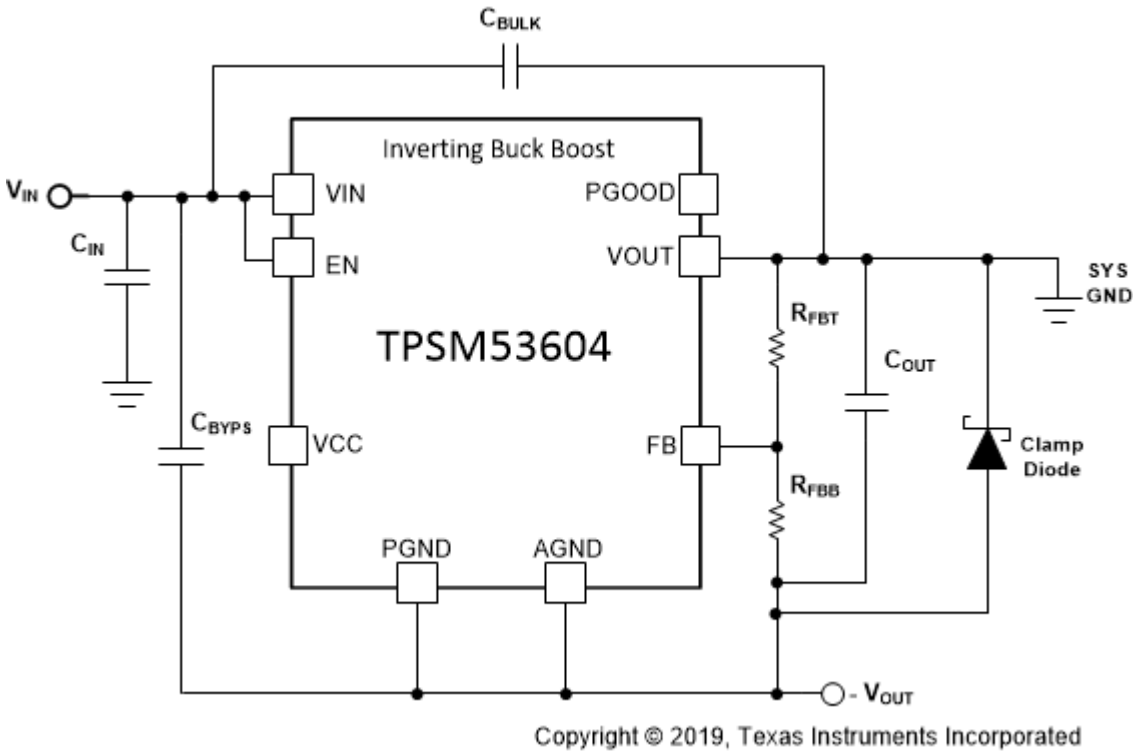

Figure 5. TPSM53604 Inverting Buck-Boost Schematic

2.2 Start-up Behavior and Switching Node Consideration

The voltage on the SW pin switches from V_{IN} to V_{OUT} in an inverting topology instead of from V_{IN} to GND in a buck topology. When the high-side MOSFET turns on, the SW node detects the input voltage. When the low-side MOSFET turns on, the SW node detects the device return, which is the output voltage. During start-up, V_{IN} rises to achieve the desired input voltage. The output voltage starts ramping down after the EN pin voltage exceeds its threshold level and V_{IN} exceeds its UVLO threshold. As V_{OUT} continues to ramp down, the SW node low level follows it down. Figure 6 shows the resulting normal and smooth start-up of the output voltage.

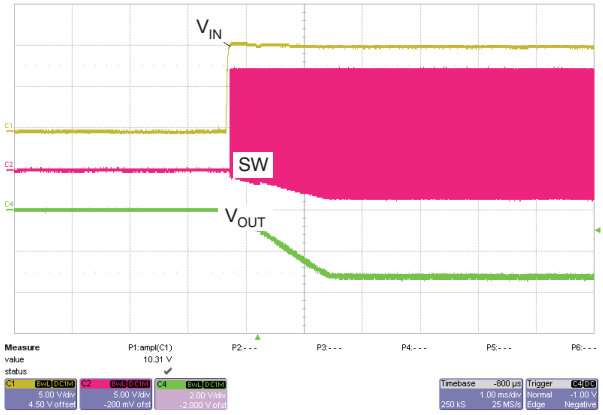

Figure 6. Typical SW Node Characteristic During Start-Up

3 External Components

The TPSM53604 is a power module that integrates a 36-V buck converter, power MOSFETs, and shielded inductor in a compact solution. As a result, using this power module in a buck application only requires as few as four external components. To configure from buck to IBB topology, two additional components (clamp diode and C_{BYPS}) are required for a total passive component count of six.

3.1 Capacitor Selection

Ceramic capacitors with low equivalent series resistance (ESR) are recommended to achieve low output voltage ripple. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. The higher the DC voltage applied to the capacitor, the less the effective capacitance. Use a minimum of 10-µF capacitance for both C_{BYP} and C_{IN}. Making this capacitor value too large can prevent proper start-up operations.

3.2 System Loop Stability

Stability is an important factor in the system when adding more output capacitance. The general rule of thumb for a stable design is a desired phase margin (PM) of at least 45° or greater. In extreme conditions too much output capacitance added to the system may result in a lowered bandwidth and slower transient response. The following table shows the PM for each output voltage selection measured from a TPSM53604EVM modified for inverting buck boost application using the default bill-of-material at room ambient temperature. For other application conditions, it is recommended to design and verify proper stability using a frequency analyzer.

Table 4. Phase Margin of IBB TPSM53604 at 3-A Load Current

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	F_{cross}(kHz)	PM (º)
12	-1.2	3	42	54
12	-1.8	3	31	47
12	-2.5	3	23	65
12	-3.3	3	17	61
12	-5	3	11	59

3.3 UVLO

The EN pin can be used to set the input under voltage lockout (UVLO) with two resistors (R_{ENT} and R_{ENB}). Note that since the return path is now -VOUT, the falling threshold is shifted down by -VOUT. If configurability of both rising and faling input voltage threshold is desired, refer to Figure 10 from the *Working with inverting buck-boost converters* application note. Make sure to not have the EN pin floating.

4 Typical Performance

Unless otherwise stated, the following conditions apply: V_{IN} = 24 V , T_A = 25°C

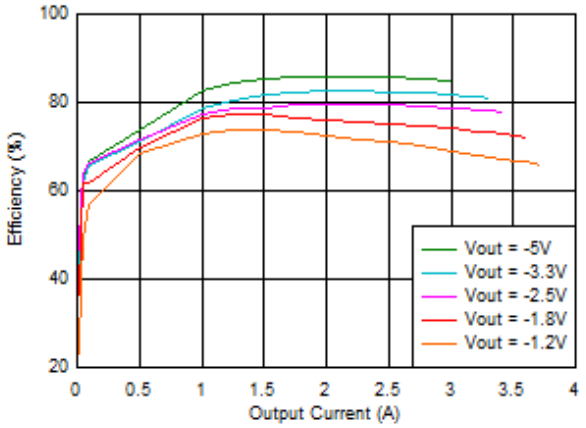

Figure 7. Efficiency

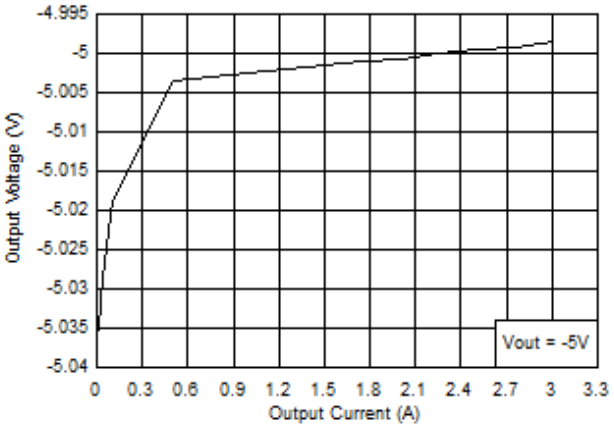

Figure 8. Typical 5-V Output Regulation

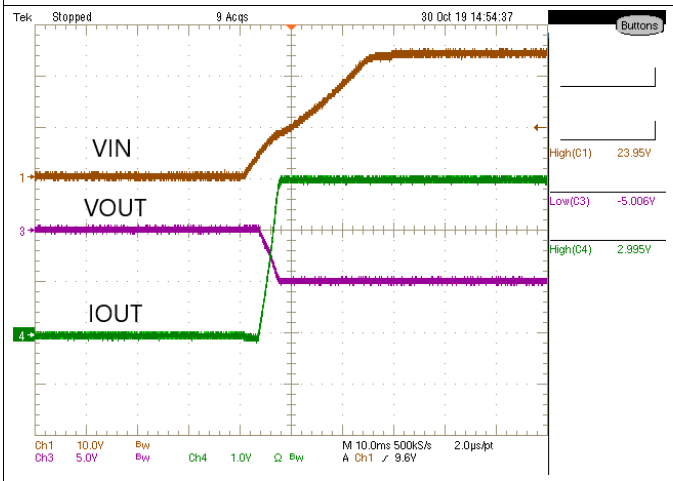

Figure 9. Start-up with 3-A Load

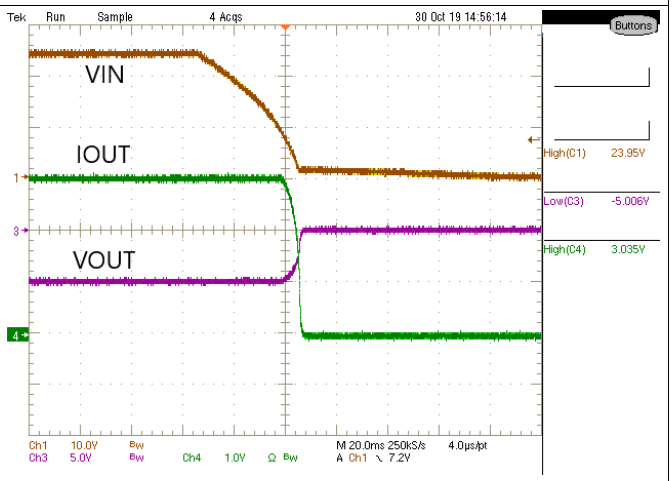

Figure 10. Shutdown with 3-A Load

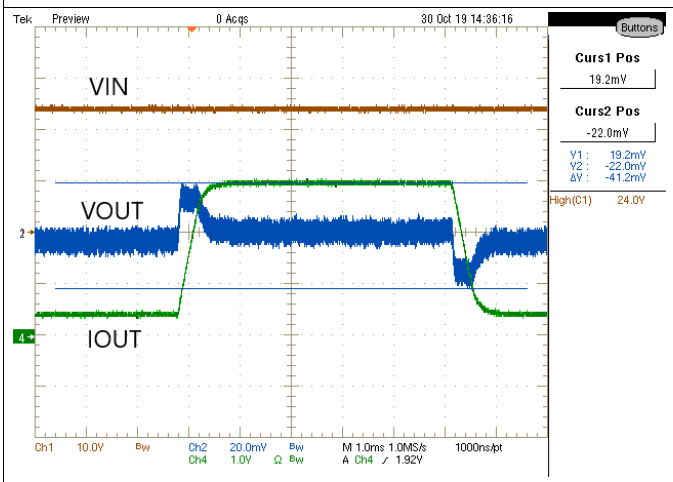

Figure 11. Load Transient With 0.5-A to 3-A Load Step

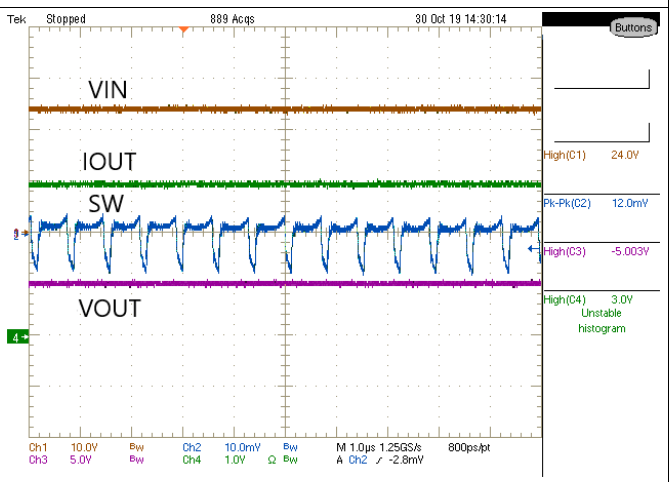

Figure 12. Output Voltage Ripple with 3-A Load

5 Digital Pin Configurations

The system return path in an IBB topology is floated on the negative output voltage. Control signals that were once referenced to ground in a buck configuration must now be level-shifted to the system return path if features such as PGOOD or EN toggle are desired. The following section discusses the external level-shifting circuit required to utilize these functions.

5.1 Digital Input Pin (EN)

If control of the enable feature is desired in a IBB topology, a level shifter is required since the IC providing the EN signal may not be able to produce a negative voltage. Figure 13 is a typical level shifter circuit. Be sure to follow the enable pin voltage rating based on the *Absolute Maximum Ratings* section of the TPSM53604 data sheet. For a robust design, a Zener diode rated below the absolute maximum enable voltage must be placed between EN pin and –VOUT.

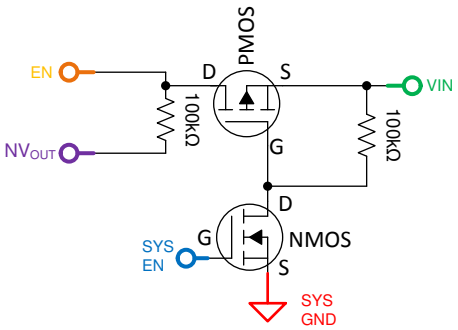

Figure 13. EN Pin Level Shifter

5.2 Power-Good Pin

The TPSM53604 has a built-in power-good (PGOOD) function to indicate whether the output voltage has reached its appropriate level or not. The PGOOD pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC return in this configuration, the PGOOD pin is referenced to V_{OUT} instead of ground, which means that the device pulls PGOOD to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PGOOD pin, because in some applications the IC detecting the polarity of the PGOOD pin may not be able to withstand negative voltages. The level shifter circuit (as shown in Figure 14) alleviates any difficulties associated with the offset PGOOD pin voltages by eliminating the negative output signals of the PGOOD pin.

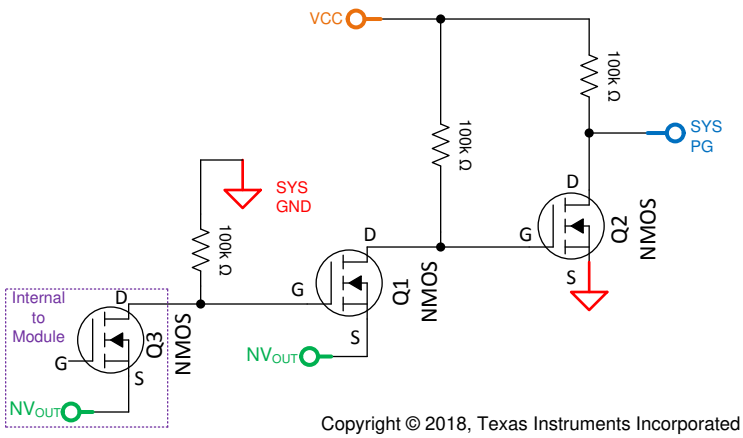

Figure 14. PGOOD Pin Level Shifter

6 Conclusion

The TPSM53604 step-down power module can be configured in an IBB topology to generate a negative output voltage by switching the output and ground connection. The input voltage range is lowered because the device now has a reference point set to the negative output voltage rather than ground. Additionally, the inductor peak current is much higher effectively lowering the recommended maximum output current operating range. Converting an original buck topology into an IBB topology results in a lowered input voltage range and maximum output current. Additional level-shifting circuitry is required to invert the negative output signal if EN and PGOOD pin usage is required.

7 References

The following documents are available for download from the TI web site:

1. Texas Instruments, *Working with inverting buck-boost converters* Application Report
2. Texas Instruments, *Create an Inverting Power Supply From a Step-Down Regulator* Application Report
3. Texas Instruments, *Using a buck converter in an inverting buck-boost topology* Technical Brief

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