Application Report
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Back-Up Power Supply Switchover With Supply Voltage Supervisor and Power Multiplexer / Switch

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ABSTRACT

This application note details a back-up power supply solution that uses a voltage supervisor to monitor a main power rail and if the main power rail falls to an undervoltage condition, a secondary power rail from a back-up battery is automatically switched into the system to provide continuous power to the output. The voltage supervisors serve the purpose of accurately monitoring each power rail and connecting the correct power rail to the output by controlling each power switch. There are voltage supervisors that have built in back-up power supply or battery switchover but these devices can't supply very much power so this solution utilizes power switches and diodes to logic OR the power rails to the output to ensure continuous power. Although this application note uses a back-up battery as the secondary power rail, this solution will work for any secondary power rail.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

There are several key applications that require back-up battery or secondary power rail. In industrial applications, often times if the main power rail fails, a back-up battery is required to supply power to the system long enough to save data or send communications before shutting down. There may be certain actions the system must take to shut down properly which is only possible if there is a secondary power rail. In applications where power is critical for operation or safety, having the ability to switch in a secondary power rail to keep the system from turning off is a key requirement. This solution can be used to create a power supply redundancy for fail-safe applications. In addition, a back-up battery is required in many electronic-point-of-sale (EPOS) applications such as portable POS and POS printers. For the portable or battery powered applications, a back-up battery is used to preserve data and send communications if needed before shutting down. Often times these devices utilize volatile memory such as DDR SDRAM to save data and volatile memory requires power otherwise the data is lost. For POS printers, continuous power is required in the case the main power rail fails and the printer is in the middle of printing. If the main power rail fails, the printer needs to switch to a battery back-up to allow printing to finish.

This application note features a nano-Iq (120 nA typical), very accurate (0.5% typical) voltage supervisor TLV840 to accurately monitor each power rail without requiring significant supply current. TLV840 also features programmable reset delay which allows programmable delays before switching from the secondary power rail back to the main power rail to prevent the possibility of switching back to the main power rail before it is stable. TLV840 is ideal for low voltage rails as the supply voltage range is 0.7 V to 5.5 V. If the power rails are higher than 5.5 V, please consider TPS3840 which has a supply voltage range 1.5 V to 10 V.

2 Solution Overview Using Power Switch / LDO

The proposed solution shows how the supply voltage supervisors can be used to switch the power rail from the Primary VDD (PVDD) to Battery VDD (BVDD) when the PVDD crosses the desired under-voltage threshold (VIT-) while driving the load (Eg. Microcontroller). This is accomplished by the voltage supervisors controlling the Power Switch PS/LDO thereby ensuring continuous power to the load. Below table gives the summary of components the respective quantities for implementing this solution.

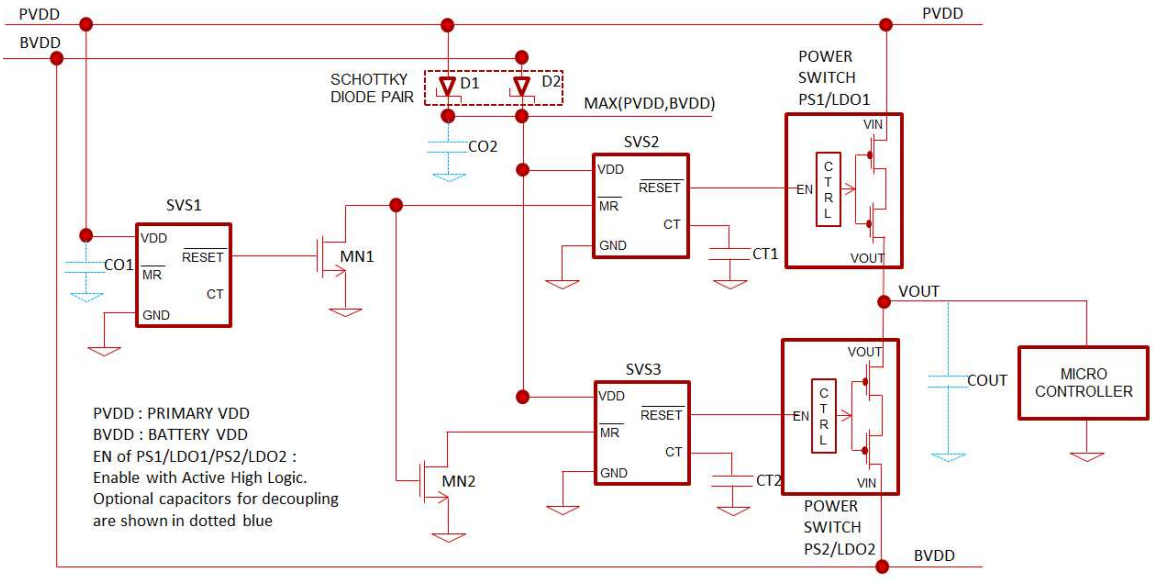

Figure 1. Back-up Battery Switchover Solution Block Diagram

Table 1. Solution Components

S No	Component	Quantity
1	Supply Voltage Supervisors (SVS) with factory trimmed under-voltage threshold, $\overline{MR}$, and programmable reset delay	3
2	Discrete NMOS	2
3	Schottky diode pair on the power line	1
4	Discrete capacitors	2
5	Optional capacitors	3
6	Power switch / LDO with active-high ENABLE	2

The pin-outs shown are only for reference and do not reflect the actual pin-outs of the chip. Please refer to the datasheet for the correct pin-outs. The Power Switch PS/LDO shown are for illustration only. Table 3 gives guidelines on how to select the supervisor based on the requirements. The description assumes all the SVS are push-pull active-low voltage supervisors.

To begin, SVS1 senses the PVDD line directly and provides $\overline{RESET}$ logic high when PVDD crosses the factory set rising threshold (VIT+) while ramping up. This, in turn, turns ON the NMOS MN1. MN1 drain is connected to the $\overline{MR}$ pin of SVS2. Push-pull active-low logic is converted to open-drain active-high logic using the discrete NMOS. The main function of $\overline{MR}$ is to keep $\overline{RESET}$ logic low when $\overline{MR}$ is set to logic low. This will turn ON the power wwitch (PS1)/LDO1 thereby connecting PVDD to VOUT. MN1 drain is also connected to the gate of NMOS MN2. MN1 drain pulled to logic low will turn OFF MN2. This will set $\overline{MR}$ of SVS3 logic high. When MR is set to logic high, $\overline{RESET}$ is determined by its VDD and the set threshold. The set thresholds are chosen in such a way that the $\overline{RESET}$ will provide logic high. This will turn OFF the power switch (PS2)/LDO2 which will disconnect BVDD line from VOUT. Please choose a Power Switch or LDO which has internal reverse current protection otherwise there can be leakage of current from VOUT to BVDD. MR has an internal pull-up resistor to its VDD. Hence separate discrete resistor is not required in this solution thereby saving the board space. The supervisors SVS2 SVS3 are directly operating from the supply which is the higher voltage rail between PVDD BVDD achieved through two Schottky diodes. This ensures that the SVS2 SVS3 are always powered irrespective of the status of PVDD. MN1 is performing level shifting operation by converting logic from PVDD line to MAX (PVDD,BVDD) line.

Figure 2 shows the pictorial representation of the functionality when PVDD crosses the rising threshold (VIT+) of SVS1.

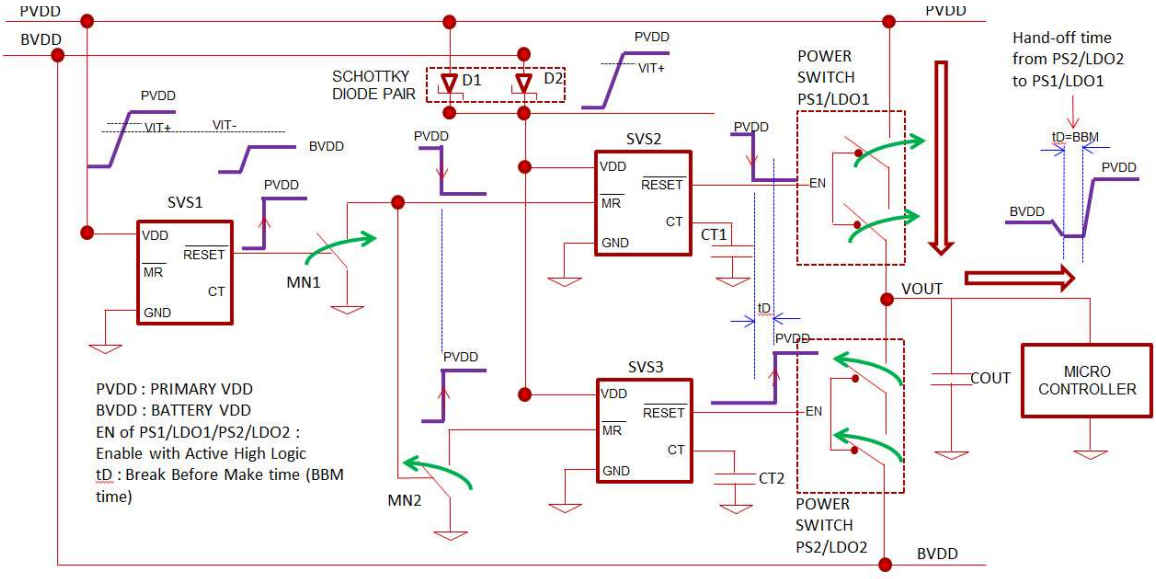

Figure 2. Back-up Battery Switchover Solution with PVDD Rising Block Diagram

If PVDD crosses the undervoltage threshold (VIT-) of SVS1 during ramp down. $\overline{\text{RESET}}$ transitions logic low which in turn turns OFF MN1. The drain of MN1 is automatically set to logic high through pull-up resistance connected at $\overline{\text{MR}}$ of SVS2 which de-asserts $\overline{\text{RESET}}$ so $\overline{\text{RESET}}$ transistions to logic high thereby turning OFF Power PFET PP1 and disconnecting PVDD rail from VOUT. Meanwhile, MN2 turns ON due to $\overline{\text{MR}}$ of SVS2 being logic high. This will pull $\overline{\text{MR}}$ of SVS3 to logic low and asserts $\overline{\text{RESET}}$ by setting it to logic low turning ON the Power PFET (PP2) thereby resulting in the connection of BVDD rail to VOUT as shown in Figure 3.

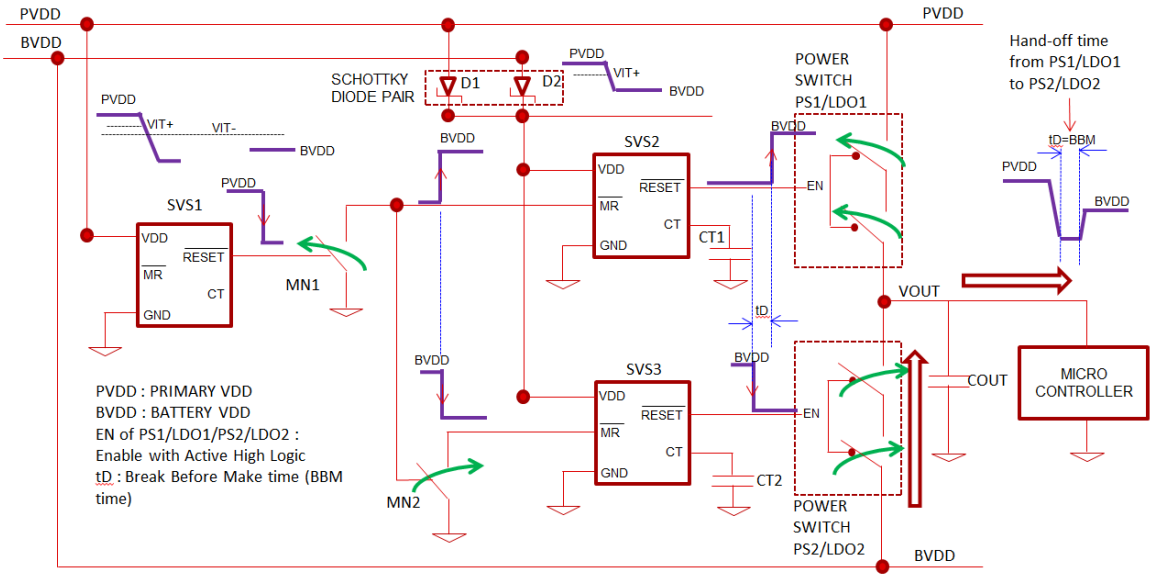

Figure 3. Back-up Battery Switchover Solution with PVDD Falling Block Diagram

In both of the cases above, it is ensured that the PVDD BVDD never get shorted under steady state condition. During the transition between PS1/LSO1 PS2/LDO2, it's important that PVDD BVDD are not connected through switches as it can damage the source. This is achieved using CT1 CT2. The main responsibility of the CT pin is to provide reset delay between the rising threshold (VIT+) of VDD or the $\overline{\text{MR}}$ transitioning to logic high before the$\overline{\text{RESET}}$ transitions to logic high. The desired delay can be set by the user using the below equation and the desired capacitance value. The addition of CT cap will not affect the delay between falling threshold (VIT-) of VDD and RESET going low.

2.1 Calculating Reset Delay

Use Equation 1 to calculate the capacitor value in Farads for a desired delay in seconds.

$$C_{CT\_EXT} = (t_D - 50\ \mu s) \div 618937 \quad (1)$$

Where t_D represents the desired delay between rising threshold (VIT+) of SVS and the $\overline{\text{RESET}}$ pin transitioning to logic high.

The delay time (t_D) set by CT1 and CT2 for SVS2 and SVS3 respectively set the "break before make" or BBM timing which protects the system and prevents an accidental short between PVDD and BVDD. If there is no delay between PVDD turning off and BVDD turning on (or vice versa), there is a direct short between the two supplies thus the reset delays are required to prevent a "break before make" situation. This also provides the user with adjustable delay when powering up or when switching back to the primary power supply from the back-up supply by adjusting CT1 and CT2. The design example shows how the delay helps in avoiding the short between PVDD and BVDD because each TLV840 voltage supervisor uses a 1 nF capacitor on the CT pin to set the reset delay to 1 ms to prevent any device from enabling a power switch before the other has disabled. The VOUT is momentarily floating during this switchover time. The user must decide the delay based on the loading conditions. If board area permits for the given load, a small capacitance can be added to the VOUT pin to support the load during the switchover time. The capacitor value at VOUT is chosen so that the capacitor maintains the output voltage during the delay times set by CT1 and CT2. By increasing the delay times to prevent accidental shorting of the two supplies, a larger value capacitor at VOUT can be used.

2.2 Choosing the Power Switch (PS) or LDO

This solution uses a PMOS based power switch (TPS22810) that has internal reverse current protection. The power PMOS ON resistance can be chosen based on the desired load current. The current solution easily accepts any power switch or LDO with active-high ENABLE option. Active-low ENABLE devices can be used but the voltage supervisors selected must be active-high in that case. The LDOs / power switches must be selected such that the outputs can be connected together without issue although only one LDO / power switch will be turned ON at any given time because of the ENABLE control provided by the voltage supervisors SV2 and SV3.

2.3 Choosing the Discrete NMOS

This solution uses a discrete NMOS (CSD13380F3). The discrete NMOS needs to be chosen based on the minimum threshold voltage required. The SVS provides a guaranteed output at V_{POR} condition. V_{POR} is the VDD voltage at which $\overline{\text{RESET}}$ is in a defined logic state. Select the NMOS which has minimum threshold voltage (V_T) higher than the max V_{POR}spec of the SVS driving it. The open-drain NMOS functions as a level shifting inverter. Level shifting is required because connecting PVDD to MAX(PVDD, BVDD) will result in logic error. This also avoids one PMOS coming from the inverter which saves board space.

2.4 Choosing SVS1

Whenever PVDD crosses VDD_{min} of SVS1 during ramp down and comes back above the rising threshold (VIT+), the delay time between the VDD and $\overline{\text{RESET}}$ transitioning to logic high will be start-up time (t_{STRT}) plus the reset time delay (t_D). Select the supervisor based on the PVDD behavior and the desired reset time delay. If this start-up time is not desired, please use a supervisor which has separate SENSE and VDD pins. Connect SENSE to PVDD and VDD to MAX(PVDD, BVDD) which ensures the continuous operation of SVS1. Also, use a decoupling capacitor between VDD and GND on any SVS to take care of voltage transients on the supply voltage.

2.5 Selecting the Threshold of SVS2 and SVS3

The voltage thresholds of SVS2 and SVS3 are selected based on the minimum PVDD and BVDD at which the user is interested to operate the system. Setting the threshold of SVS2 and SVS3 less than the minimum of lowest PVDD and lowest BVDD ensures the continuous powering of these supervisors.

2.6 Solution Functional Modes

Table 2 summarizes the various functional modes of the system.

Table 2. Solution Power Supply Logic

S No	Primary VDD (PVDD)	Battery VDD (BVDD)	VOUT
1	PVDD < VIT-	BVDD > VIT+	BVDD
2	PVDD < VIT-	BVDD < VIT-	hold previous state
3	PVDD > VIT+	—	PVDD

2.7 Selecting the Voltage Supervisor Based on PVDD

Table 3 provides guidelines on selecting the correct voltage supervisor based on the primary voltage of the system. TLV840 is recommended for primary voltage supply (PVDD) between 0.7 V and 6 V. TPS3840 is recommended for primary voltage supply (PVDD) between 1.7 V and 10 V.

Table 3. Voltage Supervisor Device Recommendations

S No	Primary VDD (PVDD)	SVS1	SVS2 and SVS3	Description
1	0.7 V < PVDD < 6 V	TLV840	TLV840	Low Iq, lower range of input voltage, adjustable delay with CT capacitor
2	1.7 V < PVDD < 10 V	TPS3840	TPS3840	Low Iq, higher range of input voltage, adjustable delay with CT capacitor
3	1.7 V < PVDD < 6 V	TLV809E	TLV809E	Low cost, low Iq, fixed reset delay (no CT capacitor required), small X2SON package available

3 Design Example

The requirements of this design are monitor a primary power supply of 3.5 V, and when the primary supply voltage falls to 3.0 V, switch to a back-up secondary (battery) supply. The secondary supply of 3.2 V maintains operation until the secondary supply drops to 2.9 V, then the system shuts off until either power supply returns to 5% above the undervoltage threshold for each device for at least the programmed reset delay. The battery switchover circuit design uses three TLV840 devices as shown in Figure 4.

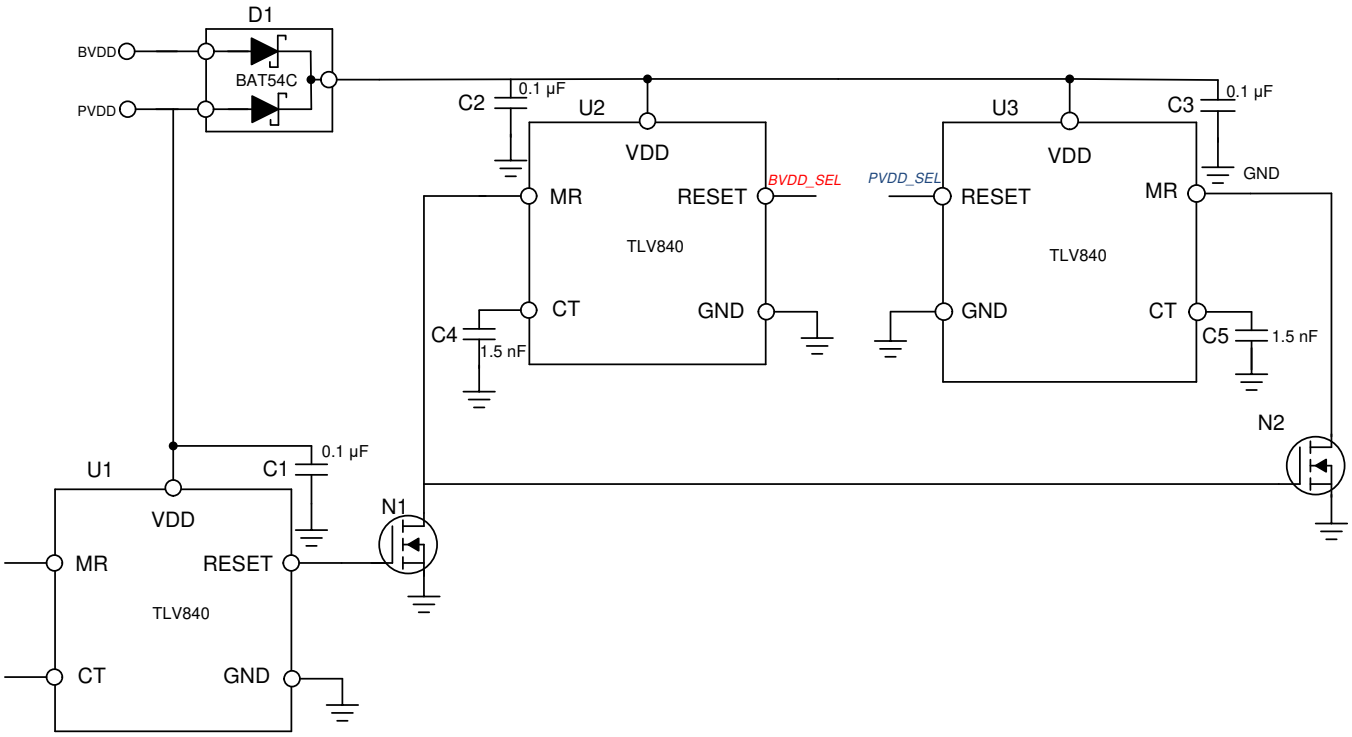

Figure 4. Solution Circuit Schematic for Simulation

3.1 Design Procedure

The design begins with the voltage supervisors that will monitor each supply. The TLV840CADL29 is selected to monitor the primary 3.5 V rail because the undervoltage threshold is 2.9 V. Similarly, the TLV840CADL28 is selected to monitor the secondary battery supply because the undervoltage threshold is 2.8 V. The TLV840 device family has built-in hysteresis of 5% and programmable reset delay to prevent the system from returning from undervoltage condition prematurely or from enabling both supplies at the same time. Using a 1.5 nF capacitor on the CT pin sets the reset delay to 1 ms. The design specifications are displayed in Table 4.

Table 4. Design Example Specifications

Parameter	Specification	Description
Primary supply (PVDD)	Switching from 3.5 V to 0 V	PVDD switching to 0 V represents primary rail supply failure
Battery back-up supply	3.2 V	Battery voltage is constant and available to switch to during primary rail supply failure
C7, C8	1.5 nF	Provides a reset delay time of 1 ms
VIT- for primary supply	3.0 V	Provided by TLV840CAPL30
VIT- for secondary supply	2.9 V	Provided by TLV840CAPL29

3.2 Simulation for Design Example

The design example in Figure 4 is simulated to show the functionality. PVDD_SEL and BVDD_SEL represent the signals that enable the power switch or LDO of the primary supply and secondary supply respectively. During a primary supply failure, PVDD_SEL transitions logic low after t_{P_HL} time (typically 40 µs) which disables the power switch/LDO of the primary supply but BVDD_SEL won't transistion logic high until after the programmed reset delay of 1 ms set by the 1.5 nF capacitor which gives sufficient time to prevent the primary and secondary supplies from shorting. When the primary supply powers up, BVDD_SEL transitions logic low after startup time + t_{P_HL} (typically 190 µs) and PVDD_SEL transitions logic high after the programmed reset delay time of 1 ms set by the 1.5 nF capacitor.

3.2.1 Results for PVDD_SEL

The results for the PVDD_SEL simulation are shown in Figure 5. The green trace is PVDD and the blue trace is the $\overline{\text{RESET}}$ of PVDD_SEL supervisor.

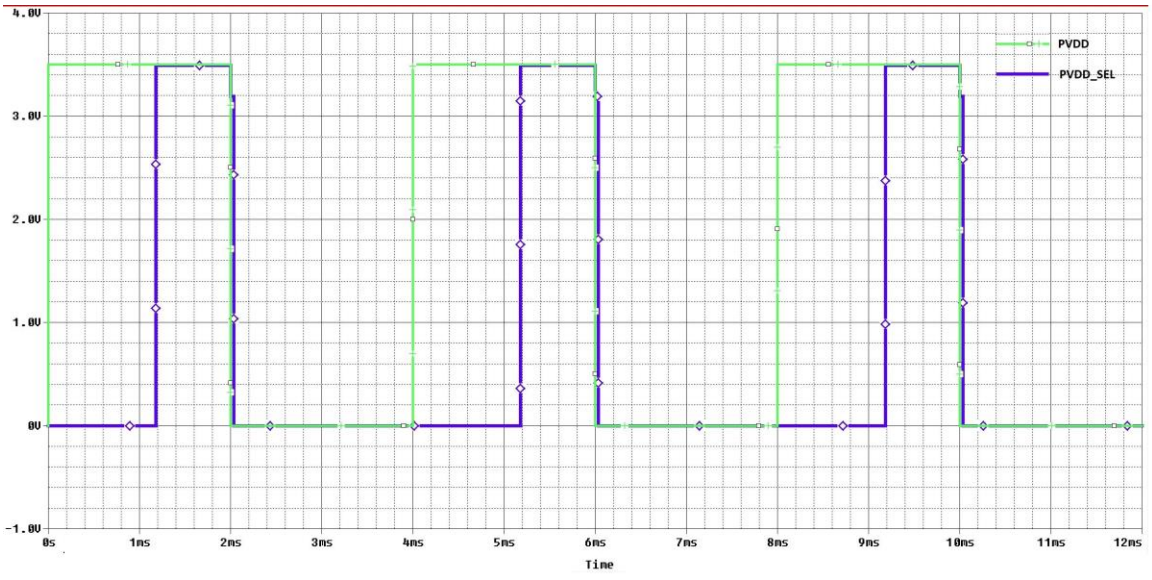

Figure 5. Simulation Results for PVDD_SEL

When PVDD signal falls to the undervoltage threshold of 3.0 V, battery select signal, BVDD_SEL transitions high after 1 ms to prevent both supplies from connecting to each other. When PVDD signal rises above 5% over the undervoltage threshold, battery select signal transitions low after T_{P_HL} propagation delay time, and PVDD_SEL signal rises after 1 ms, again to prevent both supplies from connecting to each other.

3.2.2 Results for BVDD_SEL

The results for the BVDD_SEL simulation are shown in Figure 6. The green trace is PVDD and the red trace is the $\overline{\text{RESET}}$ of BVDD_SEL supervisor.

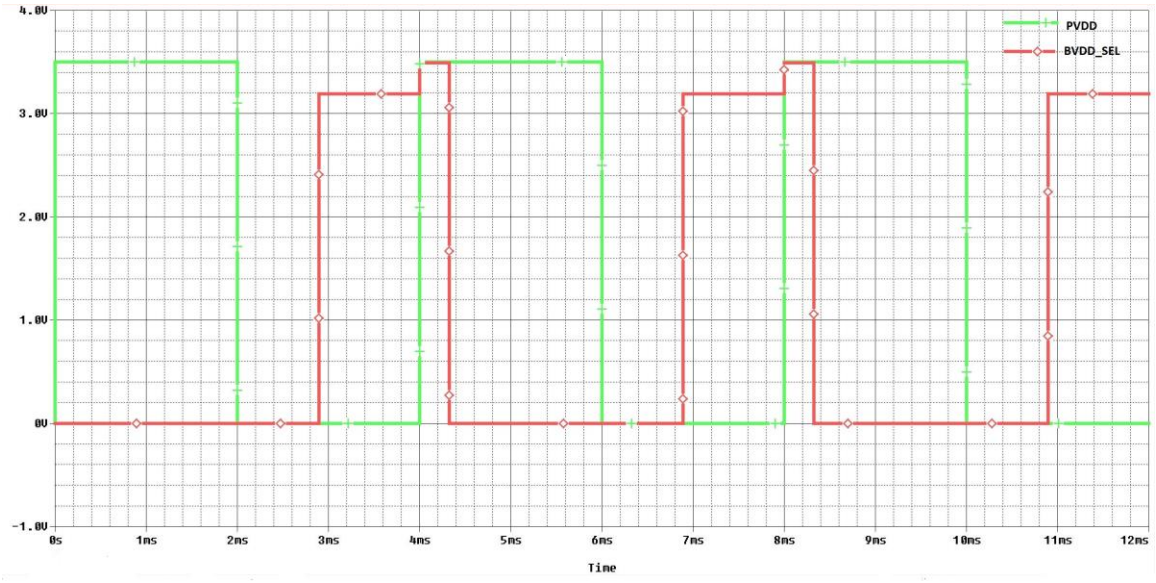

Figure 6. Simulation Results for BVDD_SEL

When PVDD signal falls below the undervoltage threshold of 3.0 V, the battery select signal, BVDD_SEL, transistions to logic high after 1 ms to prevent the two supplies from connecting to each other. When PVDD signal rises above 5% over the undervoltage threshold, the battery select signal transitions low after startup time + t_{P_HL} and the primary supply select signal, PVDD_SEL, transitions high after 1 ms to prevent the supplies from connecting to each other.

4 References

The documents below provide additional information on the devices used in this solution.

- TLV840 Datasheet
- TPS3840 Datasheet
- TLV809E Datasheet

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