*Application Report*

# *Inverting Application for the TPSM5601R5H*

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**ABSTRACT**

The TPSM561R5H is a 1.5-A rated, synchronous step-down power module that features a wide operating input range from 4.2 V to 60 V, and an adjustable output voltage range from 1 V to 16 V. The TPSM5601R5H can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted (negative with respect to the input voltage). This application report demonstrates how the conventional, non-inverting evaluation board for the TPSM5601R5H can be configured for an inverting application and provides the additional level-shifter circuitry for the enable (EN) and power good (PGOOD) pins (if the feature is required).

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# 1 Inverting Buck-Boost Topology

## 1.1 Concept

In a standard buck module configuration, the positive output connection ($V_{OUT}$) is connected to the internal inductor and the return connection is to the device ground (PGND).

In the IBB configuration, the system ground (SYS_GND) is connected to the $V_{OUT}$ of the device and the device return path is now the negative output voltage ($-V_{OUT}$). Therefore, the buck output is now the system ground, and the buck "ground" becomes the negative output voltage. This shift in topology allows the output voltage to be inverted (with respect to the input voltage).

## 1.2 Basic Configuration

Figure 1-1 shows the connections for taking the buck regulator and converting it into an IBB.

The connection changes are detailed in the following list:

1. Reassign the buck positive output as system ground.
2. Reassign the buck regulator ground nodes as the negative output voltage node.
3. Positive input remains the same.

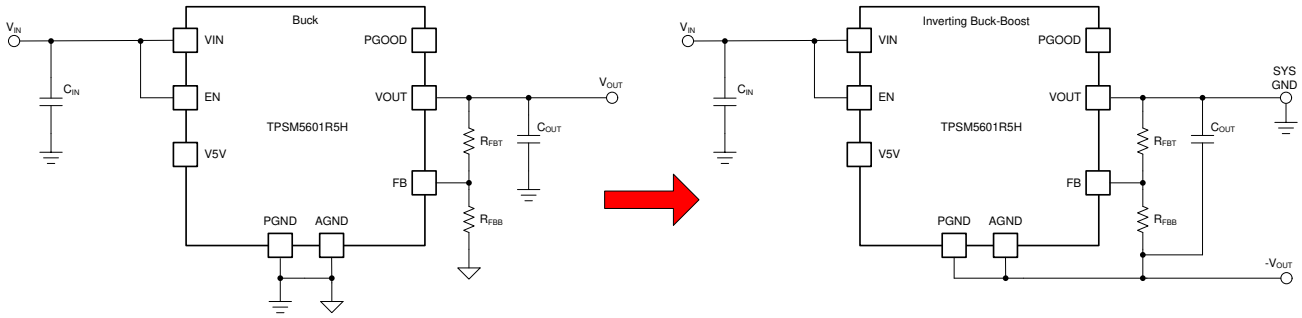


**Figure 1-1. Converting From Buck to Inverting Buck-Boost Topology**



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# 2 Design Parameters

## 2.1 Output Current Calculations

The peak current limit of the converter indicates the maximum peak inductor current which limits the output current (similar if implementing valley current limit). In the IBB configuration, the inductor current and peak switching currents are larger than in the equivalent buck converter. Consequently, the output current capability in the IBB topology is less than the buck configuration for the same current limit specifications. The maximum achievable current is calculated by Equation 1.

$$I_{OUT}\,(IBB) = I_{L_MAX} \times (1 - D) \tag{1}$$

where

- $I_{L_MAX}$ is the maximum rated inductor current
- D is the operating duty cycle

Calculate the operating duty cycle for an inverting buck-boost converter using Equation 2.

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + (V_{IN} \times \eta)} \tag{2}$$

where

- η = Efficiency

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. Given that the IBB configuration yields different efficiency values compared to a buck, use a conservative value or see Table 2-1 or Figure 5-1 for typical efficiency values. Use Equation 2 to find the expected duty cycle, then use Equation 1 to calculate the recommended maximum output current. For example, in a 24-V input voltage, –5-V output voltage system, the duty cycle is:

$$D = \frac{|-5|}{|-5| + (24 \times 0.78)} = 0.211 \tag{3}$$

The result of Equation 3 is then used to calculate the maximum recommended output current:

$$I_{OUT}\,(IBB) = 1.5 \times (1 - 0.211) = 1.184\ A \tag{4}$$

Table 2-1 and Figure 2-1 provide a general idea of the recommended maximum output current allowed from the TPSM5601R5H in an inverting configuration, with given typical efficiency values.

**Table 2-1. Recommended Maximum Output Current Calculations for IBB TPSM5601R5H**

| $V_{OUT}$ (V) | $V_{IN}$ (V) | $I_{L_MAX}$ (A) | η | *D* | $I_{OUT}$ (A) |
|---|---|---|---|---|---|
| –2.5 | 24 | 1.5 | 0.69 | 0.131 | 1.303 |
| –3.3 | 24 | 1.5 | 0.73 | 0.159 | 1.262 |
| –5 | 24 | 1.5 | 0.78 | 0.211 | 1.184 |
| –12 | 24 | 1.5 | 0.83 | 0.376 | 0.936 |
| –15 | 24 | 1.5 | 0.84 | 0.427 | 0.860 |



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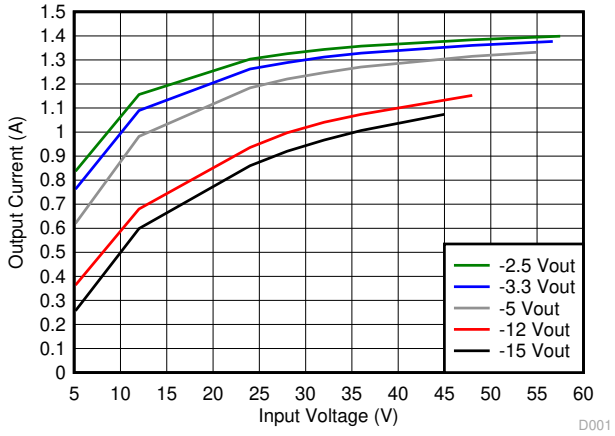


**Figure 2-1. Recommended Maximum Output Current**

## 2.2 $V_{IN}$ and $V_{OUT}$ in an Inverting Configuration

When configured in an IBB topology, the voltage across the device is equal to the input voltage minus the output voltage (where the output voltage is a negative value). One must make sure to keep the voltage across the device less than the specified maximum input voltage ($V_{IN_MAX}$) of the device. The maximum input voltage in an IBB configuration can be calculated by using Equation 5.

$$V_{IN_MAX}\,(IBB) = V_{IN_MAX} - |V_{OUT}| \tag{5}$$

where

- $V_{IN_MAX}$(IBB) is the maximum voltage across the device
- $V_{IN_MAX}$ is the specified maximum input voltage of the device
- $V_{OUT}$ is the negative output voltage

As a result, in an IBB configuration the input voltage range is reduced. For example, the TPSM5601R5H has an input voltage range of 4.2 V to 60 V. Therefore, for a desired output voltage of –5 V, the input voltage now has an operating range of 4.2 V to 55 V.



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# 3 Design Considerations

## 3.1 Additional Bypass Capacitor and Schottky Diode

A ceramic bypass capacitor, $C_{BYP}$, with a minimum capacitance of 10 µF is recommended to be placed from $V_{IN}$ to $–V_{OUT}$. $C_{BYP}$ can help filter the input voltage and minimize interference with other circuits. The voltage rating of the capacitor must be taken into consideration because it will experience stress equal to the full voltage range between $V_{IN}$ and $V_{OUT}$.

Consider that the inclusion of the bypass capacitor introduces an AC path from $V_{IN}$ to $V_{OUT}$ and might worsen the transient response. When $V_{IN}$ is applied to the circuit, this *dV/dt* across $C_{BYP}$ creates a current that must return to ground to complete the loop. This current might flow through the internal low-side body diode of the MOSFET and inductor to return to ground. For this case, it is recommended to have a Schottky diode between $–V_{OUT}$ and SYS_GND as in Figure 3-1. If large-line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

It is also recommended that a capacitor, $C_{BULK}$, is placed at the input power supply to help dampen the high-frequency noise that can couple onto the circuit. An electrolytic capacitor with moderate ESR helps dampen any input supply ringing caused by long power leads. When using the TPSM5601R5HEVM, adding a $C_{BULK}$ capacitor across $V_{IN}$ and SYS_GND is recommended.

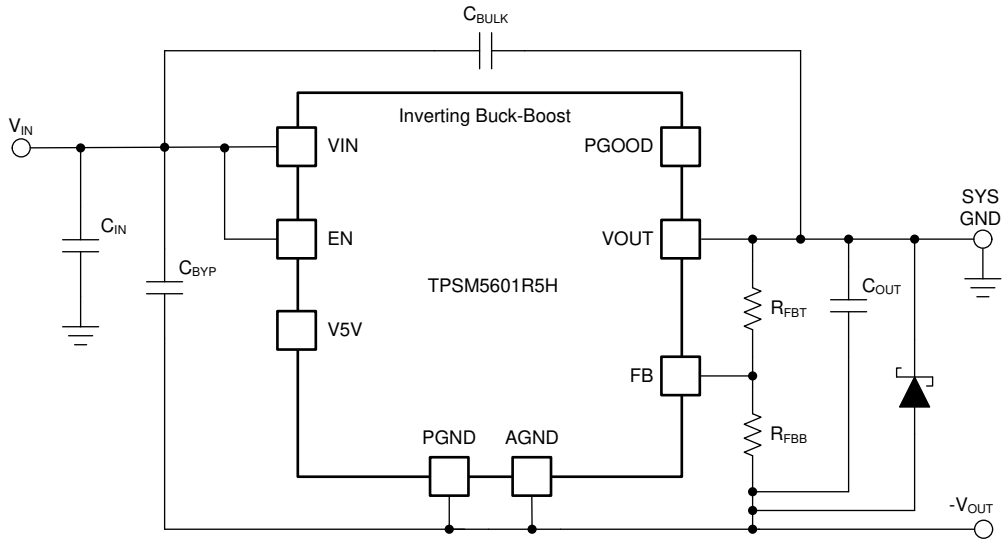


**Figure 3-1. TPSM5601R5H Inverting Buck-Boost Schematic with Schottky Diode**

## 3.2 Switching Node Behavior

The voltage on the switch node switches from $V_{IN}$ to $–V_{OUT}$ in an inverting topology instead of $V_{IN}$ to GND as in a buck topology. When the high-side MOSFET turns on, the SW node detects the input voltage. When the low-side MOSFET turns on, the SW node detects the device return path, which is the negative output voltage. During start-up, $V_{IN}$ rises to achieve the desired input voltage, then $V_{OUT}$ starts ramping down after the EN pin voltage exceeds its threshold level and $V_{IN}$ exceeds its UVLO threshold. As $V_{OUT}$ continues to ramp down, the SW node low level follows $V_{OUT}$ down. Figure 3-2 shows the resulting normal and smooth start-up of the output voltage.


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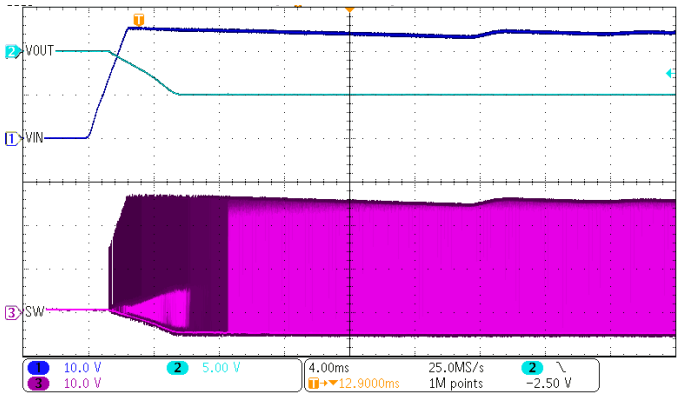


**Figure 3-2. SW Node Voltage During Start-Up**

## 3.3 Enable Pin (EN)

In an IBB configuration, because the EN pin is referenced to $V_{OUT}$ instead of 0 V, the EN voltage thresholds are affected. In a buck configuration, the specified typical threshold voltage for the EN pin with respect to the return path (GND pin) of the IC is considered high at 1.2 V and low at 1.12 V. In the inverting buck-boost configuration, however, $V_{OUT}$ is the reference; therefore, further pushing the device into an enabled state. The high EN threshold is determined by 1.2 V + $V_{OUT}$ and the low threshold is determined by 1.12 V + $V_{OUT}$. For example, if $V_{OUT}$ = –5 V, $V_{EN}$ is high for voltages above –3.8 V and low for voltages below –3.88 V.

This behavior can cause difficulties enabling or disabling the device. The level shifter alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.

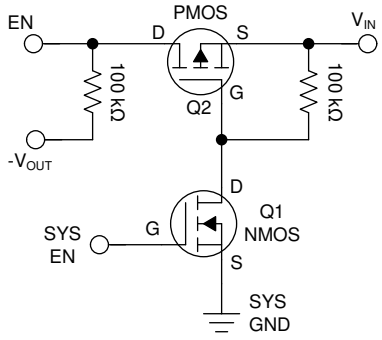


**Figure 3-3. EN Pin Level Shifter Circuit**

The positive signal (SYS_EN) that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN is grounded), Q2 detects 0 V across its $V_{GS}$ and also remains off. In this state, the EN pin detects $V_{OUT}$, which is below the low level threshold and disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (gate threshold voltage as specified in the data sheet of the MOSFET), the gate of Q2 is pulled low through Q1. This drives the $V_{GS}$ of Q2 negative and turns Q2 on. As a consequence, $V_{IN}$ ties to EN through Q2, and the pin is above the high level threshold, causing the device to turn on. Make sure that the $V_{GD}$ of Q2 remains within the ratings of the MOSFET ratings during both enabled and disabled states. Also ensure that $V_{GS}$ and $V_{DS}$ ratings are not exceeded. Failing to adhere to these constraints can result in damaged MOSFETs.

The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the output of the circuit and goes from $V_{IN}$ to $–V_{OUT}$ properly enabling and disabling the device.



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### 3.4 Power-Good Pin (PGOOD)

The TPSM5601R5H has a built-in power-good (PGOOD) function to indicate proper output voltage regulation. The PGOOD pin is an open-drain output that requires a pullup resistor. Because $-V_{OUT}$ is the return path of the IC in IBB topology, the PGOOD pin is referenced to $-V_{OUT}$ instead of system ground, which means that the device pulls PGOOD to $-V_{OUT}$ when it is low.

This behavior can cause difficulties in reading the state of the PGOOD pin, because in some applications the IC detecting the polarity of the PGOOD pin may not be able to withstand $|-V_{OUT}|$. The level shifter circuit alleviates any difficulties associated with the offset PGOOD pin voltages by translating the negative output signals of the PGOOD pin. If the PGOOD pin functionality is not needed, it may be left floating or connected to $-V_{OUT}$ without this circuit.

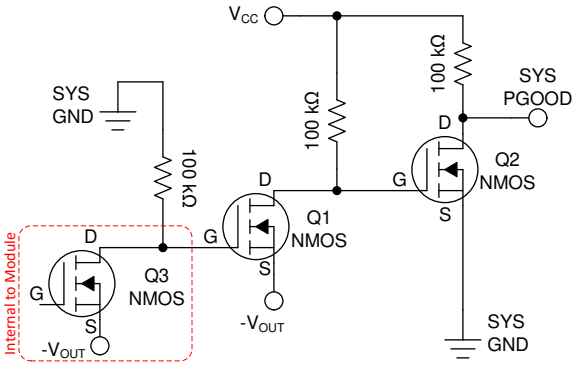


**Figure 3-4. PGOOD Pin Level Shifter**

Inside these devices, the PGOOD pin is connected to an N-channel MOSFET (Q3). By tying the PGOOD pin to the gate of Q1, when PGOOD is pulled low by the module, Q1 turns off and Q2 turns on because its $V_{GS}$ detects the $V_{CC}$ pull-up. Therefore, this pulls SYS_PGOOD to SYS_GND.

When Q3 turns off, PGOOD pin is pulled high (gate of Q1) to ground potential therefore turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PGOOD is then pulled up to the $V_{CC}$ voltage. Note that the $V_{CC}$ voltage must be at an appropriate logic level for the circuitry connected to the SYS_PGOOD net.


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# 4 External Components

The TPSM5601R5H power module integrates power MOSFETs and a shielded inductor. As a result, this application only requires as few as four external components. To configure from buck to IBB topology, two additional components are recommended (clamp diode and $C_{BYP}$) for a total passive component count of six.

## 4.1 Capacitor Selection

Ceramic capacitors with low equivalent series resistance (ESR) are recommended to achieve low output voltage ripple. X5R and X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. Higher DC bias results in decreased capacitance based on the capacitors specifications. Use a minimum of two 4.7-µF capacitance for $C_{IN}$ and a 10-µF for $C_{BYP}$. Making this capacitor value too large can prevent proper start-up operations. Evaluating the Bode plot of the circuit under normal operation can provide insight on the stability of the system.

## 4.2 System Loop Stability

Stability is an important factor in the system when adding more output capacitance. The guideline for a stable design is a desired phase margin of at least 45°. In extreme conditions too much output capacitance added to the system results in a lowered bandwidth and phase margin less than 45°. Table 4-1 shows the phase margin for each output voltage selection measured from the original BOM ($C_{OUT}$ = 2 × 4.7 µF) of the TPSM5601R5HEVM.

**Table 4-1. Phase Margin of IBB TPSM5601R5H**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $I_{OUT}$ (A) | $F_{crossover}$ (kHz) | Phase Margin (°) |
|---|---|---|---|---|
| 24 | –2.5 | 1.35 | 19.13 | 54.4 |
| 24 | –3.3 | 1.3 | 19.03 | 57.0 |
| 24 | –5 | 1.24 | 18.15 | 54.7 |
| 24 | –12 | 1.0 | 13.90 | 54.3 |
| 24 | –15 | 0.92 | 12.22 | 53.7 |

Additionally, too much output capacitance can falsely trigger hiccup-mode in the TPSM5601R5H. After start-up, hiccup mode is a feature in the module that protects the device against output short-circuit conditions. In this mode the high-side and low-side MOSFETs power off and wait for a fixed hiccup time interval before restarting the device operation. Larger output capacitance results a longer charge time of the capacitors to meet the desired output voltage. The device can see this as a false short circuit condition and trigger hiccup mode.



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# 5 Typical Performance

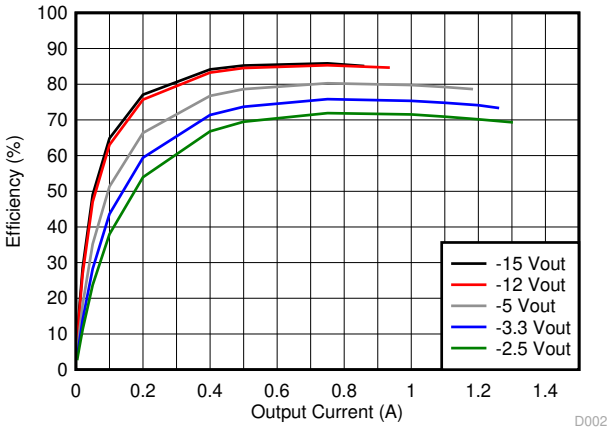


**Figure 5-1. Efficiency at $V_{IN}$ = 24 V**

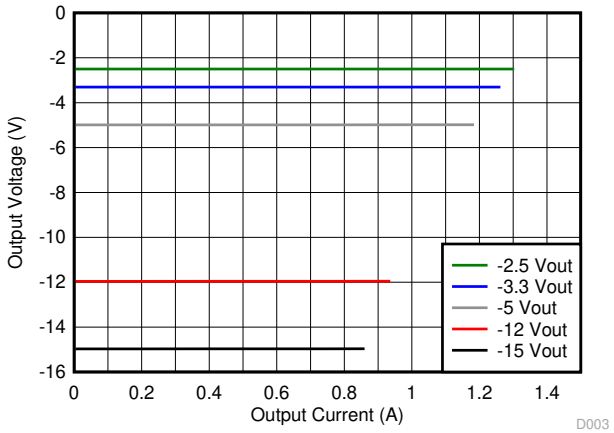


**Figure 5-2. Load Regulation at $V_{IN}$ = 24 V**

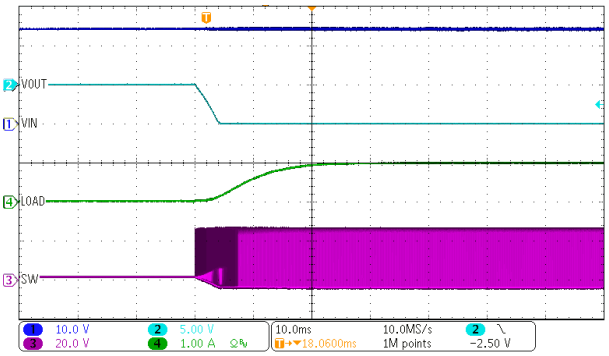


**Figure 5-3. Enable Turn-On on $V_{IN}$ = 24 V, $V_{OUT}$ = –5 V With 1-A Load**

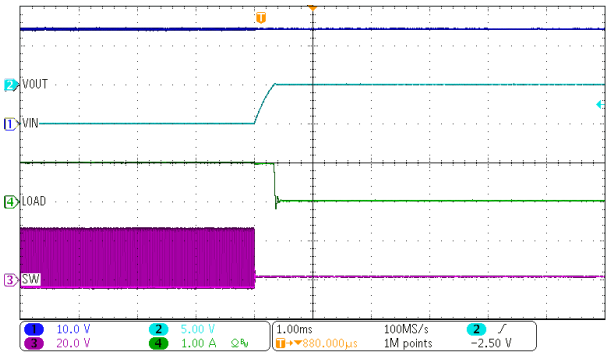


**Figure 5-4. Enable Turn-Off on $V_{IN}$ = 24 V, $V_{OUT}$ = –5 V With 1-A Load**

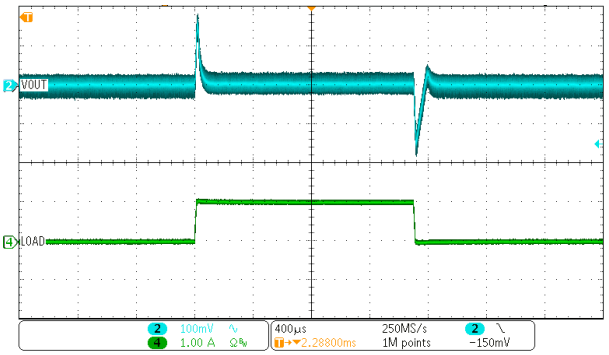


**Figure 5-5. Load Transient Response, 0 A to 1 A With $V_{IN}$ = 24 V, $V_{OUT}$ = –5 V**

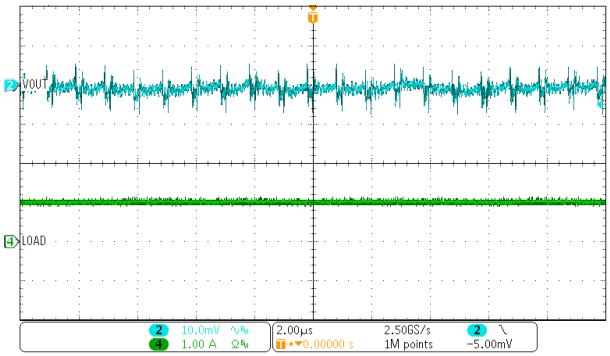


**Figure 5-6. Output Voltage Ripple, $V_{IN}$ = 24 V, $V_{OUT}$ = –5 V With 1-A Load**



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## 6 Summary

The TPSM5601R5H step-down power module can be configured in an IBB topology to generate a negative output voltage by switching the output and ground connections. Converting an original buck topology into an IBB topology reduces the input voltage range and maximum output current. The input voltage range is reduced because the device now has a reference point set to the negative output voltage rather than ground. Additionally, the inductor peak current is much higher, effectively lowering the recommended operating maximum output current range. Additional level-shifting circuitry is required to invert the negative output signal if EN and PGOOD feature utilization is required.

## 7 References

The following documents are available for download::


- Texas Instruments, *Basic Calculation of an Inverting Buck-Boost Power Stage Application Report*
- Texas Instruments, *Creating an Inverting Power Supply Using a Synchronous Step-Down Regulator Application Report*
- Texas Instruments, *Using a buck converter in an inverting buck-boost topology Technical Brief*
- Texas Instruments, *Working With Inverting Buck-Boost Converters Application Report*




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