

Application Report

ATL43xLI-Q1 Functional Safety FIT Rate, FMD and Pin FMA



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1 Overview

This document contains information for ATL43xLI-Q1 (DBZ package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.

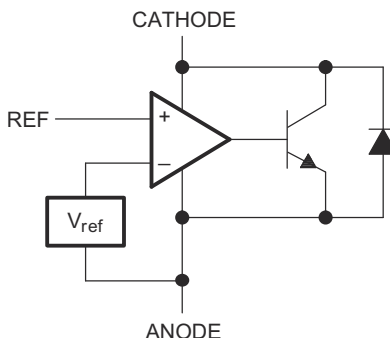


Figure 1-1. Equivalent Schematic

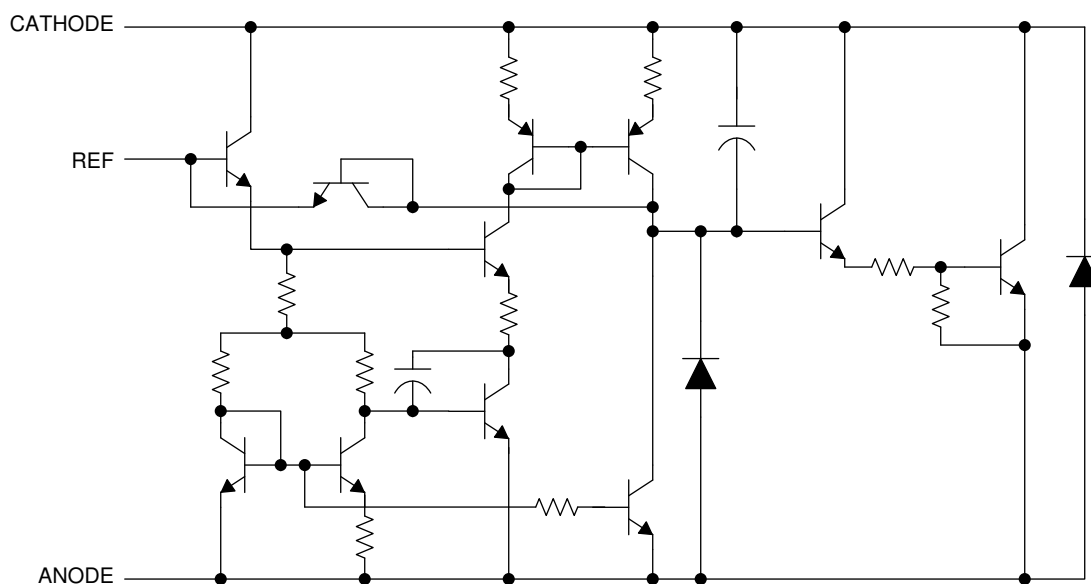


Figure 1-2. Detailed Schematic

ATL43xLI-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DBZ Package

This section provides Functional Safety Failure In Time (FIT) rates for DBZ package of ATL43xLI-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	6
Die FIT Rate	4
Package FIT Rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
4	Simple Analog / HF	3 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ATL43xLI-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Cathode or Anode open (HIZ)	25%
Cathode or Anode short	35%
Cathode not in specification voltage or current	40%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ATL43xLI-Q1 (DBZ package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VCC (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Assumptions of use and the device configuration assumed for the pin FMA are described by :

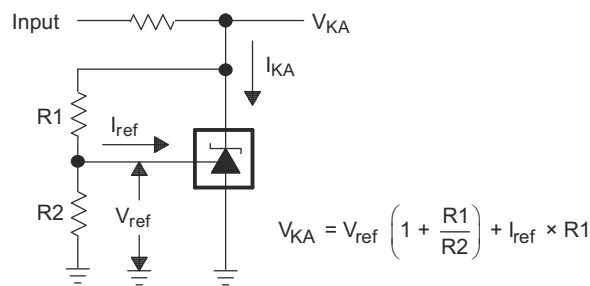


Figure 4-1. Test Circuit for $V_{KA} > V_{ref}$

4.1 DBZ Package

[Figure 4-2](#) shows the ATL43xLI-Q1 pin diagram for the DBZ package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ATL43xLI-Q1 data sheet.

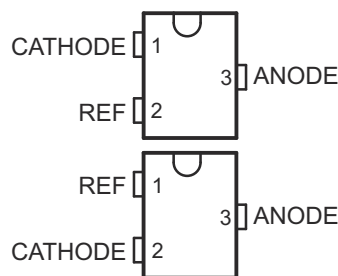


Figure 4-2. Pin Diagram for DBZ Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CATHODE	1 or 2	No power; No Cathode voltage regulation.	C
REF	1 or 2	Cathode voltage is unregulated.	C
ANODE	3	No effect.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CATHODE	1 or 2	No Output Voltage.	C
REF	1 or 2	Output is not regulated.	C
ANODE	3	Output voltage is not regulated.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CATHODE	1 or 2	REF	Voltage might be regulated differently depending on the gain of the device.	C
REF	1 or 2	ANODE	Cathode voltage is unregulated.	C
ANODE	3	CATHODE	No damage to device, can affect application functionality. Increases leakage.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC (For error amplifier, this is the cathode)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CATHODE	1 or 2	No Effect.	D
REF	1 or 2	Voltage might be regulated differently depending on the gain of the device.	C
ANODE	3	No damage to device, can affect application functionality. Increases leakage.	C

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Initial Release

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