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ABSTRACT

Current sharing between two identical buck regulators is not as simple as connecting the input and output voltage rails together. Without an external current sharing circuit there is no way to ensure that each regulator is equally loaded. Additionally, the current imbalance will cause the path that sources more current to run thermally hotter than expected and potentially trip thermal shutdown if the junction temperature of the IC is above the thermal junction shutdown threshold.

To achieve a current sharing design, a dual phase solution can be implemented by connecting two buck regulators in parallel. In this configuration, each buck regulator equally shares current to enable a design that requires output currents greater than the maximum rated current capability of each individual buck regulator. This application report details the design, implementation and preliminary lab results of two LM62460 buck regulators configured for a dual phase solution.

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1 Introduction

Every buck regulator will have a specified maximum output current rating capability that the device can handle before an over-current condition is triggered. In this over-current condition the device will shut-down, stop switching, and check if the fault is removed before switching is resumed. Normally if a design calls for a higher output current requirement above the device's maximum rated output current limit, a new device must be selected. However this would require a new schematic and PCB layout design if the device is not pin-to-pin compatible with the original layout.

With a simple external differential op-amp circuit two single-output buck regulators can be configured in a two-phase design to allow twice the load current capability of a single buck regulator. This provides customers the following benefits:

1. Tying two regulator outputs together to share current allows the spread of power loss between two regulators leading to lower tempt rise and overall thermally robust design. This removes the potential need for designing with an external heatsink which increases system design complexity, size, and overall cost.
2. Implementing 180 degrees phase shift circuit provides the following benefits:
 - a. Each path will have less switching losses. Doing this creates a design that leads to better EMI and thermal performance.
 - b. Phase shift circuits provide input and output ripple current cancellation. For more details refer to [Section 8.1.2 from the LM5119-Q1 data sheet](#).
3. Easier to design than a dual phase controller since power MOSFETS are already integrated into the regulator/converter.

2 Different Types of Current Sensing

Two Types of Current Sensing

Two commonly used methods for sensing current in the power stage of a buck converter are the use of current sense resistors and inductor DCR current sensing. The benefit of using the current sense resistor method is superior accuracy over the entire operating conditions (for example, variations in inductor DCR and inductance values between the two channels) and better matched current sharing between the two phases, while sacrificing power loss. On the other hand, DCR current sensing sacrifices accuracy while being more efficient, since there is typically negligible power loss associated with this method of sensing. The application requirements will dictate which current sensing method will be implemented.

Inductor DCR Current Sensing

When using the inductor DCR current sensing method, a carefully selected RC network is used to mimic or recreate the voltage that would be seen across the DCR of the inductor. It is as if the DCR of the inductor is the current sense resistor. In order to accurately represent the current flowing through the DCR, the RC time constant (τ), needs to be the same as that of the inductor and DCR

$$\tau = \frac{L}{DCR} = RC \quad (1)$$

- L = power inductor
- DCR = inductor direct-current-resistance

One of the ways to find the values for the RC components is by first calculating an approximate resistor value for R ($R_{temporary}$), from which we will find the capacitor value. Once an actual capacitor is selected (i.e from a component vendor), we can then re-calculate a more accurate resistor value. The reason for performing this slightly iterative process is due to the fact that it is usually more difficult to find a capacitor with the desired value, temperature coefficient, voltage rating, and availability, compared to the resistor.

1. Calculate a temporary resistor value: A good-sized resistor for most applications is either an 0402 or 0603 (Imperial) package size resistor. For most applications 0402 resistors will work fine. The characteristics of these (0402) resistors vary between manufacturers and product-series, however they *usually* have voltage ratings of about 50V and power ratings of about 1/16W, or 0.063W. Worst-case power dissipation estimation, along with buffers, let us say is 50mW for this 0402-package resistor

$$P_{dissipation_R} = \frac{(V_{in_Max})^2}{(R_{temporary})} \Rightarrow R_{temporary} = \frac{(V_{in_Max})^2}{(P_{dissipation_R})} \quad (2)$$

2. Calculate a capacitor value:

$$\tau = (R_{temporary})(C) \Rightarrow C = \frac{\tau}{R_{temporary}} \quad (3)$$

3. Find an actual capacitor that is closest to that calculated in Step 2
4. Calculate the actual resistor value to be selected/used:

$$\tau = (R_{actual})(C) \Rightarrow R_{actual} = \frac{\tau}{C} \quad (4)$$

Current Sense Resistor for Current Sensing

As a rule-of-thumb a good full-scale current sense voltage range (V_{Isns}) is approximately between 75mV and 100mV at the maximum peak inductor current.

$$\frac{V_{Isns}}{I_{Lpk_Max}} = R_{sns} \tag{5}$$

The power loss through the current sense resistor involves the maximum continuous load current, which for a buck converter is the average inductor current at this condition.

$$(I_{avgMax}^2)(R_{sns}) = P_{lossR_{sns}} \text{ (typically aim for } \leq 1W \text{ of power loss)} \tag{6}$$

For example, in the case of PMP22993, the maximum *peak* load current (per phase) is 6A, giving us a peak inductor current of 7AIL_pk. Figure 2-1 is a GUI from the Power Stage Designer Tool to help illustrate and simulate the expected inductor current given a typical design value ($V_{IN} = 16V$, $V_{OUT} = 3.3V$, $I_{OUT} = 6A$, $F_{sw} = 2.1MHz$).

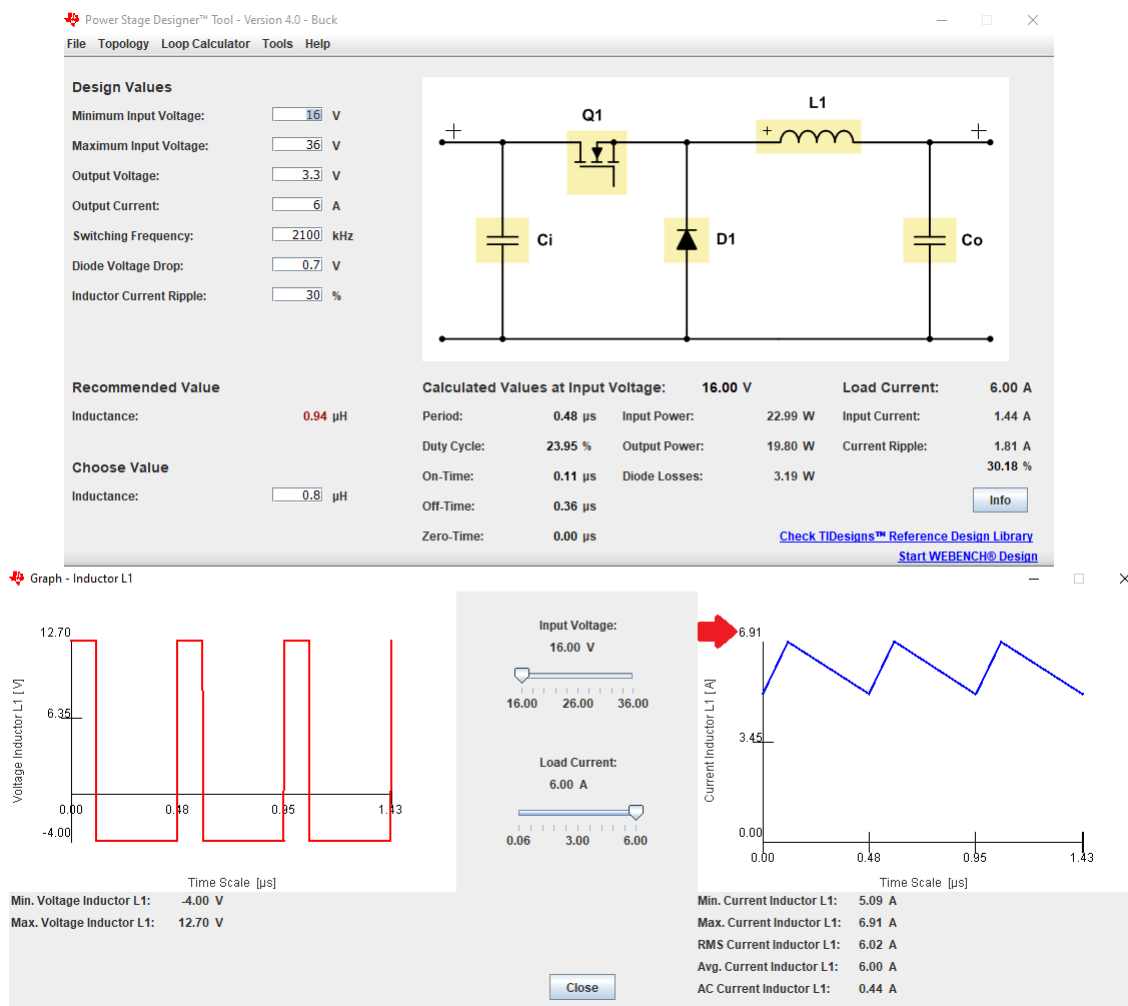


Figure 2-1. Inductor Current Simulation from Power State Designer Tool

If we were to use 100mV as the full-scale current sense voltage we get,

$$\frac{100mV}{7A_{IL_pk}} = 14.3m\Omega \Rightarrow \approx 15m\Omega \quad (7)$$

Now let us see how much power will be dissipated in this resistor when operating at the maximum continuous load current:

$$(4.5A^2)(15m\Omega) = 0.3W \quad (8)$$

Let us check how much this amount of power loss will decrease our total system efficiency:

$$\left(\frac{P_{loss_Rsns}}{P_{Out_total}} \right) (100) = \% \text{ loss relative to } P_{out}, \text{ due to } R_{sns} \quad (9)$$

$$\frac{(0.3W)}{(3.3V)(4.5A)} = 2\% \quad (10)$$

For this application, a loss of 2% of efficiency at maximum continuous load is deemed acceptable. Designing for a reduced system efficiency of 3% or lower is generally acceptable but will depend on the application requirements. As a rule-of-thumb, it is always good to select a current sense resistor that has a power dissipation rating that is twice that of the calculated power loss. This is so that the resistor temperature does not get too high.

To assist in calculating, as well as visualizing, many of the signals associated with switch-mode power supplies, such as the peak inductor current, please download Power Stage Designer ([link](#)).

3 Basic Current Sharing Operation

Current sharing between two buck regulators can be achieved using a simple current sharing op-amp circuit using a [OPA991](#). This current sharing amplifier design is configured as a differential amplifier which compares the primary and secondary phase inductor currents. The op amp circuit servos the secondary converter's load current, by controlling the output voltage, to keep the difference between the primary and secondary output currents zero. For example, if the primary phase were to source more current than the secondary phase, the output of the differential amplifier will decrease causing the secondary phase voltage to slightly increase. This results in the secondary phase sourcing more current until it achieves balanced current sharing.

R_2 and R_F should be calculated such that, when the primary and secondary output voltage is matched, the output of the difference amplifier is equal to the reference voltage (V_{ref}) of the buck regulator (Refer to schematic in [Figure 3-1](#) for more details). When both phases are evenly matched no current will be sourced or sunk from the feedback node. Note that the op-amp current sense design requires a compensation capacitor that is placed in parallel to R_F . This capacitor value may need to be adjusted per application parameters.

$$V_{C_SECONDARY} = R_{SENSE} * I_{OUT} + V_{OUT} \quad (11)$$

- $V_{C_SECONDARY}$ is the voltage before the current sense resistor of the secondary converter

$$V_P = V_{C_SECONDARY} * \frac{R_g}{R_g + R_1} \quad (12)$$

$$V_N = V_P \quad (13)$$

- Note: This equation assumes the ideal op-amp voltage on both inverting and non-inverting inputs

$$I_{RF} = \frac{V_{C_MAIN} - V_N}{R_2} \quad (14)$$

- V_{C_MAIN} is the voltage before the current sense resistor of the main converter

$$V_{DROP} = V_N - V_{REF} \quad (15)$$

- V_{REF} is the internal reference voltage of the converter

$$R_F = \frac{V_{DROP}}{I_{RF}} \quad (16)$$

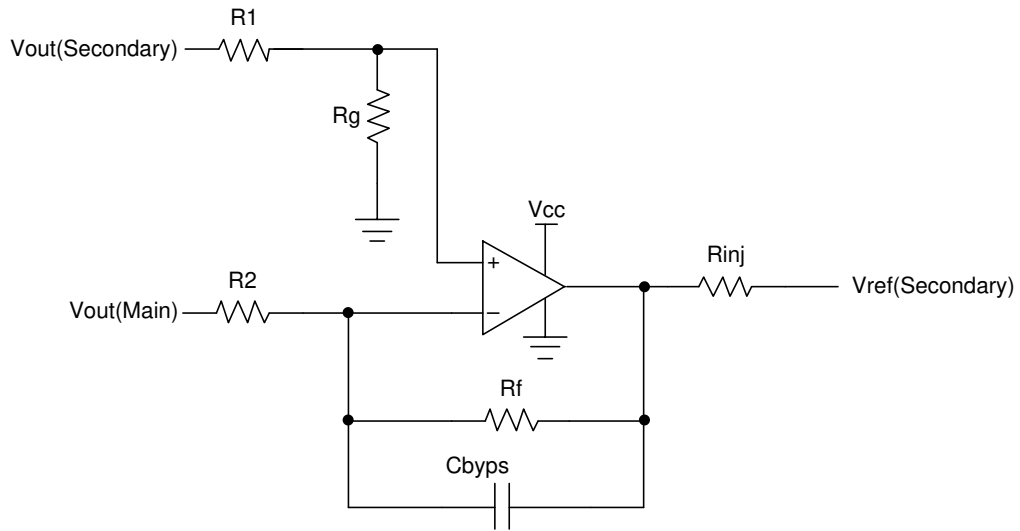


Figure 3-1. Current Sharing Differential Op-Amp Circuit Design

4 Schematic and BOM

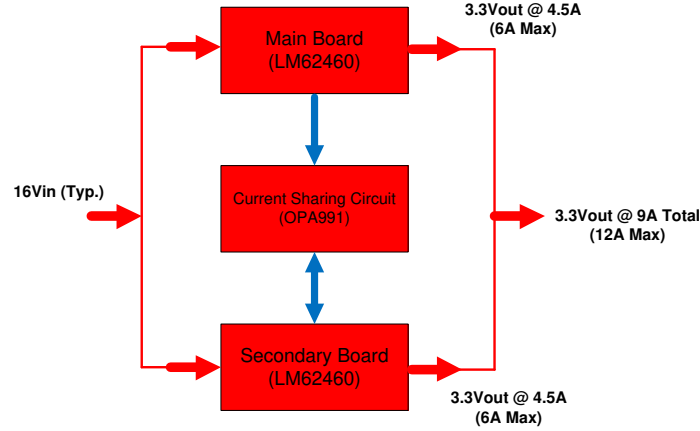


Figure 4-1. System Level Block Diagram

Test Condition:

- VIN = 16 V
- VOUT = 3.3 V
- IOUT = 9A Continuous | 12 A Peak (4.5 A continuous per phase)

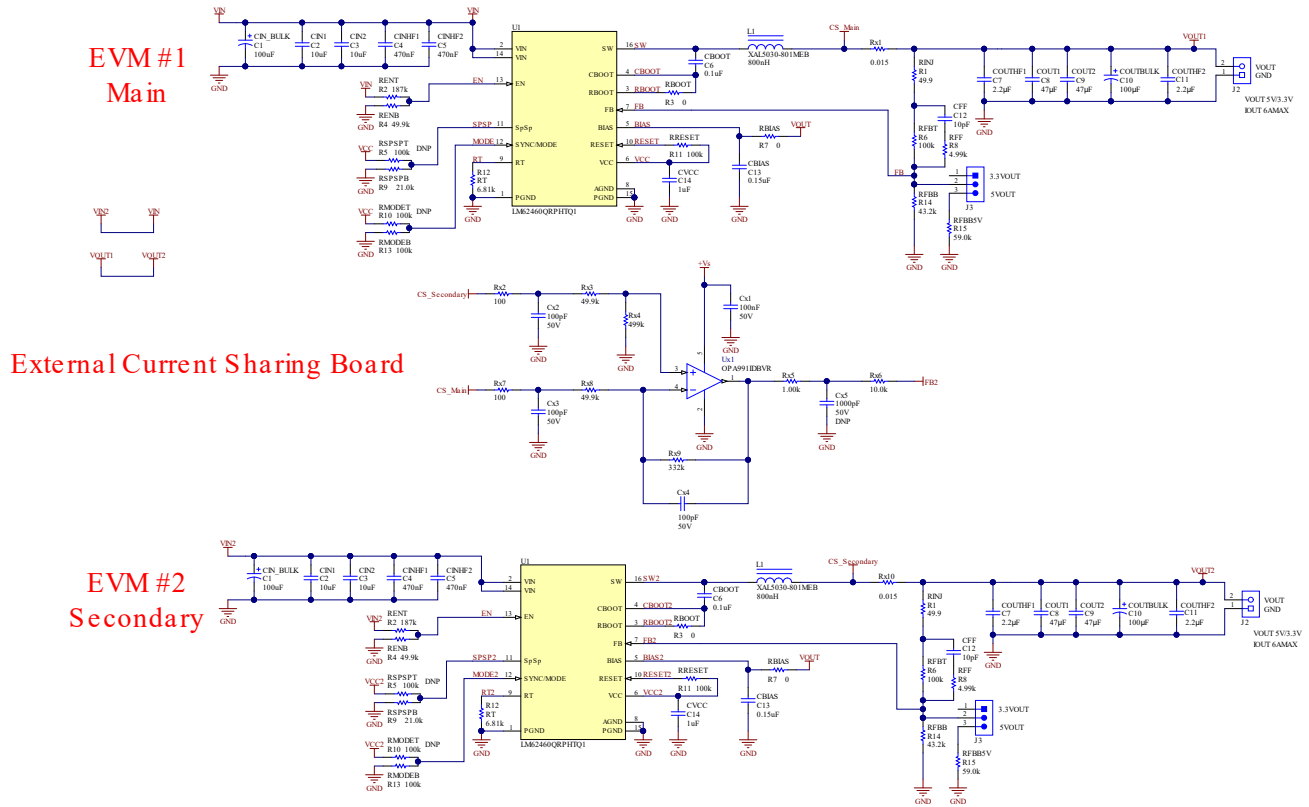


Figure 4-2. Dual Phase Application Full Schematic

Notes:

1. The EN pins of both channels are connected to each other.
2. The positive supply rail, +Vs, of the op-amp was connected to the Vout for these tests. However it is recommended to connect to an external auxiliary supply rail that is operational before these converters are started up.
3. This is a preliminary design and the component values and circuit schematic might need adjustments.
4. Two separate EVMs were used and wired together, along with a breakout board for the op-amp circuit, for this design.

Table 4-1. LM62460RPHEVM 6-A 2.1-MHz EVM Bill of Materials

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C1	CAP, AL, 100 uF, 63 V, +/- 20%, 0.35 ohm, AEC-Q200 Grade 2, SMD	Panasonic	EEE-FK1J101P	2
C2, C3	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1210	TDK	C3225X5R1H106K250AB	4
C4, C5	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H474K080AB	4
C6	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	TDK	CGA2B3X7R1H104K050BB	2
C7, C11	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GRM188R71A225KE15J	4
C8, C9	CAP, AL, 100 uF, 16 V, ±20%, AEC-Q200 Grade 3, SMD	MuRata	GCM32EC71A476KE02K	4
C10	CAP, AL, 100 uF, 16 V, +/- 20%, AEC-Q200 Grade 3, SMD	Panasonic	EEE-1CA101AP	2
C12	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	TDK	CGA3E2C0G1H100D080AA	2
C13	CAP, CERM, 0.15 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H154K080AB	2
C14	CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71C105MA64D	2
Cx1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71H104KA01L	1
Cx2, Cx3, Cx4	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0805	Kemet	C0805C101J5GACTU	3
L1	Inductor, Shielded, Composite, 800 nH, 13 A, 0.01 ohm, AEC-Q200 Grade 1, SMD	Coilcraft	XAL5030-801MEB	2
R1	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349R9FKEA	2
R2	RES, 187 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-07187KL	2
R3	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	2
R4	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349K9FKEA	2
R6, R11, R13	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	6
R7	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Stackpole Electronics Inc	RMCF0603ZTOR00	2
R8	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034K99FKEA	2
R9	RES, 21.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060321K0FKEA	2
R12	RES, 6.81 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06036K81FKEA	2
R14	RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060343K2FKEA	2
R15	RES, 59.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060359K0FKEA	2
Rx2, Rx7	RES, 100, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW1206100RFKEA	2
Rx3, Rx8	RES, 49.9 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW120649K9FKEA	2
Rx4	RES, 499 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW1206499KFKEA	1
Rx5	RES, 1.00 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW12061K00FKEA	1
Rx6	RES, 10.0 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW120610K0FKEA	1
Rx9	RES, 332 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW1206332KFKEA	1
U1	LM62460QRPHTQ1, RPH0016A (VQFN-HR-16)	Texas Instruments	LM62460QRPHTQ1	2
Ux1	OPA991IDBVR operational amplifier	Texas Instruments	OPA991IDBVR	1
Cx5	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 1206	MuRata	GRM3195C1H102JA01D	0
R5, R10	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	0

5 Lab Measurements

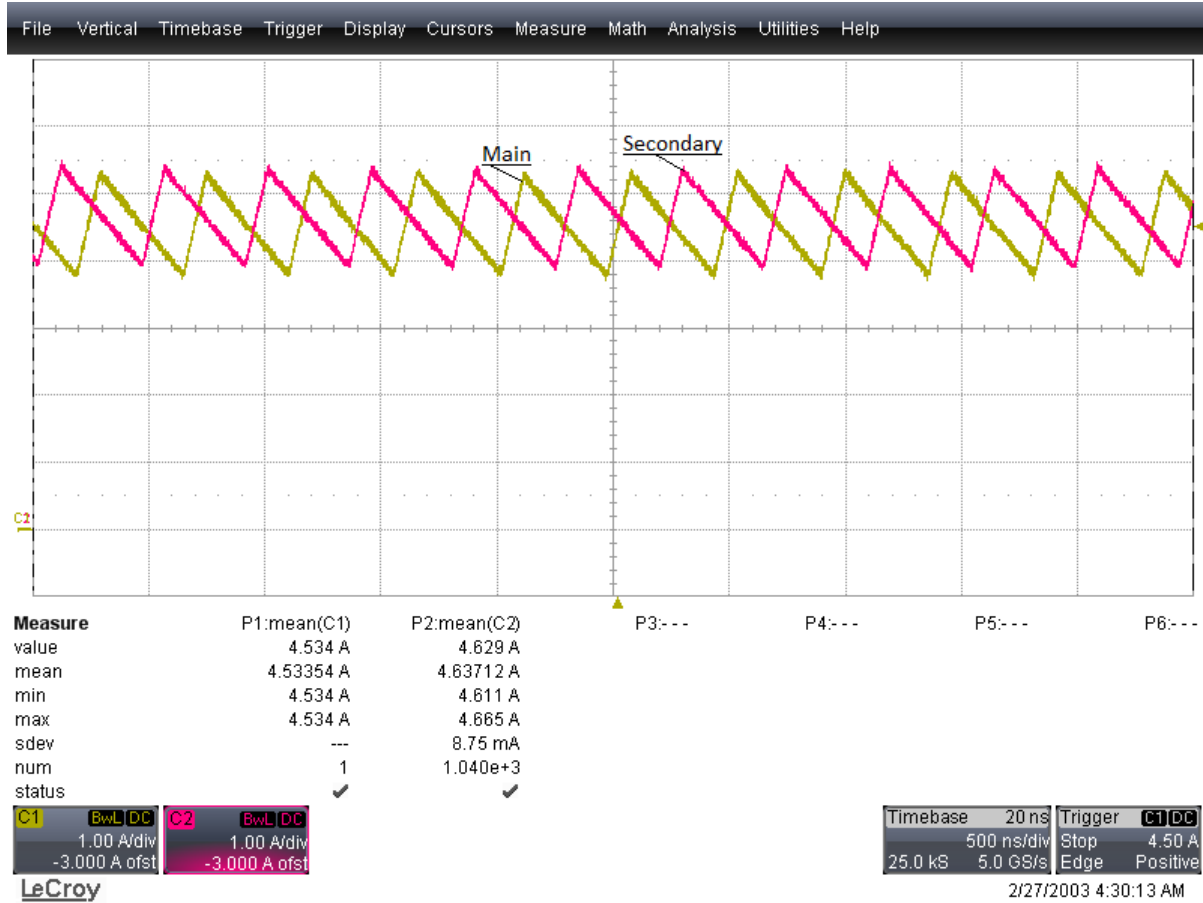


Figure 5-1. Inductor Current Sharing Steady-State Waveform

- $I_{OUT_Main} = 4.53 \text{ A}$
- $I_{OUT_Secondary} = 4.64 \text{ A}$
- $I_{OUT_Average} = 4.58 \text{ A}$
- Current sharing accuracy = $4.58 \pm 1.13\%$

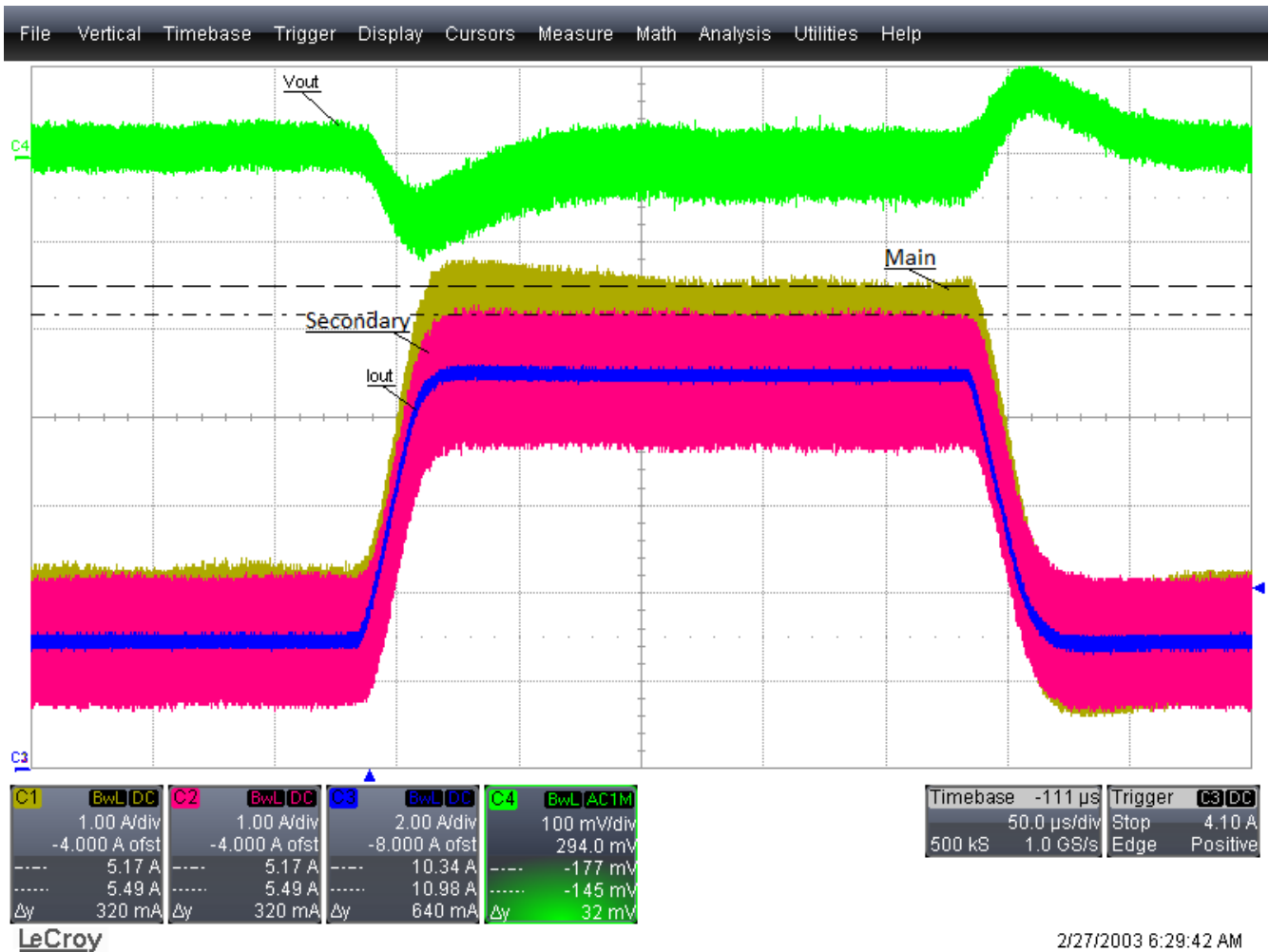


Figure 5-2. Inductor Current Sharing Load Transient (3 A to 9 A) Waveform

- $I_{OUT_Main} = 4.79A$
- $I_{OUT_Secondary} = 4.47A$
- $I_{OUT_Average} = 4.63A$
- Current sharing accuracy = 4.63 +/- 3.45%

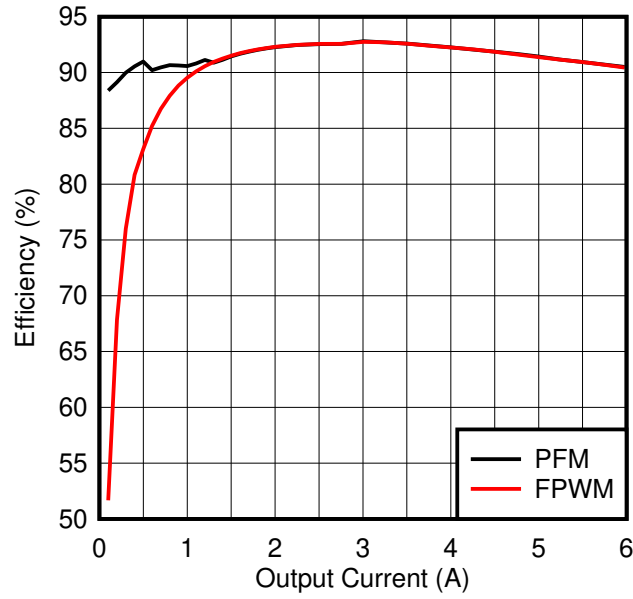


Figure 5-3. Efficiency at 400 kHz (VIN = 16 V; VOUT = 3.3 V)

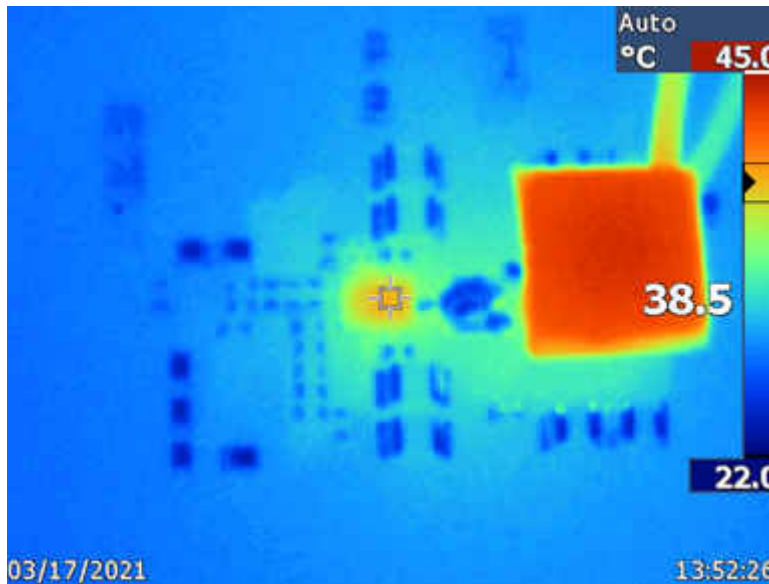


Figure 5-4. Thermal Measurement at 400 kHz (VIN = 16 V; VOUT = 3.3 V; IOUT = 4.5 A)

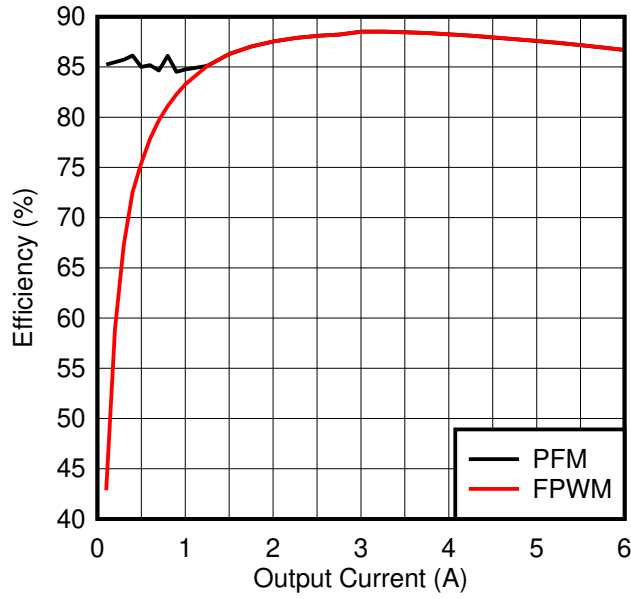


Figure 5-5. Efficiency at 2.2 MHz (VIN = 16 V; VOUT = 3.3 V)

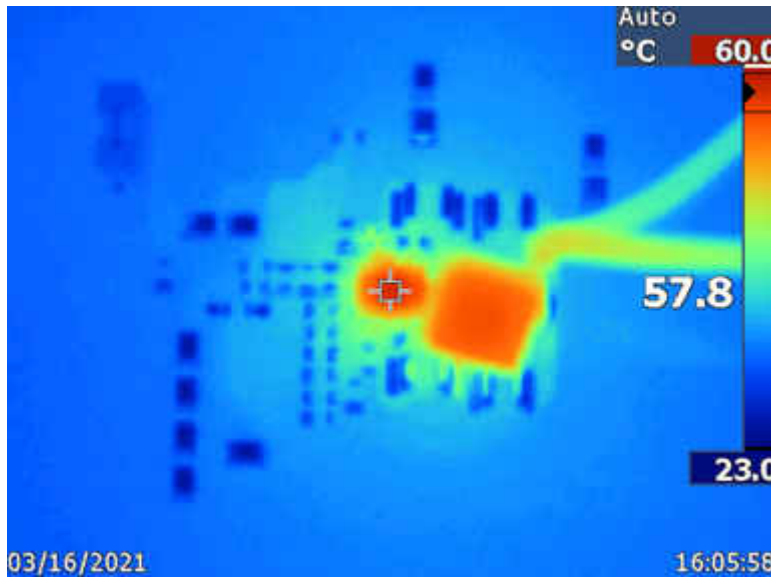


Figure 5-6. Thermal Measurement at 2.2 MHz (VIN = 16 V; VOUT = 3.3 V; IOUT = 4.5 A)

6 Caveats and Recommendations

Design Procedure

To design a dual-phase current shared solution, use the following steps:

1. Decide on the appropriate type of current sensing for the application
2. Calculate the component values to set a balanced current sharing op-amp circuit
3. Configure the circuits inputs following [Figure 4-2](#)
4. Follow layout guidelines as described in the [Proper Symmetric PCB Layout](#)

Proper Symmetric PCB Layout

When designing the LM62460 device it is recommended to follow layout guidelines outlined in [Section 11.1](#) of the data sheet. Additionally the two LM62460 devices should be positioned such that the input and output PCB trace of each phase should be as symmetrical as possible. This is to achieve a proper impedance matching between the outputs of each circuit to the point of load.

Phase Shifting Circuit for Two Phase Interleaving

Without an external phase shift circuit, the main board and secondary board will still share current, but the phase of the switching between the two will not be 180° out of phase. To provide a low noise system an external phase shift circuit is advised. This can be implemented by providing an external synchronizing clock signal connected to the SYNC input main regulator. This external clock signal then needs to be phase shifted 180° through an inverter ([HC04D](#)) and connected to the SYNC input of the secondary regulator.

7 Summary

The method and design procedures described in this application note simplify the process for designing a dual-phase current-sharing solution with the LM62460 device. A current sharing solution with two buck converters will result improved EMI performance, lower temperature rise, and reduced RMS currents in the input and output capacitors. By following the step-by-step instructions detailed in this application note, a designer can easily create a dual-phase current-sharing solution from any buck converter.

8 References

The following links give details on dual phase application

1. Texas Instruments, [How to design a simple two-phase current-sharing synchronous buck regulator](#) article.
2. Texas Instruments, [6A Current-Sharing Dual LDO](#) design guide.
3. Texas Instruments, [How to parallel two DC/DC converters with digital controllers](#) Analog Design Journal.
4. Texas Instruments, [TI Precision Labs – Op amps](#) article.
5. Texas Instruments, [LM62460-Q1 Automotive Buck Converter](#) data sheet.
6. Texas Instruments, [LM5119 Wide Input Range Dual Synchronous Buck Controller](#) data sheet.

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