

IEEE 802.3cg 10BASE-T1L Power over Data Lines Powered Device Design



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ABSTRACT

The IEEE 802.3cg 10BASE-T1L specification has simultaneously solved many problems of industrial communication by allowing 10-Mbps full-duplex communications up to a distance of 1,000 meters through a single pair of twisted wires, which can already be taken advantage of with the DP83TD510E single-pair Ethernet PHY. Furthermore, the standard also includes Power over Data Lines (PoDL) as the single-pair alternative to Power over Ethernet (PoE). This allows designers in the factory and building automation markets to use familiar Ethernet based protocols for long-distance communication between industrial controllers and sensors, with TCP/IP protocols from the Ethernet protocol suite being the basis for OPC UA, MQTT and HTTP. PoDL allows for this while also reducing wiring, as well as converging and simplifying their existing 4 mA to 20 mA or field-bus communication networks. A 10BASE-T1L PoDL system is composed of a Power Sourcing Equipment (PSE), a link segment and a Powered Device (PD). This document provides an overview of such a system and describes in detail how to design a 10BASE-T1L class-12 compliant PoDL PD.

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1 Introduction

1.1 10BASE-T1L (IEEE 802.3cg) PoDL Overview

The IEEE Std 802.3cg-2019 Ethernet physical layer standard was released by the IEEE on November 7, 2019. The standard brings a new standardized option for long-distance communication over only a single balanced twisted conductor pair up to 1000 m in length. The standard allows engineers to use their existing hardware and software knowledge of Ethernet networks to bring the existing complex communication infrastructure under the familiar Ethernet family of networking technologies. The new approach also allows for seamless connectivity of actuators, sensors, and other equipment, thereby improving operational efficiency especially in the building and factory automation markets. This converges potentially fragmented networks.

The 10BASE-T1L Ethernet variant in the IEEE 802.3cg standard defines a 10 Mbps, full duplex, point-to-point communication scheme. The DP83TD510E Ethernet PHY fully supports this new standard and goes beyond the specification by supporting lengths up to 2000 meters, providing design flexibility and maximizing cable reach over a single balanced pair of conductors.

The IEEE 802.3cg standard extends the PoDL section of the IEEE 802.3bu standard adding support for longer distance cable reach and additional power classes. The replacement of 4 mA to 20 mA or field bus communications in many cases reduces design complexity, eliminates power hungry gateways, and increases the available power to connected equipment. This is in addition to significant faster data rate compared to 4-20 mA current loops, as well as the addition of a back channel. Also in comparison to other protocols, HART allows a back channel, but is relatively slow (1200 bps). IO-Link is faster than HART (up to 230 kbps), but is limited to 20 m.

Figure 1-1 illustrates a high-level diagram of PoDL. The implementation of PoDL requires the design of a compliant Power Sourcing Equipment (PSE), a Powered Device (PD) as well as the link segment between the two. The PSE supplies power to the link and the PD draws power from that link.

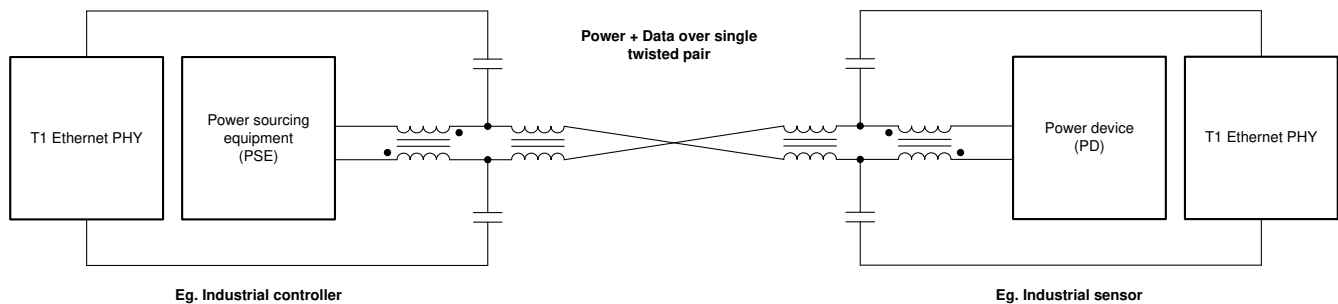


Figure 1-1. Power Over Data Lines (PoDL) High-Level Diagram

1.2 PoDL PSE Types and Power Classes

Consider the IEEE 802.3cg standard as the 10BASE-T1S/10BASE-T1L and PoDL amendment to the IEEE 802.3bu standard which applies to 100BASE-T1 and 1000BASE-T1. The IEEE 802.3bu standard defined 4 types of PSEs Type A, Type B, Type C, and Type D. The standard also defines 10 different power classes for PDs and PSEs including 12-V, 24-V and 48-V unregulated and regulated PSE classes. The IEEE 802.3cg standard extended this by introducing type E and adding 30 V and 58 V classes bringing the total to 15 different compliant classes. [Table 1-1](#) and [Table 1-2](#) detail the complete type and class power matrices.

Table 1-1. PoDL PSE Type Matrix

Type	A	B	C	D	E
10BASE-T1S	X		X		
10BASE-T1L					X
100BASE-T1			X		
1000BASE-T1		X	X		
No data or incompatible				X	

Table 1-2. PoDL Class Power Requirements Matrix

Class	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
VPSE(max) (V)	18	18	18	18	36	36	36	36	60	60	30	30	30	58	58	58
VPSE_OC(min) (V)	6	14.4	14.4	12	12	26	26	48	48	48	30	20	20	50	50	50
VPSE(min) (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48	20	20	20	50	50	50
IPI(max) (mA)	101	227	249	471	97	339	215	461	735	1360	92	249	632	231	600	1579
Pclass(min) (W)	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3	1.85	4.8	12.63	11.54	30	79
VPD(min) (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7	14	14	14	35	35	35
PPD(max) (W)	0.5	1	3	5	1	3	5	10	30	50	1.23	3.2	8.4	7.7	20	52

Note

The standard specifies mandatory detection protocol for each type and power class without if SCCP communication is not implemented between the PSE and PD.

This document focuses on the design considerations of a class 12 10BASE-T1L compliant PD.

2 Terminology

10Base-T1L	10 Mbps full-duplex communication over single balanced pair of conductors standard
CDN	Coupling, decoupling network
CMC	Common-mode choke
DMI	Differential mode inductor
IEEE	Institute of Electrical and Electronics Engineers
OVP	Overvoltage protection
PD	Powered Device
PHY	Physical layer transceiver
PoDL	Power over Data Line
PSE	Power Sourcing Equipment
SCCP	Serial Communication Classification Protocol
SPE	Single-Pair Ethernet
UVLO	Undervoltage lockout

3 PD Design

3.1 PD Design Overview

It is important to understand the functions of both the PD and PSE before designing the PoDL system. The PSE has 4 main functions according to the IEEE standards. From the IEEE 802.3bu standard, the main functions of the PSE include:

1. To search the link segment for a PD
2. To supply power to a detected PD through the link segment
3. To monitor the power applied to a link segment
4. To remove the full operating voltage when no longer required, or when a short-circuit or other fault is detected

Conversely, the PD, is simply the portion of a device that draws power from the link or the portion that participates in the detection or classification algorithms. The PD system presented in this document includes:

1. The coupling and decoupling network (CDN) which decouples power from the power and data path
2. The VID block required for the PD to be detected as PoDL-compliant to a PSE
3. SCCP communication necessary for the optional classification function for power class negotiation
4. Power protection and regulated and isolated 24-V class-12 power supply to the device being powered

Figure 3-1 shows these system blocks.

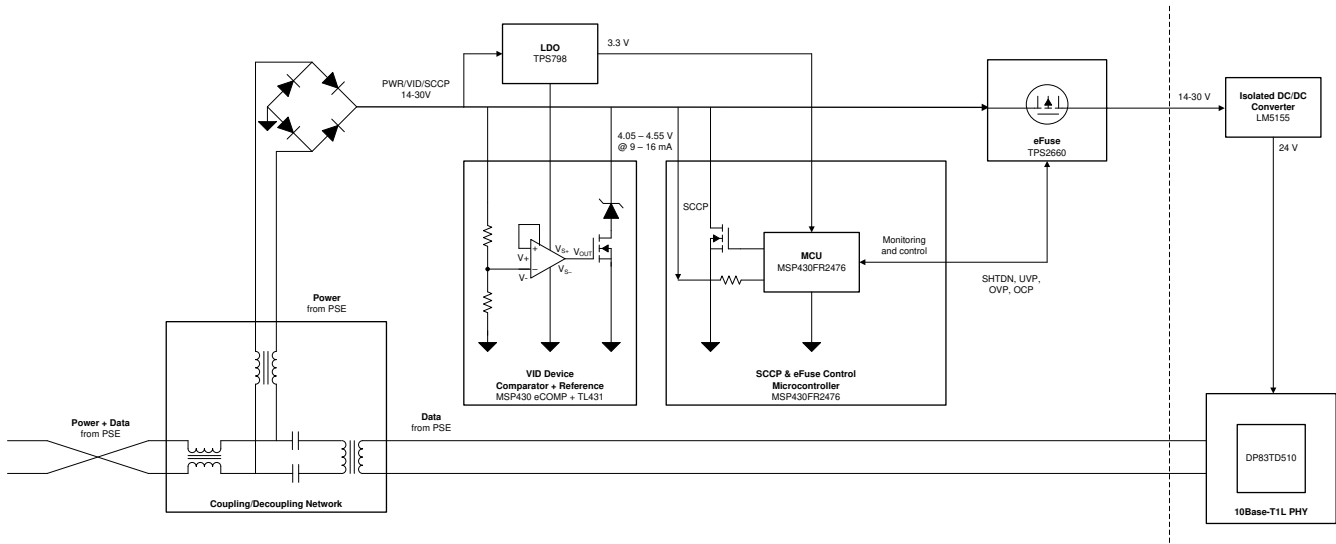


Figure 3-1. PoDL PD System Block Diagram

3.2 Coupling and Decoupling Network (CDN)

The PD must decouple power from the power and data path on the SPE link in a safe manner while allowing the data to pass through to the 10BASE-T1L PHY transparently and with no impact on the signal integrity. In addition, the IEEE 802.3cg standard specifies that the PD may receive power in two modes with power input pins swapped.

Table 3-1 details the PD pinout.

Table 3-1. PD Pinout

Contact	Mode A	Mode B
1	PI+	PI-
2	PI-	PI+

To protect the PD and implement it a manner insensitive to the polarity of the power supply, the PD includes a rectifier bridge. The Schottky diodes were carefully chosen to give a low-voltage drop across the rectifier.

The mode of operation of the CDN is as follows: Power and data come in on a SPE cable. Following the protection circuit (diodes D5 through D9), a common-mode choke (CMC) L2 suppresses common-mode noise and capacitors C2 and C3 provide the necessary damping. The common-mode noise must be filtered out without affecting the integrity of the differential signal. For this, a CMC with large common-mode impedance and small differential mode impedance in the 10-kHz range was selected.

The transformer L3 then provides isolation and the ESD diode is included for ESD protection. The choice of the transformer is dependent on the application, desired isolation rating as well as good performance in the appropriate frequency range. The inductance of the transformer has a direct impact on the droop.

From the CMC, a low DCR differential mode inductor (DMI) L1 allows DC current to pass to the rectifier (diodes D1 through D4). The rectifier ensures correct polarity to the PD regardless of cable orientation. The saturation current of the DMI must be sufficient for the desired power class (for class 12, this is at minimum 632 mA) and the DCR should be as low as possible to maximize efficiency and minimize the voltage drop, especially when designing for a 1-km cable reach. The inductance of the DMI has to be high enough to not cause too much damping of the data.

Figure 3-2 shows the PD coupling and decoupling network.

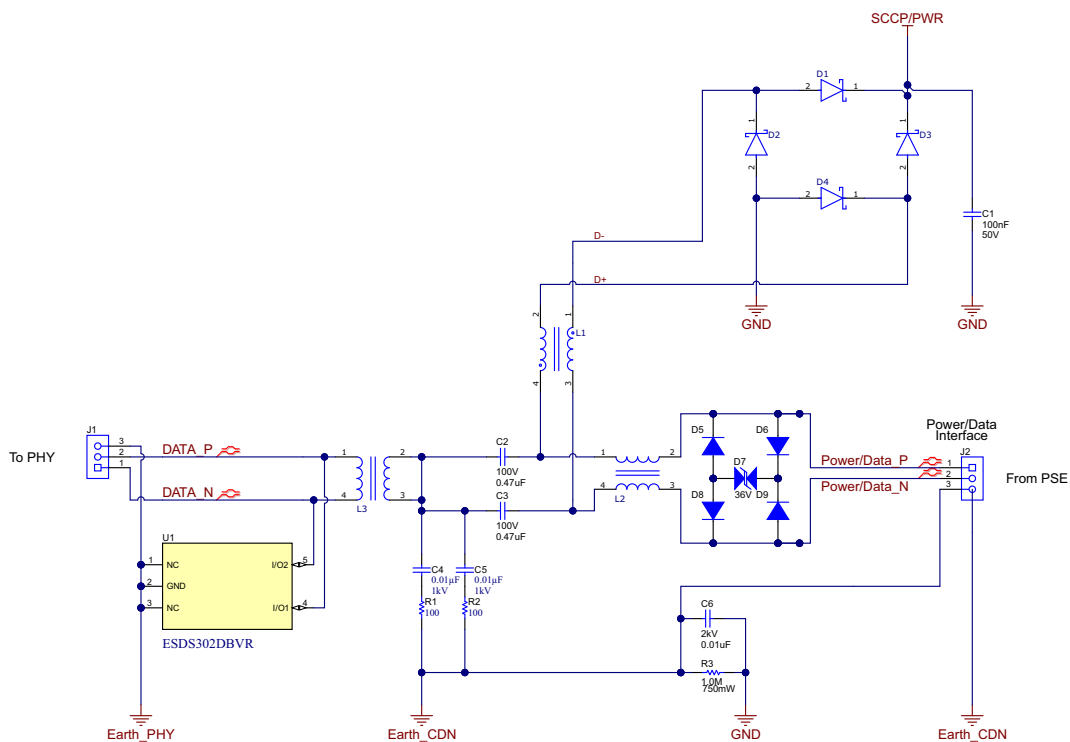


Figure 3-2. PD Coupling and Decoupling Network

Additional points of note are the termination between CDN ground and PD ground to minimize EMI (R3 and C6) as well as the common mode termination (C4, C5, R1, and R2).

3.3 VID Circuit

The voltage identification function is a mandatory feature of PD. Before the PSE applies full power to the link, it will test the link with a 9-mA to 16-mA constant current pulse and must detect a signature voltage from 4.05 V to 4.55 V. If the PSE detects a valid voltage signature, the PSE recognizes the device as PoDL compliant and can now supply full power to this link.

Table 3-2 details the PD detection parameters.

Table 3-2. PD Detection

Signature disable voltage (rising edge):	4.6 V to 5.75 V
Signature enable voltage (falling edge):	3.6 V to 4.3 V
Valid signature voltage	4.05 V to 4.55 V
Detection test current	9 mA to 16 mA

On the PD board, this voltage is generated using the eComp module integrated into the MSP430FR2476 microcontroller and a TL431 shunt reference. The shunt reference is configured to output approximately 4.2 V. The microcontroller is supplied from the 3.3-V rail and has an internal 1.2-V reference. The microcontroller checks the voltage on the connector, disconnects the shunt reference with the Q1 MOSFET when the input voltage rises above the signature disable threshold, and connects the TL431 reference U1 again when the input voltage falls below the signature enable threshold.

Figure 3-3 shows the PD VID circuit.

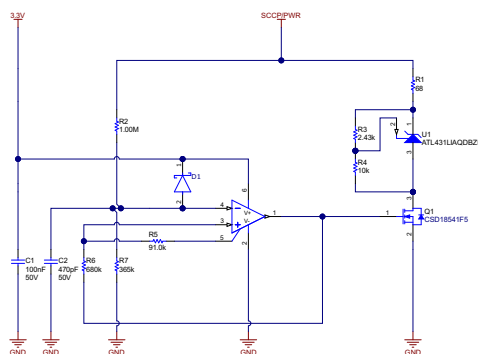


Figure 3-3. PD VID Circuit

Figure 3-4 shows the test results of the voltage signature circuit. The black line is seen to be within the 4.05-V and 4.55-V bounds when tested with a 9-mA to 16-mA signal. Note that the voltage drop across the rectifier bridge had to be taken into account in the calculation of resistors R1 through R7.

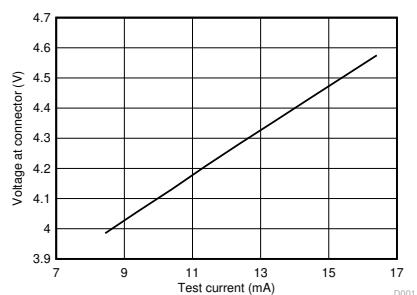


Figure 3-4. PD Signature Voltage Test Results

3.4 SCCP Communication

Serial Communication Classification Protocol (SCCP) is the bidirectional, single-wire serial communication protocol specified by the IEEE 802.3bu standard (and amended in IEEE 802.3cg) for negotiating power transfer requirements between the PSE and PD before the PSE applies power to the link. SCCP is current-sinking and wired-OR. During SCCP, the PSE acts as a controller, controlling the PD target device. The VID current source on the PSE is used as the pullup and the SCCP line is driven by pulling it low with discrete MOSFETs. The implementation of SCCP is optional if detection is implemented correctly on the PD and PSE. When classification is skipped in the system, this can be referred to as Fast Start-up Mode.

See the IEEE 802.3bu and 802.3cg standards for timing definitions. This document summarizes how to implement compliant SCCP communication on the PD. SCCP communication starts with a reset pulse from the PSE, which is followed by a presence pulse from the PD. In SCCP, every transaction starts with the falling

edge from the PSE, which can read “1” or “0” depending on the low logic time – so called “Write 1 time slot” and “Write 0 time slot”. For reading, the PD pulls the line low after a certain specified time. The PD can only transmit data to the PSE when the PSE issues read time slots. When the read time slot is started by the controller, the PD then transmits a “1” or “0” by leaving the line high or driving it low.

Due to the simplicity of the protocol and the relatively slow speed of 333 bps, one of the simplest SCCP implementations is by using only GPIO pins on the microcontroller and a clamping diode to limit the voltage at the pin when the line is high (24 V once the PSE applies power to the link).

Figure 3-5 shows the PD SCCP system blocks.

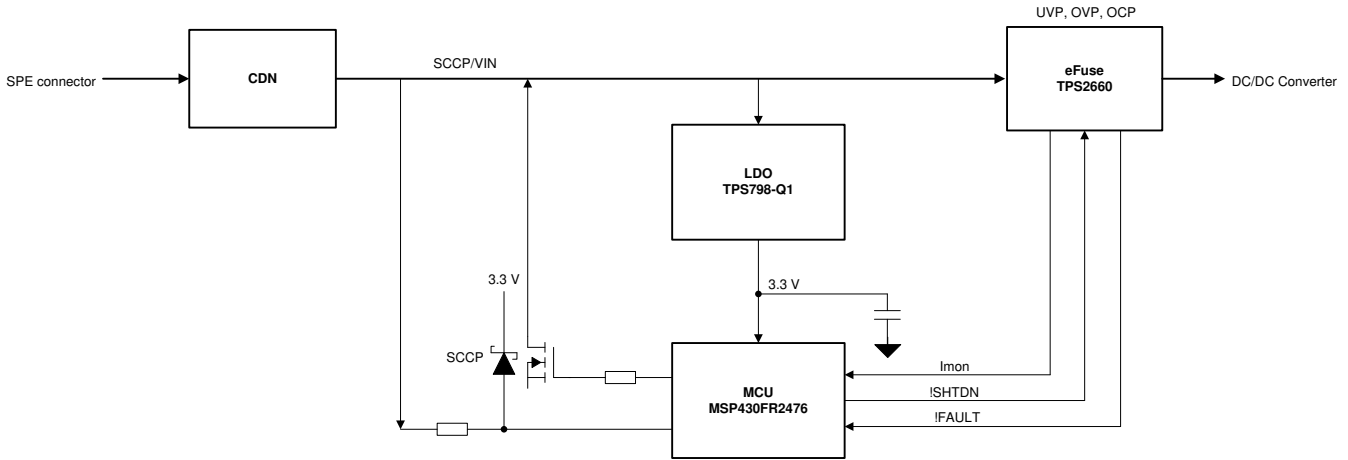


Figure 3-5. PD SCCP System Blocks

However, this approach can be improved by including a comparator as a buffer or driver on the data-in pin (U3 TLV7031). This ensures that the voltage rise and fall times are within specifications and the voltage into the GPIO pins does not exceed the supply voltage.

Figure 3-6 illustrates the PD simplified final SCCP circuit.

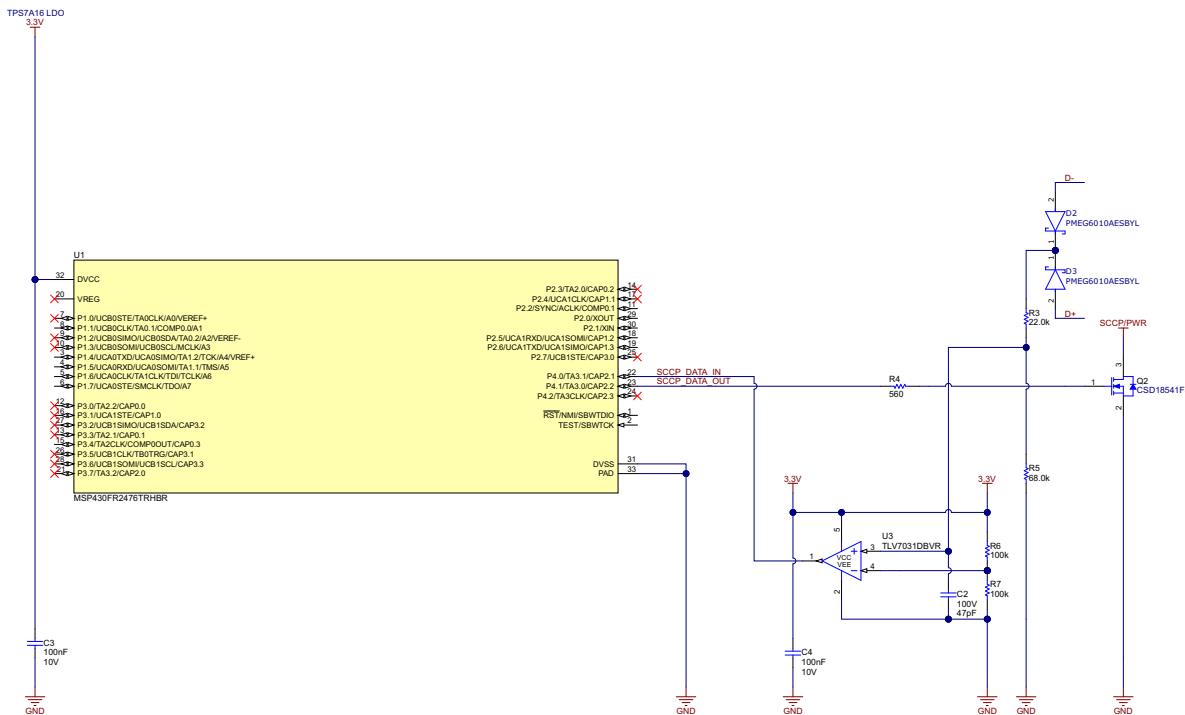


Figure 3-6. PD Simplified Final SCCP Circuit

It is important to note that during the reset pulse, the SCCP line gets pulled low for up to 11 ms. This line supplies the LDO, which in turn supplies the microcontroller in the PD with 3.3 V. As such, there must be enough energy stored in the output capacitor of the LDO to supply the MCU for the duration of the reset pulse. A 10- μ F capacitor was found to be reliable on the PD board.

It is also a concern that the current will flow from the output capacitor into the output pin of the LDO during the reset pulse and all communication. To protect against this, an LDO with reverse current blocking at the output can be used. This PD design takes advantage of the TPS798-Q1 automotive 50-mA LDO with reverse-current protection. An ideal diode controller such as the LM66100 can be used as an alternative when using an LDO without reverse-current protection.

Figure 3-7 shows the PD LDO circuit.

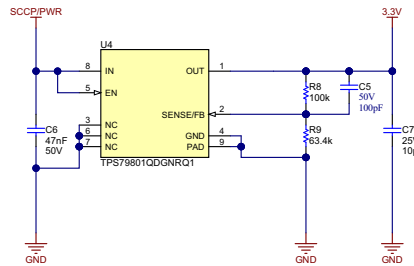


Figure 3-7. PD LDO Circuit

The oscilloscope screenshots in Figure 3-8 and Figure 3-9 show the start-up waveforms as seen on the PSE side. At first, the PSE supplies the PD with prebias voltage of 3.3 V so that the PD can operate in its low-power mode. The PSE tests the link with a detection current pulse and detects a valid voltage signature in the range of 4.05 V to 4.55 V. This is followed by a reset pulse initiated by the PSE, during which the PD microcontroller must remain functional, which then initiates SCCP communication.

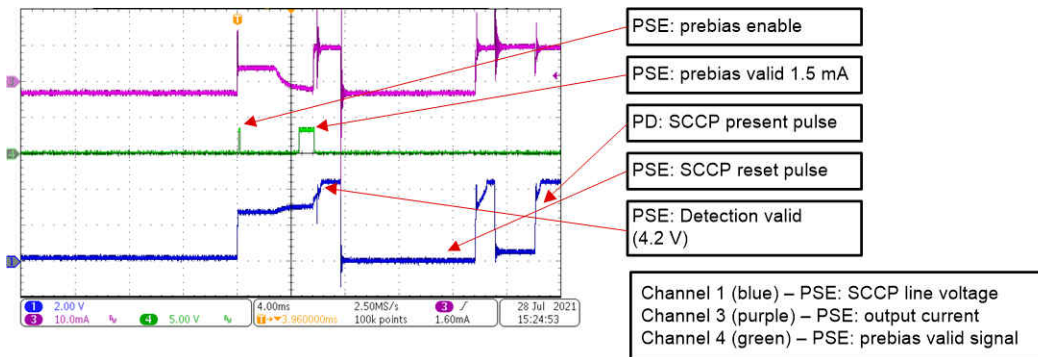


Figure 3-8. PSE Start-up Behavior

SCCP communication takes place as previously outlined, during which the PSE and PD negotiate the power class. Following SCCP communication, the PSE applies power to the link.

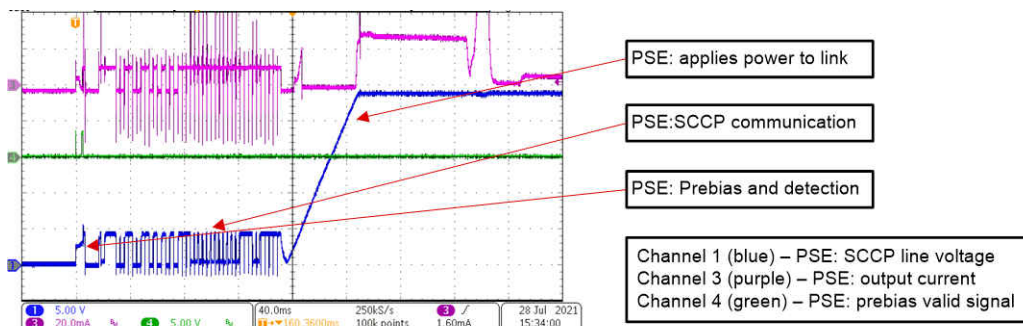


Figure 3-9. PSE Start-up With SCCP

3.5 Protection Features

The PD includes the TPS2660 eFuse, which is a wide supply input voltage protection device with a full suite of protection features. This component offers overcurrent, overvoltage, and undervoltage protection as well as slew rate control. In addition, the eFuse provides reverse-polarity protection and integrates back-to-back FETs, which provide reverse-current blocking. The eFuse is enabled and disabled by the microcontroller with a shutdown pin. For system status monitoring, the device provides fault and a current monitor output, which is fed into one of the analog pins of the microcontroller. The PD has the eFuse configured in its auto-retry mode.

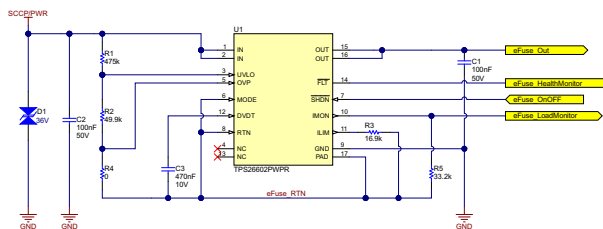


Figure 3-10. PD eFuse Circuit

The eFuse is directly supplied from the SCCP line and is placed before the isolated DC/DC converter system block.

It is important to note that every device connected to the SCCP line that has a bypass capacitor adds to the total capacitance of this line, which is also the SCCP communication bus in the system. The IEEE 802.3bu and 802.3cg standards specify that the total capacitance on the SCCP line must be under 2.64- μ F (types A-D) and under 400-nF (type E) at the PSE output during detection. The input capacitance of the PD must be under 200-nF (types A-D) and under 400-nF (type E).

3.6 Power and Scalability

The isolated DC/DC converter system block is responsible for providing regulated and isolated 24 V to the connected field equipment. To include this functionality, the PD includes a flyback design, which takes advantage of the LM5155 flyback controller with the CSD19531Q5A external N-channel MOSFET.

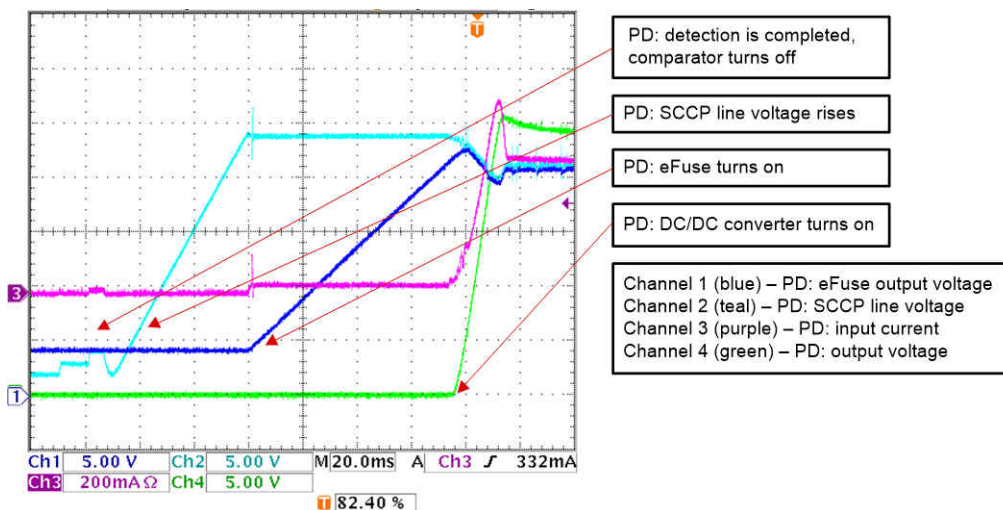


Figure 3-11. PD Power Supply Start-up

On the captured oscilloscope screenshot in Figure 3-11, the start-up of the PD power supply is seen starting at completion of the detection without SCCP (Fast Start-up). The SCCP line voltage rises with the slew rate controlled by the PSE. Once this voltage rises above the eFuse undervoltage lockout (UVLO) threshold, the eFuse turns on and the eFuse output voltage rises with slew rate set by its DVDT capacitor. Finally, once the UVLO threshold of the LM5155 controller is crossed, the DC/DC converter turns on with the slew rate controlled by its soft-start capacitor. The TPS2660 and LM5155 slew rate controls on the PD were tuned so that the inrush current would not exceed the overcurrent protection (I_{LIM}) in the eFuse.

The scalability and adaptability of this design were both very important, because of the various power classes from the IEEE 802.3bu and 802.3cg standards.

The following list shows the PD compatible power classes:

Table 3-3. PD Compatible Power Classes

802.3bu
Class 4: 12 V to 36 V, 97 mA
Class 5: 12 V to 36 V, 339 mA
Class 6: 26 V to 36 V, 215 mA
Class 7: 26 V to 36 V, 461 mA
802.3cg
Class 10: 20 V to 30 V, 92 mA
Class 11: 20 V to 30 V, 240 mA
Class 12: 20 V to 30 V, 632 mA

By changing UVLO, OVP, and other slew rate or protection passive components, the PD can operate with input voltages from 12 V to 36 V and currents of up to at least 632 mA and therefore support all 24 V classes.

4 References

- Texas Instruments, [How to design an Isolated Flyback using LM5155 Application Report](#)
- Texas Instruments, [Extend Network Reach with IEEE 802.3cg 10BASE-T1L Ethernet PHYs Application Report](#)
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- Texas Instruments, [MSP430FR267x, MSP430FR247x Code Examples](#)
- Texas Instruments, [Designing With the MSP430FR4xx and MSP430FR2xx ADC Application Report](#)
- Texas Instruments E2E™ Design Support, [eFuses in factory automation: all-in-one system power protection](#)
- Texas Instruments, [Simplifying EFT, Surge and Power-Fail Protection Circuits in PLC Systems Application Report](#)
- [A Quick Walk Around the Block with PoDL](#)

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