TEXAS INSTRUMENTS

Application Report
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Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints

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TMS470 Microcontroller

ABSTRACT

Tolerances on V_{CCIO}, resistor and capacitor values, and internal silicon variations make calculation of the analog watchdog (AWD) components and period complicated. A method for calculating the component values and corresponding watchdog is presented, along with examples.

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1 Introduction

The purpose of this note is to list explicitly the constraints on the choice of resistor, capacitor, and discharge interval for the analog watchdog and to provide an algorithm for choosing resistor, capacitor, and discharge interval.

2 Analog Watchdog Considerations

In applications using the analog watchdog (AWD) pin[1], the choice of external resistor (R), external capacitor (C), and watchdog discharge time ($T_{WATCHDOG}$) must be chosen *in order to include the interaction with the silicon*. In most cases, the AWD pin has an on-silicon pull-down implemented with a current source to ground. When the AWD key is written, the output buffer sinks current for 256 SYSCLK cycles in order to discharge the external capacitor. The presence/absence of a pull-down, its current range, and the size of the output buffer are device-specific and must be verified against the device data sheet.

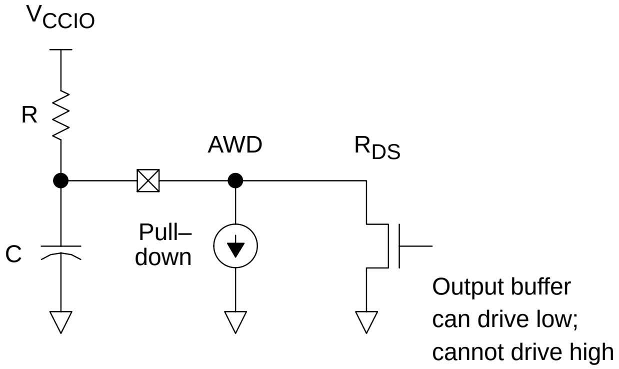

Figure 1. Typical AWD Pin Configuration With External Components

Figure 1 shows a system configuration with external resistor and capacitor. It shows that the important parameters for computing the AWD resistor, capacitor and discharge interval are:

- AWD threshold (min and max)
- V_{CCIO} (min and max)
- Pull-down current (min and max)
- Maximum drain-source resistance for the output buffer when enabled (R_{DSON})
- SYSCLK frequency [discharge is active for 256 cycles]

[1] The AWD pin must be tied to ground if not used. On some devices, AWD has an internal pull-down so that the pin is not required to be connected externally. If there is no pull-down, the AWD must be tied to ground externally in order to prevent AWD resets.

2.1 AWD Threshold

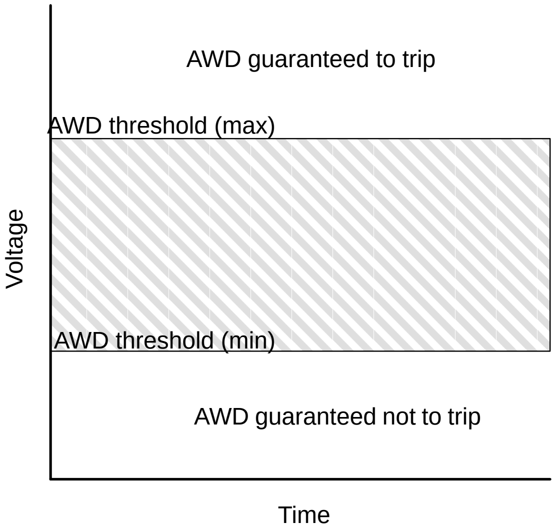

Figure 2. AWD Threshold

The external resistor and capacitor values need to be chosen so that the AWD will trip and generate a reset if not discharged.[2] Specifically, the hardware must allow the voltage on the AWD pin to exceed AWD threshold (max) in order to guarantee a reset on all parts over the specified voltage and temperature ranges.

At the same time, the discharge interval must be chosen so that the voltage on the AWD pin never reaches the minimum AWD threshold. The software must discharge the capacitor while the AWD is guaranteed not to trip and generate a reset.

When the voltage is greater than the minimum AWD threshold and less than the maximum AWD threshold, the AWD will trip on some devices but not all. For the sake of figuring the discharge interval, this region must be completely avoided.

2.2 Effect of Pull-down

The pull-down has the effect of lowering the charging asymptote by $I_{(Pull\text{-}down)}R$ as seen in Figure 3.

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[2] Notice that the AWD when not used is configured so that it cannot trip and generate a reset. When used, the AWD pin must be capable of exceeding AWD threshold (max) in order that a reset is guaranteed.

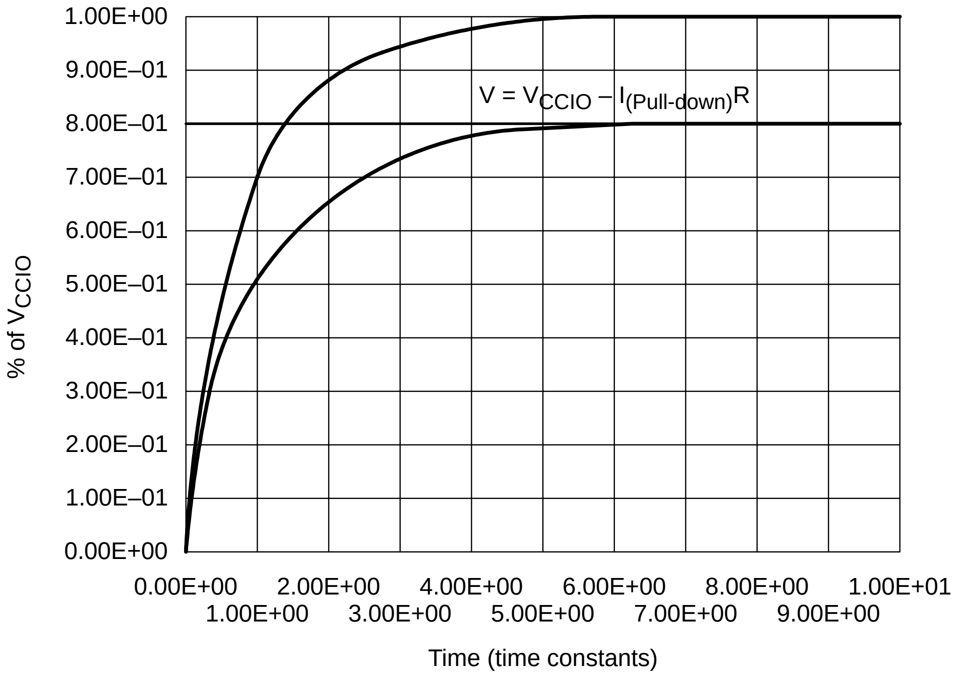

Figure 3. Effect of Pull-down

As the discharge time is fixed by SYSCLK, the capacitor may not discharge fully. If not fully discharged, each charge/discharge cycle will start from a new voltage level until the discharging voltage equals the charging voltage, as shown in Figure 4. At this point, the charging starts from some voltage, V_0, charges to V_F, and is discharged back to V_0.

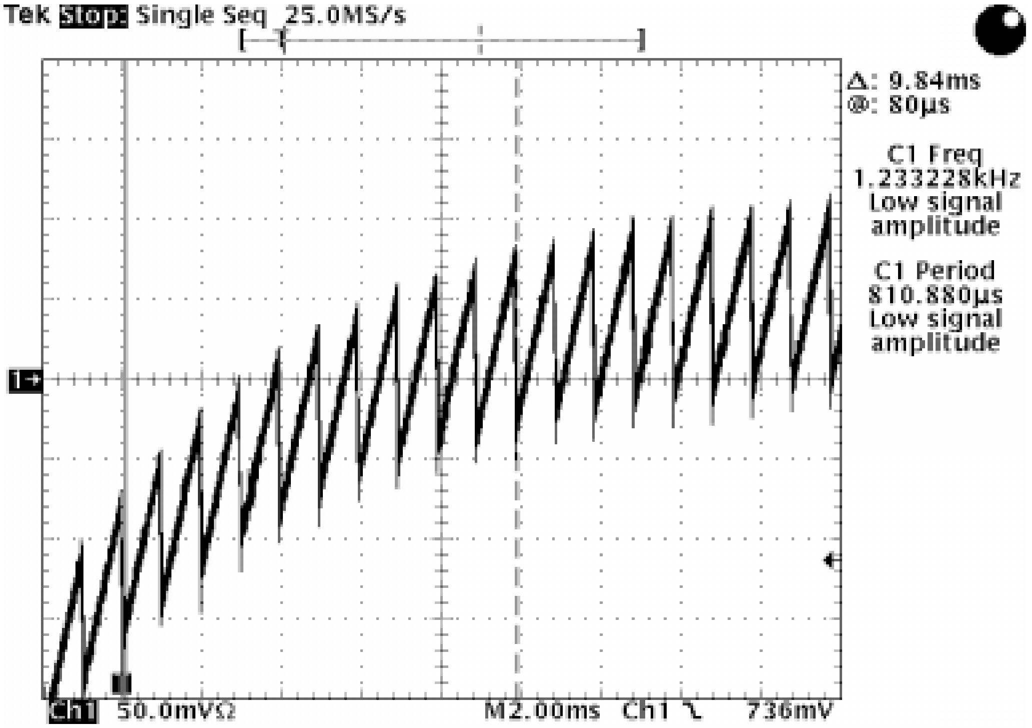

Figure 4. Sequential AWD Charge/Discharge Cycles Reach Charge Asymptote

2.3 Effect of R_{DSON}

The output buffer has a resistance from drain to source. The maximum resistance is determined by the buffer strength, as shown in Table 1. Please see the device-specific data sheet.

Table 1. Maximum Resistance By Buffer Strength

Buffer	$R_{DS_{ON}}$ (max)
2 mA	175 Ω
4 mA	75 Ω
8 mA	45 Ω

The non-zero value of $R_{DS_{ON}}$ means that the capacitor discharge follows an RC discharge curve, as shown in Table 2.

Table 2. RC Discharge Curve

	Capacitance	Resistance	Time
Charging	C	R	$T_{WATCHDOG} – 256 * T_{SYSCLK}$
Discharging	C	$R_{DS_{ON}}$	$256 * T_{SYSCLK}$

The discharge time may not be sufficient to discharge the AWD pin all the way to ground. In this case, some residual charge remains on the capacitor and the next charging cycle begins from the voltage to which the capacitor was discharged.

The resistor, capacitor, discharge interval must be chosen so that the AWD never trips – *guaranteeing that the pin does not trip during the first charge/discharge cycle is* ***not*** *sufficient*.

3 Method for Calculating AWD Components and Period

The presence of the pull-down circuitry on AWD changes the procedure for determining an appropriate RC combination. The pull-down effectively creates a maximum allowable resistor size. When the pull-down is absent, the calculated resistor is the minimum resistor size for a given RDS, charge time and operating frequency.

3.1 With a Pull-down Present

1. Calculate the maximum allowable resistance (including tolerances).
2. Select a discharge time for which to calculate RC values.
3. Select a resistor value such that the resistance with the tolerance is less than the maximum allowable resistance.
4. The voltage on the AWD pin will settle to charge and discharge between two voltage values. The high end of these voltage values must be less than the minimum AWD trip voltage. Calculate the low-end voltage.
5. Using the low end voltage, compute the minimum capacitance value (including tolerances).
6. Verify functionality with worst case resistance and worst case capacitance.

3.2 Without a Pull-down Present

1. Select a discharge time for which to calculate RC values.
2. The voltage on the AWD pin will settle to charge and discharge between two voltage values. Select the high end and low-end (V0) of the voltage ranges. The high-end of these voltage is assumed to be the minimum AWD trip voltage.
3. Compute associated maximum capacitance (including tolerances).
4. Compute the minimum resistance (including tolerances); the resistance is a function of R_{DS}, charge time, operating frequency, high- and low-end voltages specified in step 2.
5. Verify functionality with worst case resistance and worst case capacitance.

The same algorithm cannot be used for both cases because with a pull-down present, the discharge is effectively linear (due to large capacitance). With a smaller capacitance, the discharge is logarithmic and the linear assumption is grossly inaccurate.

4 Examples

4.1 Choosing External Resistor and External Capacitor for the AWD (With Internal Pull-down)

For the sake of clarity, a specific example is worked in parallel with the general constraints. For this example, the watchdog discharge interval is assumed to be 1 ms and the electrical conditions are:

Table 3. Electrical Conditions

	Min	Nom	Max
AWD Threshold (V)	1.35		1.80
V_{CCIO} (V)	3.0		3.6
Pull-down current (µA)	5		42
Drain-source resistance (Ω)			175
SYSCLK frequency (MHz)		16	
SYSCLK period (ns)		62.5	

NOTE: The Pull-down current value applies only when a pull-down is present.

1. Calculate maximum allowable resistance (including tolerances).

The voltage on the AWD pin must be capable of exceeding $V_{AWD_{THRESHOLD}}$(max). The pull-down creates a voltage drop across the resistor which reduces the maximum voltage at the AWD pin. The voltage at the AWD pin must be able to equal or exceed the maximum AWD threshold voltage.

$$V = V_{CCIO} - I_{pull-down}R \geq V_{AWD_{THRESHOLD}}(max)$$

$$V_{CCIO}(min) - I_{pull-down}(max)R \geq V_{AWD_{THRESHOLD}}(max)$$

$$R \leq \frac{\left(V_{CCIO}(min) - V_{AWD_{THRESHOLD}}(max)\right)}{\left(I_{pull-down}(max)\right)}$$

For the specific example shown above, if

$V_{CCIO}(min) = 3.0\ \text{V}$

$V_{AWD_{THRESHOLD}}(max) = 1.80\ \text{V}$

and $I_{pull\text{-}down}(max) = 42\ \mu\text{A}$

then $R \leq 28.5\ \text{k}\Omega$

2. Select a discharge time for which to calculate RC values.

Per the example, 1 ms.

3. Select a resistor value such that the resistance with the tolerance is less than the maximum allowable resistance.

The maximum resistance is 28.5 kΩ. A ±5% resistor with 27.0 kΩ meets this requirement.

4. The voltage on the AWD pin will settle to charge and discharge between two voltage values. The high end of these voltage values must be less than the minimum AWD trip voltage. Calculate the low-end voltage. V_0

The presence of the drain-source resistance, R_{DS}, means that the voltage on the AWD pin is discharged through an RC circuit. The discharge may not be carried all the way to ground.

The discharge voltage after many charge/discharge cycles can be computed by recognizing that the current through the output buffer and pull-down can be treated as an average “pull-down” current. This average current is a weighted average of the pull–down and the average current through the output buffer when the buffer is enabled.

$$I(avg) = \frac{\left(I_{pull-down}T_{WATCHDOG} + 256I_{outputbuffer}(avg)T_{SYSCLK}\right)}{T_{WATCHDOG}}$$

$$I(avg)(min) = \frac{\left[I_{pull-down}(min)T_{WATCHDOG} + 256\frac{\left(\frac{(V_F+V_0)}{2}\right)}{(R_{DS}(max))}T_{SYSCLK}\right]}{T_{WATCHDOG}}$$

$$V_0(max) = V_{CCIO}(max) - I(avg)(min)R$$

$$V_0(max) = \frac{\left(V_{CCIO}(max) - I_{pull-down}(\text{min})R(min) - \frac{(256{*}T_{SYSCLK}R(min))}{(2T_{WATCHDOG}R_{DS}(max))}V_F\right)}{\left(1 + \frac{(256{*}T_{SYSCLK}R(min))}{(2T_{WATCHDOG}R_{DS}(max))}\right)}$$

In order to guarantee that the watchdog does not trip, V_F must be less than $V_{THRESHOLD}$ (min).

For the specific example shown above,

$V_{CCIO}(max) =$ 3.6 V

$I_{pull\text{-}down}(min) =$ 5 µA

$R(min) =$ 27 kΩ * 0.95 = 25.65 kΩ

$T_{WATCHDOG}$ = 1 ms

$V_F < V_{THRESHOLD}\ (min) =$ 1.35 V

$R_{DS}(max) =$ 175 Ω

$T_{SYSCLK} =$ 62.5 ns

$$V_0(max) = \frac{\left(3.6\text{V} - (5\mu\text{A})(25.65\text{k}\Omega) - \frac{(256(62.5\text{ns})(25.65\text{k}\Omega))}{(1\text{ms}(2*175\Omega))}1.35\text{V}\right)}{\left(1 + \frac{(256*(62.5\text{ns})(25.65\text{k}\Omega))}{(1\text{ms}(2*175\Omega))}\right)}$$

$V_0(max)$ = 0.87 V

5. Using the low end voltage, V_0, compute the minimum capacitance value (including tolerances).

After many charge/discharge cycles, the AWD capacitor charges between V_F and V_0 (calculated in step 2). The charging must not exceed $V_{THRESHOLD_{MIN}}$.

$$V_F = V_{CCIO}(max)\left(1 - \exp\left[-\frac{T_{charge}}{RC}\right]\right) + V_0 \exp\left[-\frac{T_{charge}}{RC}\right]$$

$$\exp\left[-\frac{T_{charge}}{RC}\right] = \left[\frac{(V_{CCIO}(max) - V_F)}{(V_{CCIO}(max) - V_0)}\right]$$

$$C = \frac{T_{charge}}{\left(R(max) * \ln\left[\frac{(V_{CCIO}(max) - V_F)}{(V_{CCIO}(max) - V_0)}\right]\right)}$$

For the specific example shown above:

$T_{charge} = T_{WATCHDOG} - 256 * T_{SYSCLK} =$ 1 ms – 256* 62.5 ns = 0.984 ms

$R(max) =$ 28.35 kΩ

$V_{CCIO}(max) =$ 3.6 V

V_F = 1.35 V

V_0 = 0.87 V

$$C = \frac{(0.984\text{ms})}{\left(28.35\text{k}\Omega * \ln\left[\frac{(3.6\text{V} - 1.35\text{V})}{(3.6\text{V} - 0.87\text{V})}\right]\right)}$$

$C(min) = 0.15\ \mu F$

6. Verify functionality with worst case resistance and worst case capacitance.

4.2 Choosing External Resistor and External Capacitor for the AWD (With No Internal Pull-down)

For the sake of clarity, a specific example is worked in parallel with the general constraints. For this example, the watchdog discharge interval is assumed to be 10 ms and the electrical conditions are shown in Table 3 (along with a pull-down current value, not applicable to this example).

1. Select a discharge time for which to calculate RC values.

Per the example, 1 ms.

2. The voltage on the AWD pin will settle to charge and discharge between two voltage values. Select the high end and low end (V0) of the voltage ranges. The high end of these voltage is assumed to be the minimum AWD trip voltage.

Discharge to 1 mV.

3. Compute associated maximum capacitance (including tolerances).

When the watchdog discharges the capacitor, its discharge level is a percentage of the value at discharge. The percentage is based on how many time constants the capacitor is discharged. The capacitor must be chosen so that the capacitor can be discharged from the highest allowable voltage to the desired level, $V_{DischargeLevel}$.

$$V = V_0 \exp\left[-\frac{t}{(R_{DS}C)}\right]$$

$$C = -\frac{t}{\left(R_{DS} * \ln\left[\frac{V}{V_0}\right]\right)}$$

For the specific example shown,

$V = V_{DischargeLevel} = 1\text{ mV}$

$V_0 = V_{THRESHOLD}(min) = 1.35\text{ V}$

$R_{DS} = 175\ \Omega$

$t = 256 * T_{SYSCLK} = 256 * 62.5\text{ ns} = 16\ \mu s$

$$C = -\frac{(16\mu s)}{\left(175\Omega * \ln\left[\frac{1mV}{1.35V}\right]\right)} = 12.7nF$$

4. Compute the minimum resistance (including tolerances); the resistance is a function of R_{DS}, charge time, operating frequency, high and low end voltages specified in step 2.

Set a discharge point – $V_{DISCHARGE}$ – (less than $V_{THRESHOLD}(min)$) in order to compute R. For this example, $V_{DISCHARGE}$ =1 V.

$$V = V_{CCIO}\left\{1 - \exp\left[-\frac{t_{charge}}{RC}\right]\right\} + V_0 \exp\left[-\frac{t_{charge}}{RC}\right]$$

$$V_{DISCHARGE} = V_{CCIO}(max)\left\{1 - \exp\left[-\frac{t_{charge}}{RC}\right]\right\} + V_{DISCHARGELEVEL} \exp\left[-\frac{t_{charge}}{RC}\right]$$

$$\exp\left[-\frac{t_{charge}}{RC}\right] = \left[\frac{(V_{CCIO}(max) - V_{DISCHARGE})}{(V_{CCIO}(max) - V_{DISCHARGELEVEL})}\right]$$

$$R(min) = -\frac{t_{charge}}{\left(C(min) * \ln\left[\frac{(V_{CCIO}(max) - V_{DISCHARGE})}{(V_{CCIO}(max) - V_{DISCHARGELEVEL})}\right]\right)}$$

For the specific example above,

$V_{DISCHARGE} = 1\ \text{V}$

$V_{DISCHARGELEVEL} = 1\ \text{mV}$

$V_{CCIO}(max) = 3.6\ \text{V}$

$t_{charge} = 10\ \text{ms} – 16\ \mu\text{s} = 9.984\text{ms}$

Assuming a 10 nF capacitor with ±20%, *C(min)* = 8 nF

$$R(min) = -\frac{9.984\text{ms}}{\left(8\text{nF} * \ln\left[\frac{(3.6\text{V} - 1\text{V})}{(3.6\text{V} - 1\text{mV})}\right]\right)} = 385\text{k}\Omega$$

5. Verify functionality with worst case resistance and worst case capacitance.

Appendix A Experimental Results

The following data was taken on a TMS470R1F369 device in order to offer some validation of the algorithm proposed in the application note. The validation sequence presented is not intended for production use but instead ONLY for validation of the application note.

With an external resistor divider of 2 kΩ in series with 499 Ω, the AWD voltage sits at 1.02 V when not discharging and 212 mV when discharging (see Figure A–1). The current is measured at 2.03 mA. The 212 mV discharge level implies an R_{DS} of 132 Ω.

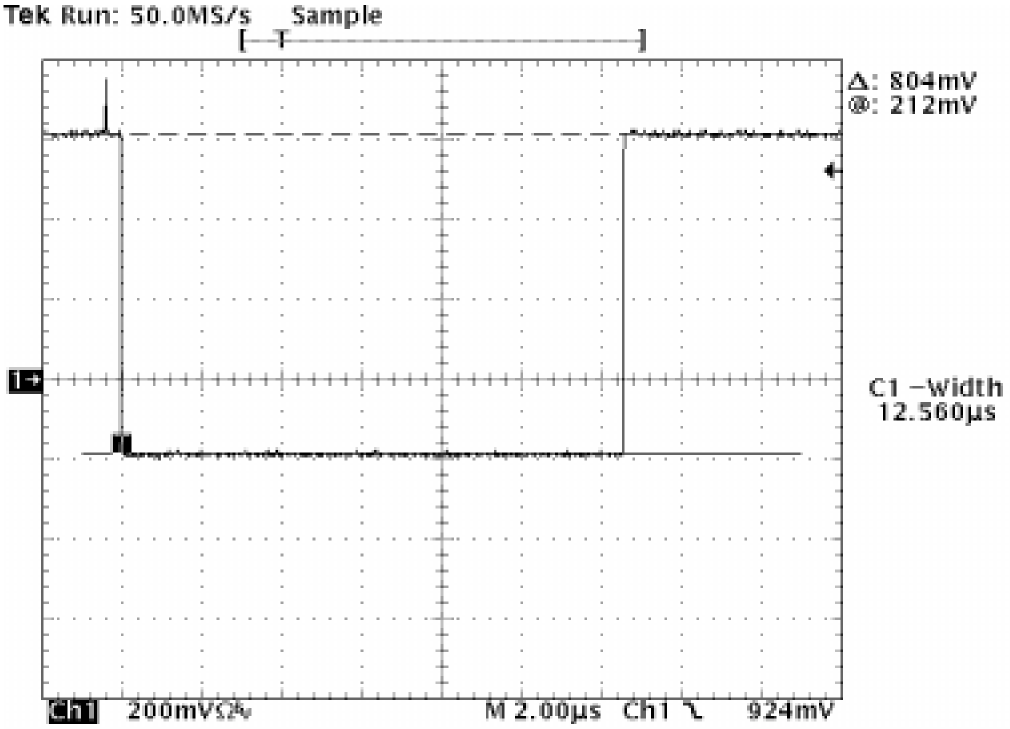

Figure A–1. Voltage Level on AWD Pin (With Resistor Divider) During Discharge

Within the spreadsheet, the specified R_{DS} value is replaced with that calculated above. The specific resistance, capacitance, and voltage are measured to remove tolerances.

R = 33.5 kΩ

C = 1.07 µF

V_{CCIO} = 5.03 V

$T_{WATCHDOG}$ = 989 µs

SYSCLK = 20 MHz

The spreadsheet predicts a V_0 value of 1.03 V and a V_{max} value of 1.14V.

The measurement yields a V_0 value of 869 mV and a V_{max} value of 983 mV, as seen in Figure A–2.

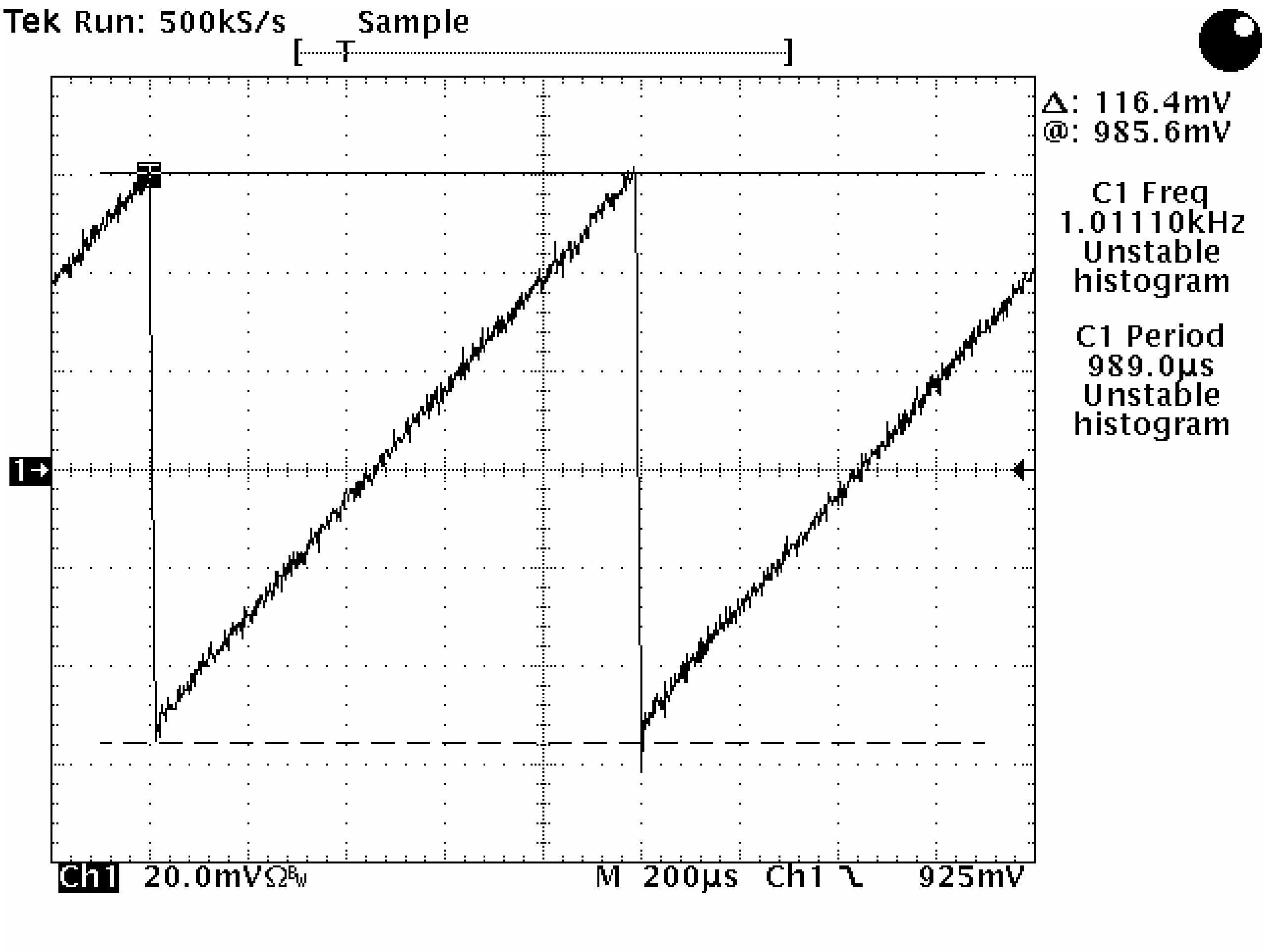

Figure A–2. AWD Charge/Discharge Cycles Used to Verify V_0 and V_{max} Voltage Levels

That is, the method of calculating RC values in this application note predicts correctly within 150 mV, and the prediction errs on the conservative side.

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