Application Report
SPNA107–April 2007

Power Mode Settings Within the TMS470

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ABSTRACT

The TMS470 family of ARM7 microcontrollers has four modes of operation: Standby, Idle, Halt and Run. The device starts in Run mode, and the other three are considered low-power modes. Additional power savings are available by disabling the flash memory.

This application report explains how to change into the low-power modes and how to disable and enable the flash.

This application report also describes idiosyncrasies associated with the disabling and bypassing of the PLL.

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1 Introduction

This application report describes how to set the TMS470 family of ARM7 microcontrollers into each of the four modes of operation: Standby, Idle, Halt, and Run. It also describes how to enable and disable the flash memory.

This document starts by listing and describing the clocks associated with the TMS470 family of devices, followed by the state of these clocks for each mode of operation. The remaining sections describes each mode of operation and how to program them and how to disable the flash.

2 Clock Descriptions

The TMS470R1xxx family of devices has various clocks. Table 1 describes these clocks and where they are used in the devices.

Table 1. Clock Descriptions

Clock	Description
ACLK	ACLK is the output clock from the oscillator/PLL prior to the prescale divider. The system synthesizes the other device clocks off the prescaled ACLK. The clock control module synthesizes SYSCLK from ACLK by dividing the frequency by the prescale divider (GLBCTRL).
SYSCLK	SYSCLK clocks these modules: RAM HET Flash control registers Flash system control registers DMA
MCLK	MCLK operates at the same frequency as SYSCLK and is inverted (180 out of phase). MCLK clocks the CPU.
ICLK	ICLK is generated from the SYSCLK, and the frequency is controlled by a prescale (PCR.4:1). ICLK clocks peripherals.
RTICLK	RTICLK operates at the same frequency and is in phase with the SYSCLK. RTICLK clocks only the real-time interrupt counters.
ADCLK	The ADC core is synchronized with the internal ADC clock. ADCLK is derived from ICLK.

2.1 Active Clock Domains

Table 2 shows the state of each clock for each mode of operation.

Table 2. Clock Domains

Device Condition	LPM Bits	Oscillator	ACLK	RTICLK	SYSCLK	ICLK	MCLK
RUN	LPM.1:0 = 0x00	Active	Active	Active	Active	Active	Active
RST low	N/A	Active	Active	Active	Active	Active	Active
IDLE	LPM.1:0 = 0x01	Active	Active	Active	Active	Active	Inactive
STANDBY	LPM.1:0 = 0x02	Active	Active	Active	Inactive	Inactive	Inactive
PORRST low	N/A	Active	Inactive	Inactive	Inactive	Inactive	Inactive
HALT	LPM.1:0 = 0x03	Inactive	Inactive	Inactive	Inactive	Inactive	Inactive

3 Setting Low-Power Modes and Disabling the TMS470 Flash

This section explains the procedures for entering standby and halt mode on the TMS470R1xxx family of devices. The flash module must be configured for sleep mode before entering device standby or halt mode.

- Standby mode

  When the TMS470R1xxx device is in standby mode, the oscillator, ACLK, and RTICLK are active. SYSCLK, ICLK, and MCLK are inactive.
- Halt mode

  When the TMS470R1xxx device is in halt mode, the oscillator, ACLK, RTICLK, SYSCLK, ICLK, and MCLK are inactive.
- Flash sleep mode

  When the flash module enters sleep mode, both banks and charge pump are asleep. While the banks are asleep, both the sense reference and the sense amplifiers are disabled. While the charge pump is in sleep mode, all circuits are disabled.

The flash module consists of the flash banks, charge pump, power and mode control logic, data path, burst logic, and write/erase state machines. Flash banks are a group of flash sectors, which share input/output buffers, data paths, sense amplifiers, and control logic. The charge pump consists of voltage generators and associated control.

3.1 Automatic Power Down of Flash Banks

The flash module provides a mechanism to automatically power down flash banks after they have not been accessed for a user-programmable time. Special timers automatically sequence the power up and power down of each bank independently of each other. The charge pump module has its own independent power up/down timers.

3.1.1 Sequence for Bank Power Down

1. Enter flash configuration mode.

   GCR |= FLCONFIG;
2. Set up the PSLEEP in the FMMAC1 register.
   - Pump Sleep (PSLEEP) contains the starting count value for the charge pump sleep down counter. While the charge pump is in sleep mode, the power-mode management logic holds the charge pump sleep counter at this value. When the charge pump exits sleep power mode, the down counter delays from 0 to 32767 SYSCLK cycles before putting the charge pump into standby power mode (the flash module cannot exit charge pump sleep mode directly to active mode).

   FMMAC1 = PSLEEP_MAX;
3. Set up PSTDBY, PMPPWR, and BANK in the FMMAC2 register.
   - Pump Standby (PSTDBY) contains the starting count value for the charge pump standby down counter. While the charge pump is in standby mode, the power-mode management logic holds the charge pump standby counter at this value. When the charge pump exits standby power mode, the down counter delays from 0 to 2047 SYSCLK cycles before putting the charge pump into active mode.
   - Flash Pump Fallback Power Mode (PMPPWR) contain the bits to select what power mode the charge pump enters after the pump active grace period (PAGP) counter has timed out.
   - Bank Enable (BANK) selects which bank is enabled for operations.

   FMMAC2 = BANK0_ENA + PMPPWR_SLEEP + PSTDBY_MAX;

4. Set up BAGP, BSTBY, and BNKPWR in the FMBAC1 register.
   - Bank Active Grace Period (BAGP) contains the starting count value for the BAGP down counter. Any access to a given bank causes its BAGP counter to reload the BAGP value for that bank. After the last access to this flash bank, the down counter delays from 0 to 255 SYSCLK cycles before putting the bank into one of the fallback power modes as determined by BNKPWR[1:0] in this register.
   - Bank Standby (BSTBY) contains the starting count value for the bank standby down counter. While the bank is in standby mode, the power-mode management logic holds the bank standby counter at this value. When the bank exits standby power mode, the down counter delays (counts down to zero) from 0 to 63 SYSCLK cycles before putting the bank into bank active mode.
   - Bank Power Mode (BNKPWR) describes the fallback power mode that the flash bank enters after the bank active grace period counter has timed out.

   FMBAC1 = BNKPWR_SLEEP + BSTDBY_MAX + 0xff00;
5. Setup BSLEEP,WAIT[7:4] and WAIT[3:0] in the FMBAC2 register.
   - Bank Sleep (BSLEEP) contains the starting count value for the bank sleep down counter. While the bank is in sleep mode, the power-mode management logic holds the bank sleep counter at this value. When the bank exits sleep power mode, the down counter delays from 0 to 127 SYSCLK cycles before putting the bank into active mode.
   - Wait State Counter (WAIT[7:4]) contains the starting count value for the wait state down counter. The down counter delays from 0 to 15 SYSCLK cycles before indicating that data is available. For normal operation, these bits are set to 000 for single cycle standard read mode, or to 001 for pipeline mode. Wait bits 7:4 must match wait bits 3:0.
   - Wait State Counter (WAIT[3:0]). For normal operation, these bits are set to 000 for single cycle standard read mode, or to 001 for pipeline mode. Wait bits 3:0 must match wait bits 7:4.

   FMBAC2 = PIPELINE_MODE + BSLEEP_MAX;
6. Setup ENPIPE in the FMREGOPT register.
   - Enable Pipe Mode (ENPIPE). Pipeline mode is active when ENPIPE is set, configuration mode is disabled, and the MCU F05 flash module is not in halt mode. Pipeline mode is overridden in configuration mode and in halt mode. The default value of ENPIPE is device specific. See the device-specific data sheet for the reset state of ENPIPE.

   FMREGOPT = ENPIPE
7. Enter Halt mode. After executing the HALT instruction, a dummy access to this register is needed to enter the low-power mode.

   CLKCNTL |= LPM_HA;

   dummy=CLKCNTL;

3.1.2 Code Example for Setting the CLKCNTL Register Into Standby Mode

```
int dummy
CLKCNTL = CLKSR_SYSCLK + CLKDIR + CLKDOUT + LPM_STANDBY;
dummy = CLKCNTL;          // Dummy Read required
```

3.1.3 Code Example for Setting the Idle Mode

```
int dummy
CLKCNTL = CLKSR_SYSCLK + CLKDIR + CLKDOUT + LPM_IDLE;
dummy = CLKCNTL;          // Dummy Read required
```

3.1.4 Code Example for Setting the Halt Mode

```
int dummy
CLKCNTL = CLKSR_SYSCLK + CLKDIR + CLKDOUT + LPM_HA;
dummy = CLKCNTL;          // Dummy Read required
```

3.1.5 Code Example for Setting the Run Mode

```
int dummy
CLKCNTL = CLKSR_SYSCLK + CLKDIR + CLKDOUT + LPM_RUN;
dummy = CLKCNTL;         // Dummy Read required
```

3.1.6 Code Example for the A64, A128, and A256

```
GCR |= FLCONFIG;                                  // Must be in flash config mode
FMMAC1 = PSLEEP_MAX;                              // pump sleep to standby time
FMMAC2 = BANK0_ENA + PMPPWR_SLEEP + PSTDBY_MAX;   // Pump power sleep
FMBAC1 = BNKPWR_SLEEP+ BSTDBY_MAX + 0xff00;       // Bank power sleep 256 cycles
                                                  // before flash shut down
FMBAC2 = PIPELINE_MODE + BSLEEP_MAX;              // 1 wait states
FMREGOPT = ENPIPE;                                // ENABLE PIPELINE MODE

CLKCNTL |= LPM_HA;                                // Halt mode
dummy=CLKCNTL;                                    // Dummy access
```

3.1.7 Code Example for the B1M

```
GCR |= FLCONFIG;                                  // Must be in flash config mode
FMMAC1 = PSLEEP_MAX;                              // pump sleep to standby time
FMMAC2 = BANK0_ENA + PMPPWR_SLEEP + PSTDBY_MAX;   // Pump power sleep bank0
FMBAC1 = BNKPWR_SLEEP+ BSTDBY_MAX + 0xff00;       // Bank power sleep 256 cycles
                                                  // before flash shut down
FMBAC2 = PIPELINE_MODE + BSLEEP_MAX;              // 1 wait states

FMMAC2 = BANK1_ENA + PMPPWR_SLEEP + PSTDBY_MAX;   // Pump power sleep bank1
FMBAC1 = BNKPWR_SLEEP+ BSTDBY_MAX + 0xff00;       // Bank power sleep 256 cycles
                                                  // before flash shut down
FMBAC2 = PIPELINE_MODE + BSLEEP_MAX;              // 1 wait states
FMREGOPT = ENPIPE;                                // ENABLE PIPELINE MODE

CLKCNTL |= LPM_HA;                                // Halt mode
dummy=CLKCNTL;                                    // Dummy access
```

3.2 Register Description for Disabling the Flash

Table 3 describes the register settings necessary to disble the flash.

Table 3. Registers for Disabling Flash

Register	Description
CLKCNTL	Configures the CLKOUT pin and a bit that controls the module low-power mode. See the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
GLBCTRL	Controls the PLL and one bit configures the flash module. See the *TMS470R1x System Module Reference Guide* (literature number SPNU166)
FMBAC1	The Bank Access Control Register 1 (BAC1) is a half-word-access only register. It controls bank standby mode wait state generation, bank fall back power mode and bank Active Grace Period (AGP) delay. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).
FMBAC2	The Bank Access Control Register 2 (BAC2) is a half-word-access only register. It controls special burst and standard read wait state generation, bank sleep delay, and OTP sector protection. There is one BAC2 register for each bank in the flash module. The bank is selected via BANK[2:0] of the MAC2 register. Since only one bank at a time can be selected by MAC2, only the selected bank's register appears at this address. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).
FMMAC1	The Module Access Control Register 2 is a half-word-access only register. It supports pump sleep wait state generation and Level 1 protection. MAC1 is a global register; therefore, there is only one for the entire flash module, regardless of the number of banks present. See the *TMS470R1x F05 Flash Module Reference Guide* (literature number SPNU213).

4 Rules for Enabling and Bypassing the PLL

The evaluation boards for the TMS470 devices feature a PLLDIS (PLL disable) jumper that enables and bypasses the ZPLL. With the ZPLL bypassed, the oscillator becomes the system clock.

- Jumper closed: 3.3 V to PLLDIS – Bypass mode
- Jumper open: PLLDIS is pulled down with a 10-kΩ resistor

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1 to 8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other B1M device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

It should be emphasized that the PLL is not disabled or shut off if the user is trying to achieve a lower power mode by inserting the PLLDIS jumper. The PLL is only bypassed, which allows the oscillator to become the system clock and essentially the device runs much slower. See the *TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212) for more details.

5 References

1. *TMS470R1x System Module Reference Guide*, Texas Instruments (SPNU189)

2. TMS470R1B1M Kickstart™ Development Kit from IAR, Texas Instruments, http://focus.ti.com/docs/toolsw/folders/print/spnc010.html

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