

Interfacing the Embedded 12-Bit ADC in a TMS570LS31x/21x and RM4x Series Microcontrollers

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ABSTRACT

The Texas Instruments Hercules™ Arm® Safety Microcontrollers TMS570LS31x/S21x and RM4x series of products have two 12-bit analog-to-digital converters (ADC). This document provides the device configuration and layout recommendations to achieve the best performance of the embedded ADC. These include layout requirements on power and ground, decoupling and bypass capacitor requirements on voltage reference pins and power pins, typical circuit and requirements in front of ADC input channel, recommendations on ADCLK configuration, phase-locked loop (PLL) settings and trigger signal to achieve the best effective number of bits (ENOB), how to do calibrate and compensate, and how to use over-sampling to improve resolution.

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1 Description

Two 12-bit ADC cores and 24 ADC input channels are implemented on most TMS570LS31x/21x and RM4 devices. Figure 1 illustrates the connection of the two A/D converter peripherals on the TMS570 device.

- Each ADC supports 16 channels
- Each ADC has 8 dedicated channels
- Each ADC has a dedicated pin for event trigger
- Two ADC cores share 8 channels
- The references are shared between the two cores

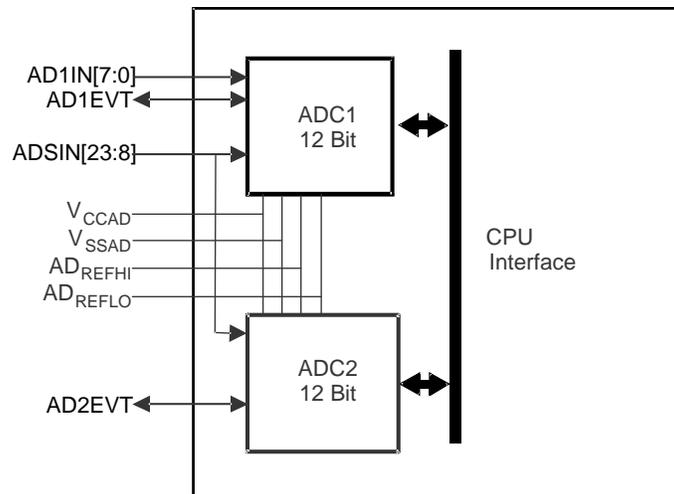


Figure 1. Channel Assignments of Two ADC Cores

2 Circuit Design and Layout Requirement

2.1 General Requirements

The most important thing of an ADC is to protect the analog part from excessive digital noise. The following section states the general recommendations to use for the TMS570LS31x/21x embedded ADC.

First of all, the board should be partitioned into 'Analog Region' and 'Digital Region'. The ADC inputs, V_{CCAD} , V_{SSAD} , AD_{REFLO} and AD_{REFHI} are only allowed to route in the 'Analog Region'. The digital signals and the ADC event triggers are only allowed to route in the 'Digital Region'. If the digital signals and analog signals are mixed up, the digital noise couples to the analog signal. This may generate 'random noise', offset and gain errors on the conversion result. If you have to route a digital signal in the 'Analog Region', try to make the analog and the digital signals perpendicular to each other to minimize the coupling.

Second, ground strategy is also very important. A split ground plane can be used to prevent digital logic ground currents from contaminating the analog signals. However, it should be used only when necessary because it introduces many potential risks. If your board has some very noisy components or huge current consumption components, for example, switching power supplies and MOSFET drivers for the motor, you need to split your ground plane or use star ground connection carefully to reduce the noise coupling to AD circuit. You might also need to shield the noisy components to prevent field coupling in those cases, too. However, splitting the ground plane under TMS570LS20x/10x devices is not required due to the following reasons:

Reason 1 - DC current:

In a 3.3-volt system, the least significant bit (LSB) of a 12-bit ADC represents $3.3 \text{ V}/4096 = 0.8 \text{ mV}$. If the DC drop on the ground plane from external analog input to the TMS570 device is less than one LSB, it is not necessary to split the ground plane to prevent the DC current.

DC current spreads from the source to the destination evenly on the ground plane. The largest DC current for a TMS570LS device is the V_{CC} current. The worst case current is around 400 mA. An example of the ground plane is shown in Figure 2. This component placement is not optimized because the IC that consumes most of the power is far away from the power supply.

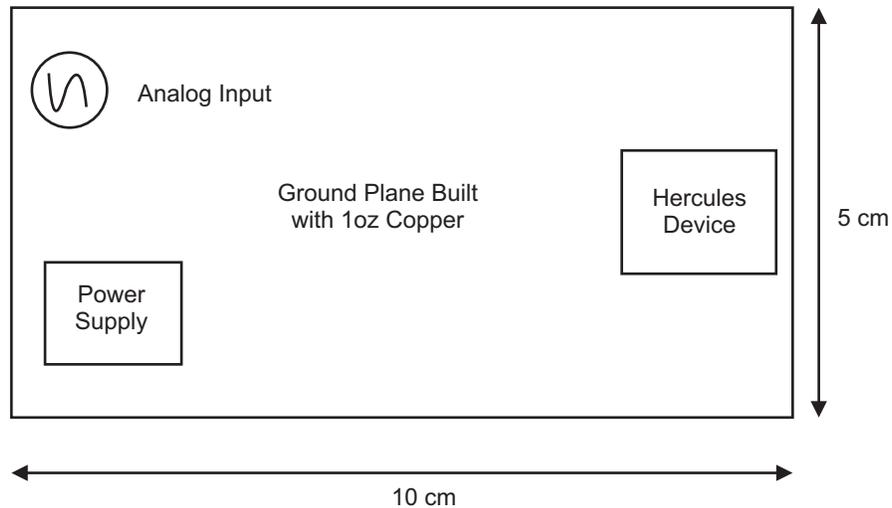


Figure 2. Ground Plane Example

The resistance of a 1 oz of copper ground plane is about $0.5 \text{ m}\Omega/\bullet$, where \bullet represents a square area with equal length and width. The ground plane in Figure 2 looks like a 2:1 (length: width) rectangle. The worst case voltage drop on the ground plane is around $0.5 \text{ m}\Omega/\bullet \times 2\bullet \times 400 \text{ mA} = 0.4 \text{ mV}$, which is only half LSB. In a real case, after you optimize your power delivery and your component placement, running at normal voltage and room temperature, the voltage drop on the ground plane due to the MCU itself should be less than half LSB.

Here, only the power consumed by the Hercules MCU itself is considered. If your system includes some high current device, for example, a motor driver consumes current in the order of an ‘Amp’, you need to split your ground plane to avoid DC voltage drop on the ground plane

Reason 2 - High frequency current:

Due to the skin effect (to minimize the impedance in the path), the high frequency return current flowing through the plane is restricted to a narrow area underneath and above the PCB trace carrying the outgoing current. The equations to calculate the current distribution on an infinite and finite ground plane can be found in [1]. Figure 3 is a calculation example (the left part shows the setup while the right part shows the calculated current distribution).

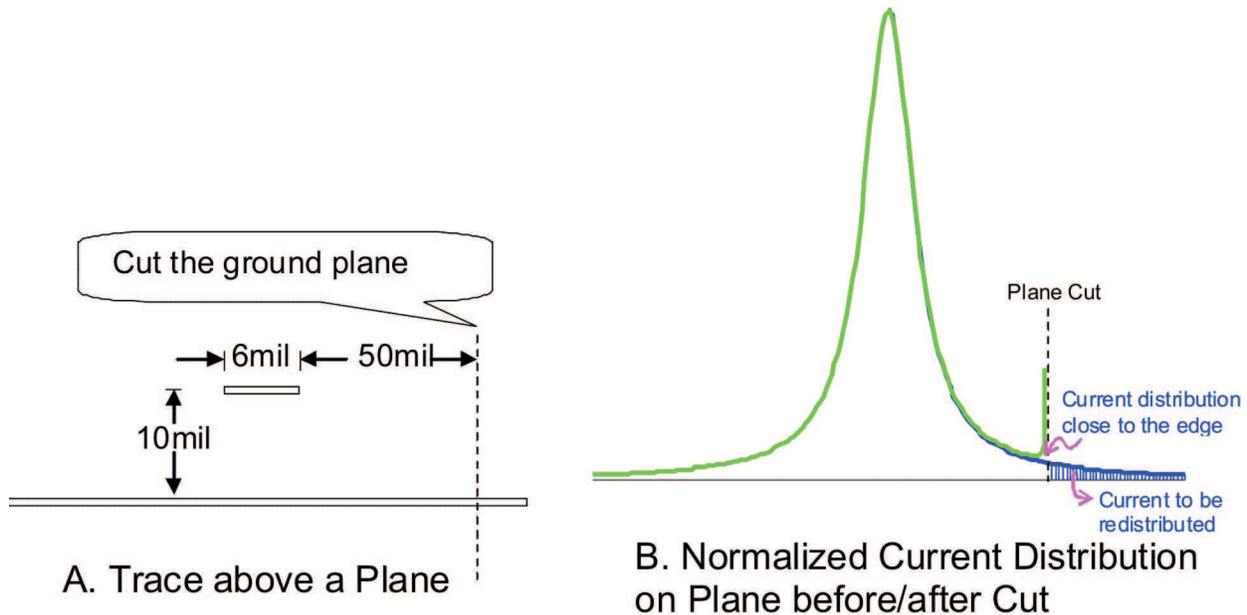


Figure 3. Current Distribution on an Infinite and a Cut Ground Plane

Since almost all the current flows underneath and above the trace, splitting the ground does not help much to reduce the high frequency coupling between analog and digital circuits.

Splitting the ground plane should be done only when you know where the ground current flows. If you have to split the ground plane, follow two important rules [2]:

- Do not run any signal across the gap of a split ground plane. The analog ground and the digital ground should be connected at one point and all the traces commuting between the analog and digital region should be routed over this bridge point as shown in the left part of Figure 4. By doing this, the current returns directly underneath and above each trace and the current loop area is minimized. A high frequency signal across the gap, like the right part in Figure 4, can generate both signal integrity problems (discontinuities) and EMI problems. Even if it is low frequency or DC signal, it might also carry high frequency noise due to the on-board and on-chip coupling.

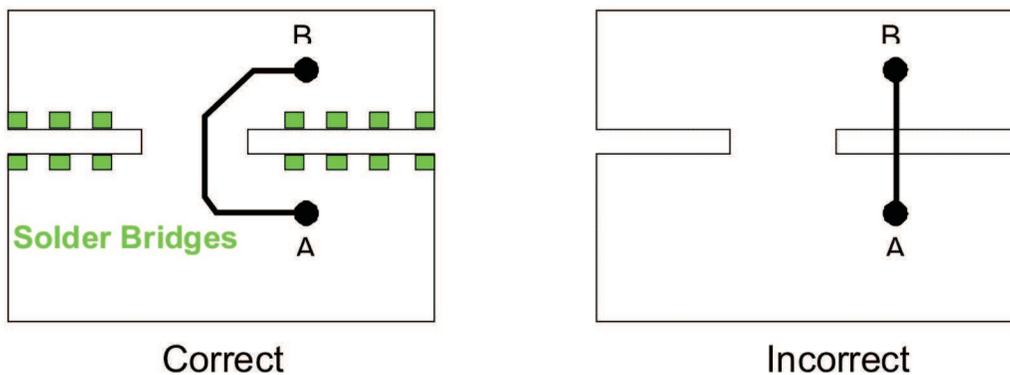


Figure 4. Signal Traces Crossing the Gap of Ground Plane

- Reserve a few solder-bridges along the gap (every half inch) of the ground plane as shown in the left part of Figure 4. You can connect them in case the ground gap introduces problems in your system.

2.2 Power and Reference Voltage

V_{CCAD} and V_{SSAD} are not truly analog power and grounds. They contain digital noise generated during conversion. V_{SSAD} is also connected to V_{SS} through p-substrate inside the IC, the high frequency V_{SS} current in the digital and core area can also follow through this V_{SSAD} pin to the board ground. A minimum 100 nF decoupling capacitor should be placed between V_{CCAD} and V_{SSAD} before they reach the power and ground plane as shown in Figure 5.

V_{REFHI} and V_{REFLO} are the reference voltages for the conversion. They should be extremely clean. Random noise on these two pins leads to random noise on the conversion result. With synchronized noise (with the clock inside the device) presenting on these two pins, the conversion result looks 'stable' but has offset and gain errors. A minimum 100 nF decoupling capacitor should be placed between them before they reach the power and ground plane as shown in Figure 5. Do not share VIAs between V_{SSAD} and V_{REFLO} or between V_{CCAD} and V_{REFHI} because the self-inductance of the common VIA couples digital noise to the voltage reference pins.

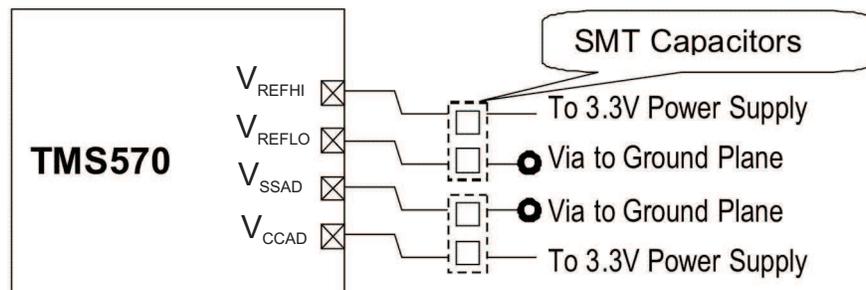


Figure 5. Power and Reference Voltage Layout Strategy

2.3 Input Channel

A typical input stage of the ADC input includes a low-pass filter and an operational amplifier (OP-AMP) as shown in Figure 6. You can combine the low-pass filter and OP-AMP together.



Figure 6. ADC Input Strategy

2.3.1 Anti-aliasing Low-Pass Filter

Usually, the analog input carries all kinds of noise (FM noise, cell phone band noise and other spurious signal). You should have some prior understanding of the nature of the input signals to be measured, for example, the minimum or maximum frequency. Then, a filter can be designed to improve the signal to noise ratio (SNR).

On the other side, the highest ADC sampling rate on TMS570LS31x/21x and RM4 devices is around 1 MSPS. The Nyquist frequency is half the sampling frequency. Any signal or noise beyond the Nyquist frequency can be considered as 'disturbance' to the system and should be filtered before sampling.

To protect the analog input signal integrity, the capacitor and inductor used in the filter must be screened carefully. The capacitance of the capacitor must not change across the voltage, frequency and temperature range (NPO capacitor). The inductance of the inductor must not change across the current, frequency and temperature range either. The change of capacitance or inductance will result in harmonic distortion to the system and degradation of the ENOB.

2.3.2 Op-Amp

Figure 7 shows the equivalent circuit of an ADC input channel for the TMS570LS31x/21x or RM4 device. The ADC loading changes before and after the sample switch closes. To protect the analog input from changes in ADC loading, especially at sampling frequency greater than 100 KSPS, an Op-Amp is recommended. The OP-AMP can provide the following benefits to the system:

- Isolate the analog input and ADC loading
 - High-input impedance
 - Low-output impedance
 - Protects the analog input from changes in ADC loading
- Charge sample and hold networks effectively
- Provides gain, offset and level shifting
- Configure as filters

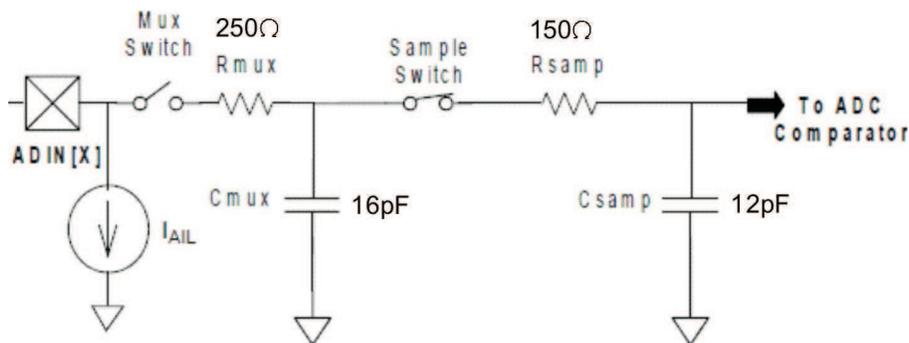


Figure 7. MibADC Input Equivalent Circuit

The OP-AMP is not a must. If the input frequency and sampling frequency is low, or the input signal driving strength is strong, the OP-AMP can be removed. Once the OP-AMP is removed, the circuit looks like Figure 8. Two offsets must be considered in this case [3]:

- Offset caused by charge sharing between C_{ext} and the ADC sampling capacitor.
- Offset caused by re-charging the C_{ext} .

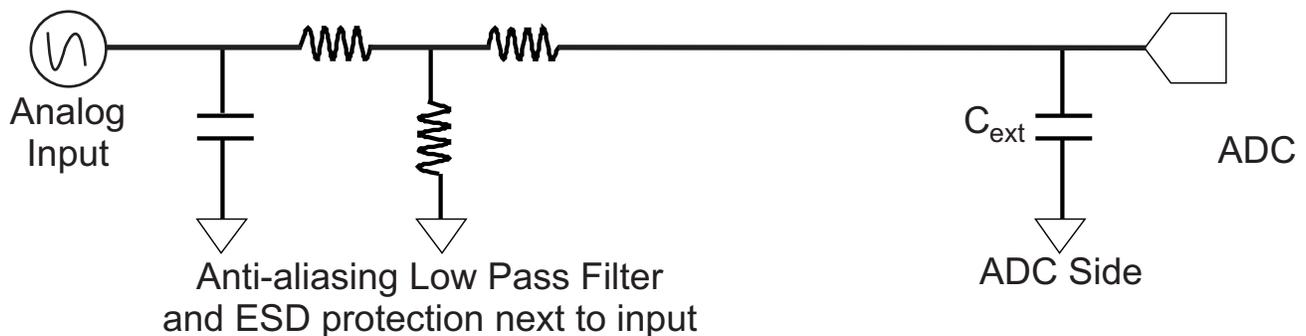


Figure 8. ADC Input Passive Circuit (No OP_AMP)

For more details on how to estimate these offsets and to know if OP-AMP is a must in your system, see the *Hercules Safety MCU Technical Reference Manual* [3]. An alternative way is to run a test on the board:

1. Bypass the Op-Amp.
2. Provide a DC voltage to the analog input.
3. Run 10 ADC conversions with the desired sampling rate and acquisition time.
4. If the 1st conversion is more than 1LSB greater than the other nine conversions, you might need an OP-AMP (takes too long to charge the C_{ext}).
5. Run 10 ADC conversions with the desired sampling rate and twice the acquisition time.
6. If the average value of is more than 1LSB, greater than the average of , you might need an OP-AMP (C_{ext} is not big enough to share charge with the sampling capacitor).
7. If your application tolerates the uncertainty in [Step 4](#) and [Step 6](#), you don't need an OP-AMP.

3 References

1. Hockanson, D. M., J. L. Drewniak, T. H. Hubing, T. P. van Doren, F. Sha, and C. W. Lam, *Quantifying EMI Resulting From Finite Impedance Reference Planes*, IEEE Trans. Electromagn. Compat., vol.39, no.4, pp.286–297, Nov 1997.
2. Henry W. Ott, *Electromagnetic Compatibility Engineering*, Chapter 17 Mixed Signal Layout, John Wiley & Sons, Inc, New Jersey, 2009.
3. [TMS570LS31x/21x Technical Reference Manual](#)
4. [ADC Source Impedance for Hercules™ ARM® Safety MCUs](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2012) to A Revision	Page
• Update was made in Section 1	2

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