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Use of the TMS320C5x Internal Oscillator With External Crystals or Ceramic Resonators

Application Report

1995 Digital Signal Processing Products

Printed in U.S.A., October 1995

SPRA054

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SPRA054
October 1995

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Abstract

This application report provides information regarding crystal and ceramic resonators, their frequency characteristics, a general background on oscillators, and the type of oscillator circuit used on the TMS320C5x. Also covered are design aspects of the ’C5x oscillator including appropriate configuration of the external components, measured parameters for the on-board portion of the circuitry, use of the oscillator with overtone crystals, and general design considerations for choosing the external components for the oscillator. Finally, this report shows some design solutions for common frequencies.

Introduction

The TMS320C5x is one of the Texas Instruments family of high-speed digital signal processors (DSPs). The TMS320C5x is capable of performing operations at a rate of up to 50 million instructions per second (MIPS). The wide variety of digital signal processing applications requires a wide range of clocking frequencies. The TMS320C5x allows considerable flexibility in meeting these clocking requirements.

The TMS320C5x provides several different modes for clock generation and control for use with different application needs. These include:

- External clock input with capability to divide the clock frequency by two
- External clock input to an on-board phase-locked loop (PLL) which can multiply the clock frequency by one, two, three, four, five, or nine
- Internal clock generation from an on-board oscillator with no external clock necessary

The built-in oscillator provides a method for accurate clock generation that requires few external components (a crystal or ceramic resonator and two load capacitors) . This saves board space and reduces system cost.

On the TMS320C5x devices, the on-board oscillator operates in a divide-by-2 mode. In this mode, the frequency of CLKOUT1 (which indicates the actual machine cycles of the processor) is one-half of the oscillator frequency. The TMS320C5x cannot use the on-board oscillator in conjunction with the PLL mode of clock generation.

Recommendations for Oscillator Use

As previously mentioned, the TMS320C5x family of devices provides several clock generation options that can be chosen based on cost, component count, and the required clock frequency for the application. The oscillator clocking option on the TMS320C5x provides a low-cost method of clock generation with as few as three external components (one crystal and two load capacitors) which helps to minimize board space consumed for clock generation. The crystal or ceramic resonator used determines the frequency of operation. This frequency can extend up to 80 MHz with third-overtone crystals.

Using the internal-oscillator option for operation above 80 MHz is not recommended. CMOS-compatible-integrated circuit crystal oscillators are available across a wide frequency range. These can be more expensive than the internal oscillator and usually consume more space on the board. CMOS oscillators also become more expensive with higher operating frequency. A low-cost alternative is a lower frequency CMOS oscillator used in conjunction with the frequency multiplication capability of the on-chip PLL. The multiplication factors available depend on which DSP is being used. For more information, refer to the *TMS320C5x User's Guide* (literature number SPRU056) or the *TMS320C5x, TMS320LC5x Digital Signal Processors Data Sheet* (literature number SPRS030).

Behavior and Operation of Quartz Crystal and Ceramic Resonators

Resonator Theory

All oscillators require resonating components to determine the frequency of oscillation. A resonating component reacts more strongly within a certain frequency range than at other frequencies outside that range. A simple resonator can consist of an inductor and a capacitor. These components resonate or favor the frequency at which their individual reactances cancel each other. Figure 1 shows a simple series-LC resonator.

$Z_L = j\omega L \qquad Z_c = 1/j\omega C \qquad Z_t = Z_L + Z_c = j(\omega L - 1/\omega C)$

Z_t is minimum where $\omega L = 1/\omega C$

$$so \quad \omega s^2 = \frac{1}{LC} \quad \Rightarrow \quad \omega s = \frac{1}{\sqrt{LC}}$$

Figure 1. Series-LC Schematic With Impedance Equations

Consider the impedance of the series combination of these components. The impedance of the inductor $Z_l = j\omega L$, where ω is the angular frequency ($\omega = 2\pi f$), and the impedance of the capacitor $Z_c = 1/j\omega C$. The total impedance of the inductor-capacitor combination is $Z_t = Z_l + Z_c = j(\omega L - 1/\omega C)$. Therefore, the magnitude of the combined impedance of these two components is a minimum at the frequency where $\omega L = 1/\omega C$. This frequency (ω_s) is the resonant frequency and is determined by :

$$\omega s = \frac{1}{\sqrt{LC}}$$

Although oscillators frequently consist of different combinations of inductors and capacitors as resonating elements, the accuracy of the frequency control with these components is limited. Changes in the values of L and C due to tolerance limitations and changes in the environment (such as temperature) strongly affect the frequency of the oscillator. Many applications in digital systems require precise clock timing and need more accurate resonators. Quartz crystal and ceramic resonators can provide a more stable and precise frequency control.

Quartz Crystal and Ceramic Resonators

Quartz crystal and ceramic resonators are resonating components made with materials that have specific piezoelectric properties. Piezoelectric materials deform mechanically in the presence of an electric potential and likewise mechanical stress on the material produces a voltage. This property can be used to make a very stable resonator since the frequency of mechanical vibration is controlled precisely by the size, shape, and material properties of the crystal or ceramic used. In fact, many quartz crystal resonators are so precise that they operate within 10 parts-per-million (ppm) of the intended frequency. The oscillator circuitry built into the TMS320C5x devices is designed for use with a quartz crystal or ceramic resonator as the frequency-controlling element.

Ceramic resonators are similar to quartz crystal resonators in physical structure, but they are made from a polycrystalline ceramic instead of monocrystalline quartz. The production process for the ceramic is

much less expensive than for quartz, reducing the final cost of the resonator. However, the polycrystalline structure of the ceramic vibrates within a wider range of frequency than a quartz crystal does, and consequently, the frequency control is not as precise as quartz. Where quartz crystal resonators can operate within 10 ppm of the intended frequency, ceramic resonators generally operate within 5000 ppm. However, if accuracy greater than 5000 ppm is not necessary, ceramic resonators are a cost-effective alternative. Table 1 shows a comparison of three different types of resonators.

Table 1. Advantages/Disadvantages of Resonator Types

TYPE	RELATIVE PRICE	ADJUSTMENT	FREQUENCY TOLERANCE	LONG-TERM STABILITY
LC Resonator	very low	necessary	±20000 ppm	fair
Ceramic Resonator	low	not necessary	±5000 ppm	excellent
Crystal Resonator	high	not necessary	±10 ppm	excellent

In the remainder of this document, the discussion of the use of the ’C5x oscillator will assume that a quartz crystal is being used as the resonator; however, the information presented applies equally to ceramic resonators unless otherwise specified.

Figure 2 shows a circuit model that is (a) equivalent to a crystal, (b) a graph that illustrates the behavior of the magnitude of the crystal impedance, and (c) a graph that shows the reactance of the crystal with frequency. The three components, Lx, Rx, and Cx, model the electrical behavior related to the mechanical vibration of the crystal. Lx and Cx control the resonant frequency according to the same equation shown in Figure 1. Rx models the mechanical energy loss in the crystal and is related to the power dissipation in the crystal. C_0 is the capacitance of the two electrodes. The dielectric of the quartz physically separates the two electrodes. Together, these components are a reasonably accurate electrical model for the behavior of the crystal. Values for these component models are usually available from the crystal manufacturer.

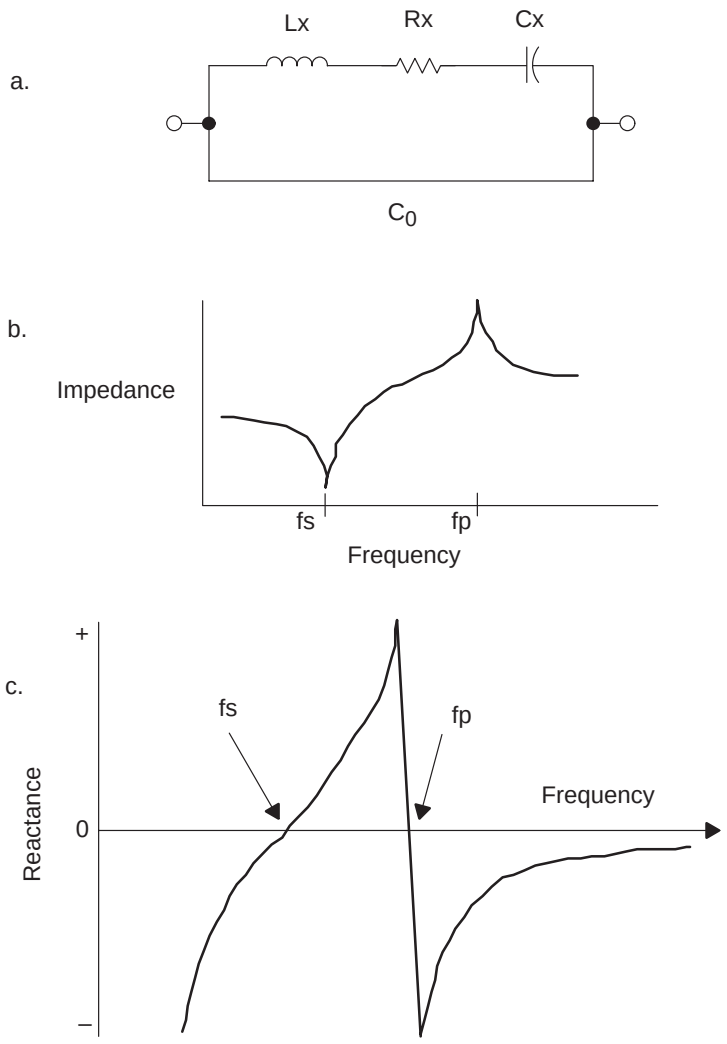

Figure 2. Crystal Equivalent Circuit Model

Like the series LC-resonator, crystals have an impedance minimum at a frequency determined by Lx and Cx. This is the series-resonant frequency (f_s). The presence of C_0 also introduces an impedance maximum at a frequency determined by Lx and C_0. This frequency is the parallel-resonant frequency (f_p). A graph of impedance magnitude that illustrates this behavior is also shown in Figure 2b. The series-resonant frequency corresponds to the natural mechanical vibration frequency of the crystal. The parallel-resonant frequency is basically an electrical measurement phenomenon due to the resonance between Lx and C_0 in the electrical model of the crystal and does not occur naturally. Consequently, all crystal oscillators operate at or near their series-resonant frequency.

The graph in Figure 2b illustrates the behavior of the magnitude of the impedance of the crystal, but the crystal's phase response is also important in oscillator design. Figure 2c shows the reactance of the crystal with frequency. The reactance (and consequently the phase) is zero at the series-resonant frequency (f_s) because at this frequency the reactances of Lx and Cx cancel each other. At this frequency, the total impedance of the crystal is equal to the resistance Rx.

Below f_s, the crystal appears capacitive (negative reactance). Between f_s and f_p, the crystal appears inductive (positive reactance) and above f_p the crystal appears capacitive again. In an oscillator circuit, the crystal always is operated at or slightly above the series-resonant frequency in the inductive region. The capacitance C_0 has little effect on the series-resonant point (f_s), but in combination with the external load on the crystal, the capacitance C_0 affects the parallel-resonant point (f_p). For simplification of the circuit analysis, C_0 is sometimes considered part of the external load on the crystal.

When ordering a crystal, you must tell the manufacturer whether a *series-resonant* or *parallel-resonant* crystal is required. The nature of these terms is slightly different from the serial and parallel-resonant frequency terms previously described. A series-resonant crystal is intended to operate in a circuit with a low-load impedance across its terminals and consequently resonates very close to the series-resonant frequency (f_s). A parallel-resonant crystal is intended to operate in a circuit with a high-impedance load across its terminals and operates at some frequency slightly above f_s where the crystal's reactance is inductive. In this case, the crystal attempts to resonate at the frequency at which its own inductive reactance exactly cancels the capacitive reactance of the combination of C_0 and an external-capacitive load. If supplied with the desired frequency and the external load to which the crystal will be connected, the manufacturer can produce a crystal which meets both of these requirements. The oscillator circuit used on the 'C5x devices requires a parallel-resonant crystal.

Crystal Response to Square-Wave Drive

Figure 3a shows the equivalent circuit model of a crystal driven by a step-function-voltage source in series with a resistive load. In this figure, the capacitance, or C_0, of the crystal model is being ignored because it usually is considered part of the load on the crystal and does not affect strongly the series-resonant frequency. When a step function excites a crystal, the crystal produces damped sinusoidal oscillation at its series-resonant frequency as shown in Figure 3b. The magnitude of the damping on the output waveform is proportional to the magnitude of Rx.

The lowest natural frequency of the crystal is the fundamental frequency. Depending on the design of the crystal, it also can have contributions to its output waveform from odd multiples of the fundamental frequency, or *overtones*. However, if the response at the fundamental frequency is considerably stronger than the response at these overtone frequencies, the contribution of the overtones to the output waveform is negligible.

If the step-function input is changed to a square-wave drive (a periodic set of step functions) at the frequency of the fundamental, the output of the crystal is sinusoidal as shown in Figure 3c. The source of the square-wave provides enough energy to overcome the damping in each cycle. Although a square-wave has a high content of odd overtones, the crystal resonates at its fundamental frequency and strongly attenuates all other frequencies. Consequently, the output of a crystal driven by a square-wave is sinusoidal. If this sinusoidal output is fed back to the input of an appropriately designed amplifier as shown in Figure 3d, sustained oscillation can be generated.

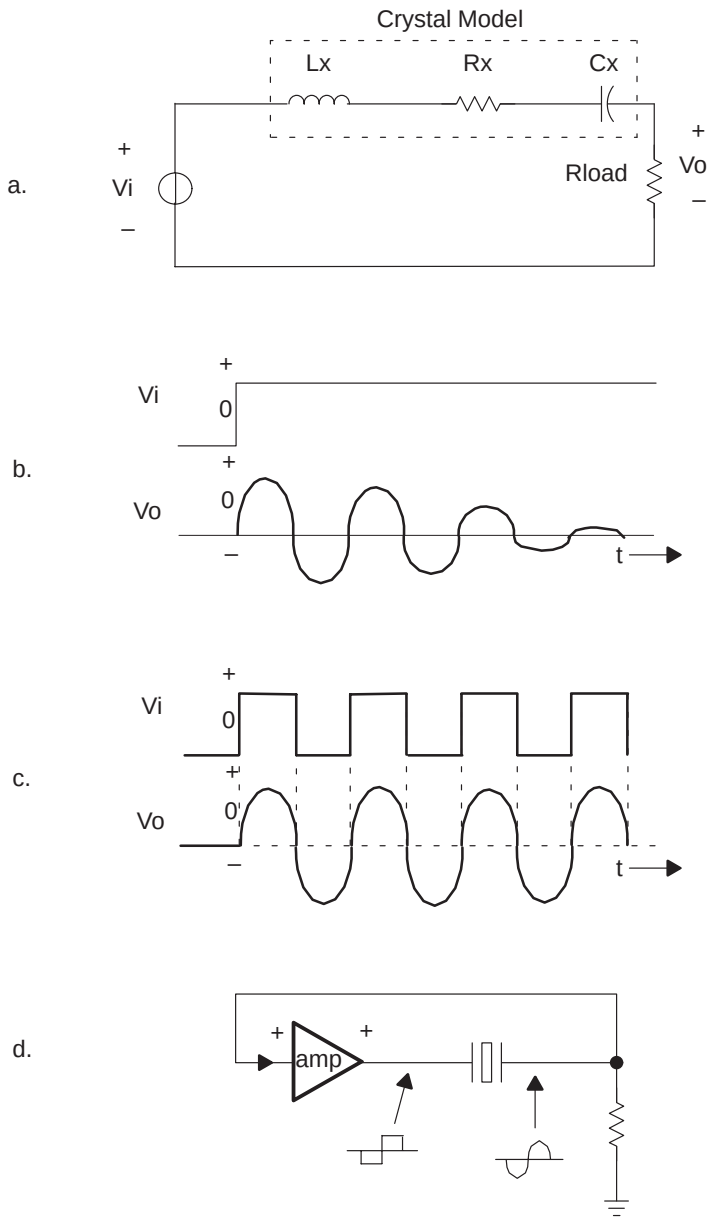

Figure 3. Crystal Response to a Square-Wave Drive

Behavior and Operation of the Pierce Oscillator Circuit

Theory of Oscillator Operation

Figure 4 shows an oscillator circuit in its simplest form: an amplifier and a feedback network. This circuit must meet two requirements to sustain oscillation:

- The circuit must have positive feedback.
- The open loop gain must be greater than one.

In Figure 4, A is the gain of the amplifier and B is the gain of the feedback network. For the circuit to have open-loop gain greater than 1, A x B must be greater than 1. For the circuit to have positive feedback, the phase shift around the loop must be zero degrees (or n360° where n=0, 1, 2, 3, ...). If these conditions are met, the output oscillates at a frequency determined by the frequency selective feedback network and the amplitude increases until it reaches the linearity limitation of the amplifier.

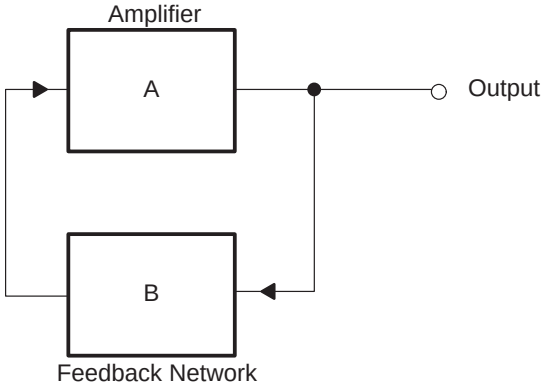

Figure 4. Simple Form of an Oscillator Circuit

There are many possible combinations of amplifiers, crystals, and phase-shifting components (inductors and capacitors) which meet the above specified conditions for oscillation. One of the most common is a circuit based on the Pierce oscillator. Figure 5 shows an ideal version of this circuit. The Pierce oscillator uses an inverting amplifier, a parallel-resonant crystal as a resonator, and two capacitors as phase-shifting elements and load for the crystal. This circuit frequently is used for several reasons:

- It has a large frequency range from approximately 1 kHz to 200 MHz.
- It has high Q (because the load impedances are mostly capacitive and not resistive) and consequently exhibits very good stability.
- It maintains a high output signal while driving the crystal at a low-power level. This is important at higher frequencies where crystals are physically thinner and therefore have lower power-dissipation limits.
- The low-pass RC networks formed by the crystal and load capacitors tend to filter transient noise spikes, giving the circuit good noise immunity.

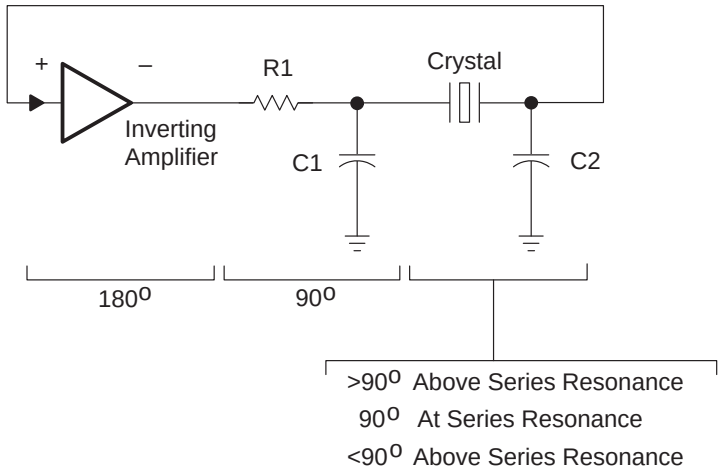

Figure 5. Pierce Circuit: Ideal Operation

The ideal circuit operates in the following manner. An input signal to the amplifier appears at the output phase-shifted by approximately 180°. If it is assumed that at a certain frequency the impedance of C_1 is much greater than R_1, then the phase shift of this RC network introduces another approximate 90° phase shift. At the series-resonant frequency, the crystal appears to be a resistor and forms another RC network with C_2. If the impedance of C_2 is much greater than the series resistance (Rx) of the crystal, this network provides another 90° phase shift. The total phase shift around the loop is now 180° + 90° + 90° = 360°**.** This phase shift meets one of the conditions for oscillation. If the gain of the amplifier is high enough to overcome the losses in the R_1 – C_1 – crystal(Rx) – C_2 network for a total loop gain of greater than 1, then the circuit meets both oscillation conditions and oscillates.

This explanation, however, is unrealistic because it ignores too many aspects of real-world circuit effects. Figure 6 illustrates a more typical example of the circuit behavior. In this case, the inverting amplifier has some phase delay which causes it to produce a phase shift somewhat longer than 180°, depending on the frequency of operation. If oscillation is to occur, the passive components are forced to compensate for this phase difference. The only manner in which the impedance of the load capacitances can change is if the frequency of operation changes, and it does. The frequency of operation tends to move above the series-resonant frequency, lowering the impedance of the load capacitances and raising the impedance of the crystal as it goes from being purely resistive to being both resistive and inductive (see Figure 2c). When the frequency changes such that the loop phase shift once again equals 360°, the circuit oscillates at the higher frequency. For this reason, most Pierce circuits operate 5 – 40 ppm above the series-resonant frequency. This explanation clearly illustrates the circuit's actual behavior and explains why a parallel-resonant crystal always operates slightly above the series-resonant frequency.

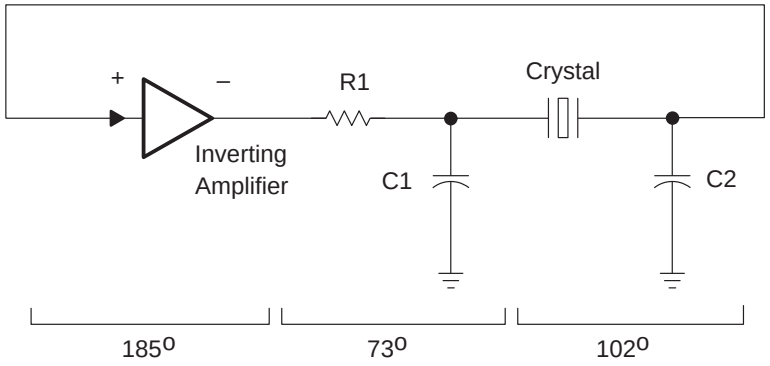

Figure 6. Pierce Circuit: Actual Operation

When a square-wave output is desired (such as for a microprocessor clock source) the Pierce circuit sometimes is implemented in the manner shown in Figure 7. The crystal and load capacitances are in the same configuration as the circuit shown in Figure 6, with the exception that R_1 is replaced with the output impedence of the inverter. In the linear region, the inverter behaves like a linear inverting amplifier. The resistor (R_f) is introduced across the inverter to bias it into the linear region. This is the transition region between the two digital states, as shown in Figure 8. Otherwise, the inverter output would move toward one of its two stable digital states and oscillation would not start because there is no gain in these regions (the output characteristic shown in Figure 8 is flat).

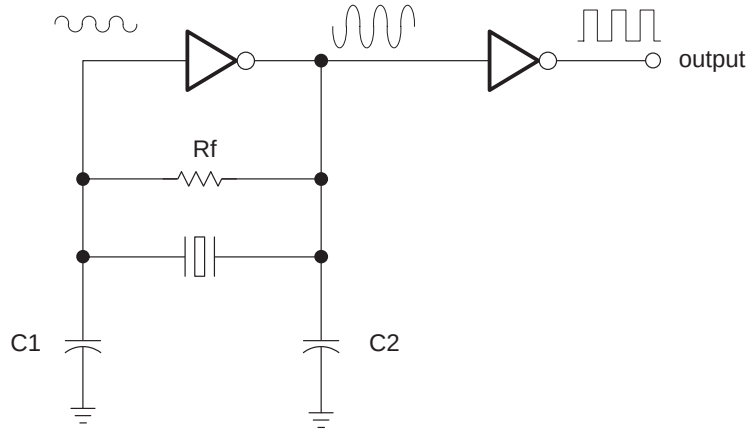

Figure 7. Pierce Circuit

The removal of R_1 from the circuit improves the loop gain and thus improves the likelihood of oscillation. However, removing R_1 also increases the drive level (power dissipation) on the crystal. The power dissipation limit of the crystal should not be exceeded under these conditions (power dissipation issues are discussed in the Drive Level/Power Dissipation section in this report). Otherwise, the circuit operation is identical to that described for Figure 6.

The second inverter is added as a buffer and a waveshaping device. Since the output of the crystal is sinusoidal, the output of the first inverter also is sinusoidal. The second inverter provides a rail-to-rail square-wave output at the oscillation frequency to drive the microprocessor clock.

’C5x Pierce Oscillator Configuration

As mentioned in the introduction, the ’C5x DSPs have a variety of options for clocking the processor:

- Divide-by-2 operation of an externally supplied clock
- Use of an internal phase-lock loop (PLL) to multiply an externally supplied clock by one, two, three, four, five, or nine
- Divide-by-2 operation using the internal oscillator

The PLL and internal oscillator modes are separate. You cannot use these two modes together.

The clock-mode pins are CLKMD1, CLKMD2, and CLKMD3. Table 2 shows the standard clock options available on the ’C50, ’LC50, ’C51, ’LC51, ’C52, ’LC52, ’C53, ’LC53, ’C53S, and ’LC53S. For these devices, CLKIN2 functions as the external-frequency input when using the PLL options. Table 3 shows an expanded set of clock options that are available on the ’LC56, ’C57S, and ’LC57 devices. For these devices, X2/CLKIN functions as the external-frequency input when using the PLL options. For more information on the clock options listed in Table 2 and Table 3, refer to the *TMS320C5x User’s Guide* (Literature Number SPRU056B).

Table 2. Standard Clock Options

CLKMD1	CLKMD2	CLOCK SOURCE
1	0	PLL clock generator option
0	1	Reserved for test purposes
1	1	External/Internal divide-by-2 option with oscillator enabled
0	0	External divide-by-2 option with internal oscillator disabled

Table 3. PLL Clock Options for the ’LC56, ’C57S, and ’LC57

CLKMD1	CLKMD2	CLKMD3	CLOCK SOURCE
0	0	0	PLL multiply-by-3
0	1	0	PLL multiply-by-4
1	0	0	PLL multiply-by-5
1	1	0	PLL multiply-by-9
0	0	1	External divide-by-2 option with internal oscillator disabled
0	1	1	PLL multiply-by-2
1	0	1	PLL multiply-by-1
1	1	1	External/Internal divide-by-2 option with oscillator enabled

To use the ’C5x internal oscillator, CLKMD1 and CLKMD2 (and CLKMD3 for the ’LC56, ’C57S, or ’LC57) must be held high. All other clock modes disable the internal oscillator circuit.

The ’C5x oscillator circuitry (with the exception of the crystal and the load capacitors) is integrated into the processor. Figure 9 shows the ’C5x oscillator circuitry, which is similar to the Pierce IC oscillator shown in Figure 7. On the ’C5x, the waveshaping inverter (I_2) takes its input from the input side of the inverter being used as the amplifier (I_1) rather than from the output as in the Pierce oscillator. This has little affect on the oscillator other than generating the digital complement of the clock that would be generated in the circuit of Figure 7. Also, the feedback resistor in Figure 7 has been integrated into the ’C5x as an active-load transistor-feedback network, so an external-feedback resistor is unnecessary. This feedback network ensures that the inverter I1 is biased in its linear region.

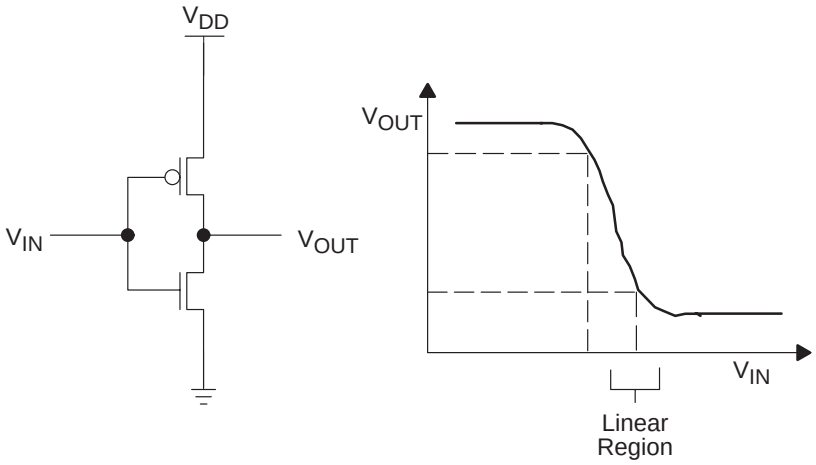

Figure 8. Digital Inverter Circuit and Its Transfer Characteristic

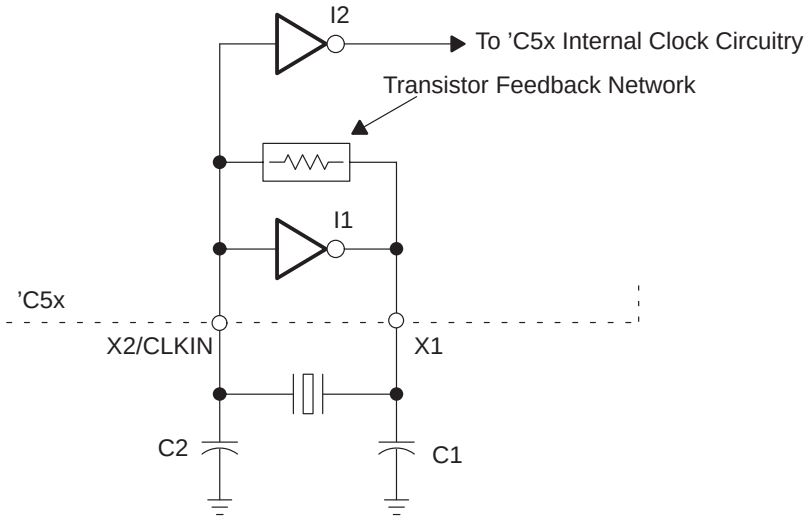

Figure 9. 'C5x Oscillator Circuitry

The inverters in the oscillator circuitry differ from the usual CMOS inverter configuration (shown in Figure 8) in that the p-channel transistor is biased as an active load instead of having the gate connected as the input of the inverter. This difference is part of the biasing scheme, which helps to ensure that the oscillator starts when power is applied. This design causes the rise and fall times to be asymmetrical (for example, the rise time is longer than fall time), but since the oscillator output is divided by 2 before driving the internal-processor circuitry, the duty cycle of the final clock (CLKOUT1) is 50%.

Measured Parameters for the 'C5x Internal Oscillator Circuitry

Various measurements were made on the internal oscillator circuitry on the 'C5x to aid in design and analysis of an oscillator. Measurements were made on multiple devices across several different wafer lots. All of the measurements were made on 80-MHz-rated devices at room temperature with V_{DD} = 5.0 V. Table 4 shows a summary of the measured parameters and is followed by a detailed explanation of how each measurement was taken. These values are actual device limits with no guardbanding. In order to have proper device operation, data sheet values should be used.

Table 4. Measured Oscillator Parameters

PARAMETER	MIN	TYP	MAX	UNITS
Bias point		1.6		V
Gain	5.6			
Input capacitance		25		pF
Output impedance	150		300	ohms
Propagation delay (falling output)		2.3		ns
Propagation delay (rising output)		8.1		ns
High logic level voltage	2.0			V
Low logic level voltage			1.2	V
High logic level pulse width	4.0			ns
Low logic level pulse width	4.0			ns

The bias point of the inverter within its linear region is determined by the internal transistor feedback network (of Figure 9). At V_{DD} = 5.0 V, the bias point at the input of the ’C5x internal inverter (I_1) is 1.6 V. This is the voltage around which the oscillation will occur when the circuit is operating normally.

Gain of the internal inverter was measured by ac coupling a low-level input signal to pin X2/CLKIN and measuring the output level at pin X1. The input signal was maintained at a level low enough that the output signal swing was within the linear region of the inverter. The frequency of the input signal was 500 kHz. The lowest voltage gain measured was 5.6.

Input capacitance at pin X2/CLKIN was measured by applying a voltage step input signal to the pin through a 10-kΩ resistor. The input capacitance was calculated from the measured time constant at the input. The capacitance of the setup alone (application board and test probe only, no ’C5x in the socket) showed 11 pF. The capacitance with the ’C5x installed showed 36 pF, so the ’C5x input capacitance is 36 – 11 = 25 pF. There was no measurable deviation of this parameter among the parts tested.

Output impedance of the inverter was measured by comparing the unloaded output voltage to the loaded output voltage and calculating the output impedance. The load resistance of 200 Ω was ac coupled to pin X1 through a 0.1 µF capacitor. The frequency of the input signal was 500 kHz. The coupling capacitor at this frequency represents approximately 0.3 Ω. The calculated output impedance values varied from 150 –300 Ω.

Propagation delay of the inverter was measured with a 1 MHz square-wave input. Delay was measured at the 50% point of the voltage transition. The rising input to falling output propagation delay averaged 2.3 ns. The falling input to rising output propagation delay averaged 8.1 ns. This increased time for the output rise time is expected due to the p-channel transistor in the inverter being designed as an active load. There was little measurable deviation of this parameter among the parts tested.

Computer circuit simulations yielded similar values for these parameters.

These measured parameters are related to the ’C5x internal inverter I_1, which drives the oscillator. Also relevant is the ’C5x clock circuitry (including I_2) which monitors the input of the inverter I_1 (see Figure 9) and generates CLKOUT1 based on that signal. Measurements were made to determine the minimum signal required at X2/CLKIN for the ’C5x internal clock circuitry to respond properly. These measurements can be used to determine the worst-case input conditions at X2/CLKIN that still produce a system clock and response at CLKOUT1.

Minimum high logic-level voltage input was measured by applying 0 –5-V square-wave at X2/CLKIN and monitoring pin CLKOUT1 as the high logic-level voltage was decreased (see Figure 10). The average minimum value at which CLKOUT1 would still respond properly was 2.0 V.

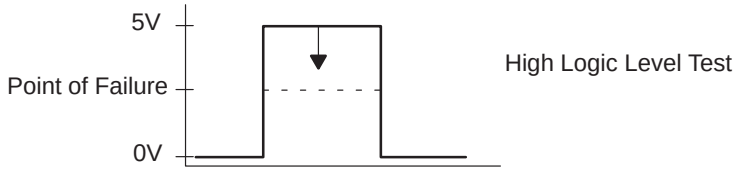

Figure 10. Minimum High Logic Level Voltage Input Signal

Maximum low logic-level voltage input was measured by applying 0 –5-V square-wave at X2/CLKIN and monitoring CLKOUT1 as the low logic-level voltage was increased (see Figure 11). The average maximum value at which CLKOUT1 would still respond properly was 1.2 V.

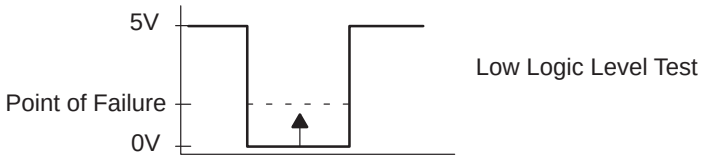

Figure 11. Maximum Low Logic Level Voltage Input Signal

Minimum high logic-level pulse width input was measured by applying 0 –5-V input pulse at X2/CLKIN on an 80 MHz ’C5x device and monitoring CLKOUT1 as the pulse width was decreased. The pulse width was measured as the time between transitions across the 2-volt level (see Figure 12). The average minimum pulse width was 4.0. ns.

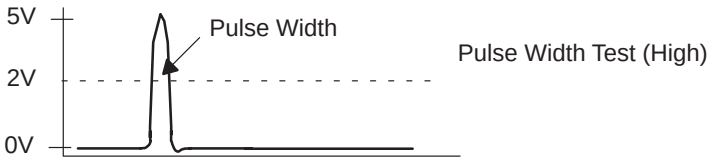

Figure 12. Minimum High Logic Level Pulse Width Input Signal

Minimum low logic-level pulse width input was measured by applying 0 –5-V input pulse X2/CLKIN on an 80 MHz ’C5x and monitoring CLKOUT1 as the pulse width was decreased. The pulse width was measured as the time between transitions across the 2-V level (see Figure 13). The average minimum pulse width at which CLKOUT1 would still respond properly was 4.0 ns.

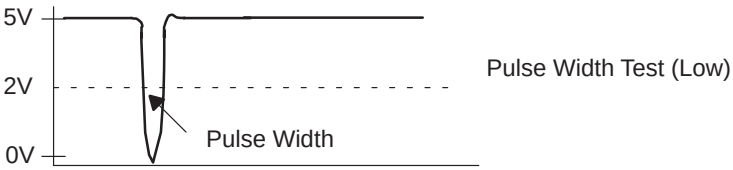

Figure 13. Minimum Low Logic Level Pulse Width Input Signal

These measurements determine the minimum requirements for the input signal at X2/CLKIN. This is detailed in Figure 14. The first trace represents the input signal at X2/CLKIN. The second trace shows the

response of the output of internal inverter (I2) (Figure 9), and the third trace shows the response of CLKOUT1. CLKOUT1 was found to behave reliably, if the following conditions were met:

- X2/CLKIN input positive swing must exceed 2.0 V for at least 4.0 ns.
- X2/CLKIN input negative swing must fall below 1.2 V for at least 4.0 ns.

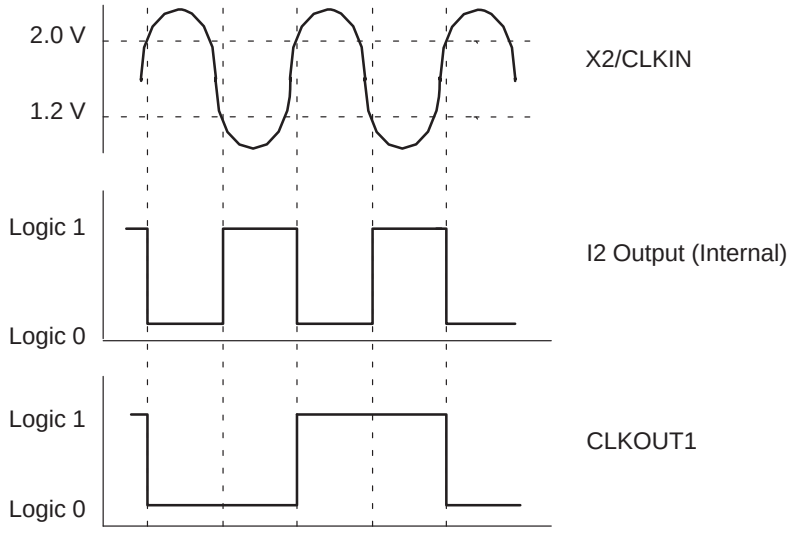

Figure 14. Behavior of Pin CLKOUT1 Relative to Input Signal at Pin X2/CLKIN

Although ’C5x devices are produced both in 5-V and 3.3-V V_{DD} compatible processes, some 3.3-V V_{DD} devices are actually 5-V processed devices that are operated at 3.3-V. Oscillator operation is not supported on the 5-V processed 3.3-V devices due to threshold voltage differences. Therefore, if oscillator operation at a 3.3-V V_{DD} level is required, 3.3-V processed devices must be used. To determine the fabrication process for specific ’C5x devices, contact Texas Instruments directly.

Overtone Operation of the Oscillator

Although crystals are usually considered to vibrate at only one frequency, they also resonate at odd multiples, or overtones, of the series-resonant frequency. The series-resonant frequency is the fundamental frequency of the crystal, and the odd overtones are odd multiples of the fundamental frequency (for example: 3×, 5×, 7×, ...). For low frequencies, it is common to operate crystals at their fundamental frequency. For higher frequencies, the crystal is made thinner. The thinner the crystal is, the more fragile and expensive it becomes. Thinner crystals also have a low-power dissipation limit and damage easily when overdriven.

Most fundamental mode crystals are made to operate at frequencies of 40 MHz or less. To generate frequencies higher than 40 MHz, it is common to use overtone crystals. Overtone crystals have been optimized for operation at an overtone frequency with the fundamental frequency attenuated. Figure 15 illustrates the impedance of a crystal with respect to frequency. The strongest change in impedance is at the fundamental frequency, but there is also a response at the third and fifth overtones. If a crystal with the properties in Figure 15 is used in a Pierce circuit, it oscillates at the fundamental frequency. However, if the fundamental frequency is attenuated, the crystal circuit oscillates at the next higher odd overtone, in this case, the third overtone. High-frequency operation is achieved by using an overtone crystal and attenuating the fundamental frequency.

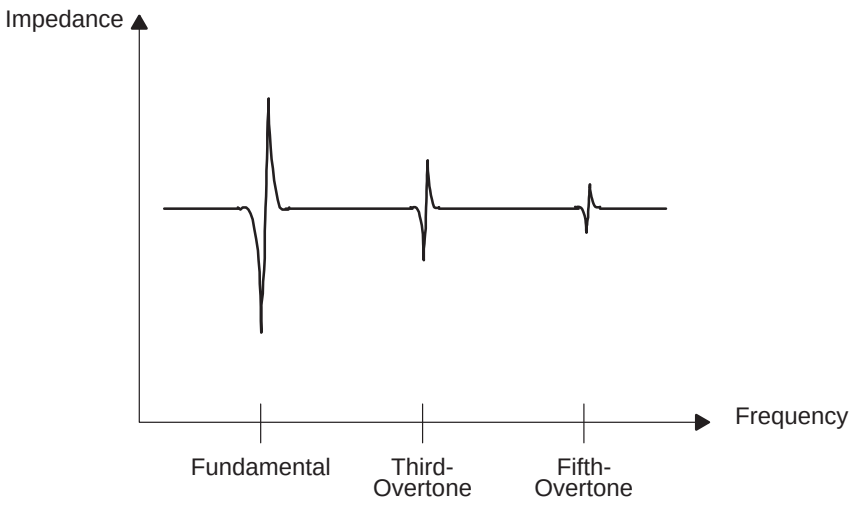

Figure 15. Impedance Characteristics of a Crystal

For the Pierce circuit used on the ’C5x, this attenuation of the fundamental frequency can be achieved by capacitively coupling an inductor (L_1) in parallel with the load capacitor (C_1), as shown in Figure 16. The value of L_1 is chosen to resonate with C_1 at some intermediate frequency between the frequency of the desired overtone and the next lower odd overtone. At the desired overtone frequency, the impedance of L_1 is high enough compared to C_1 that L_1 can be neglected and the network of C_1 and the inverter’s output impedance provides the near-90° phase lag desired. Since the phase conditions are met, the circuit oscillates at this frequency. At all lower overtones, L_1 is a lower impedance than C_1 and will cause a 90° phase lead instead of phase lag. At any of these lower frequencies, the total phase shift around the feedback loop is 180°, not 360°, which is negative feedback, and stabilizes the circuit and prevents oscillation. L_1 is coupled with a 0.1 µF capacitor, which prevents the inductor from altering the dc bias of the inverter while causing negligible additional impedance at the oscillation frequency.

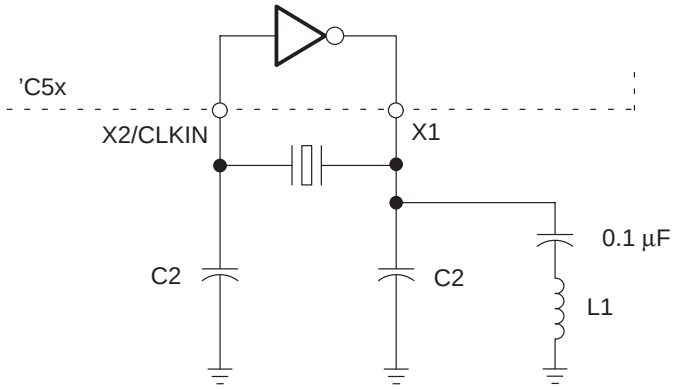

Figure 16. Oscillator Circuit for Overtone Crystal Operation

As an example, assume a 60 MHz third-overtone crystal is used with 10 pF load capacitors. The fundamental for this crystal will be at 60/3 = 20 MHz. L_1 should be chosen so it will resonate with C_1 at some frequency between 20 MHz and 60 MHz. If you choose the frequency halfway in between, 40 MHz, the value of L_1 can be calculated as follows:

$$L_1 = 1/(\omega^2 C_1) = 1/(4\pi^2 f^2 C_1) = 1/(4\pi^2\ (40\times10^2)^2\ (10\times10^{-12})) = 1.58\ \mu H$$

Since the value of this inductance is not critical, the closest conveniently available inductor is used as long as the resonant frequency of L_1–C_1 falls between the desired overtone and the next lower overtone.

A variety of crystals were evaluated in this circuit. Although, at higher frequencies, fifth-overtone crystals are more commonly available, they are not recommended for this circuit. The available gain from the internal inverting amplifier limits this configuration to third-overtone crystals. Several third-overtone crystal solutions for this circuit were evaluated up to 80 MHz and are listed at the end of this report.

Design Considerations

This section discusses some of the aspects of the design of the oscillator and their effects on its operation.

Crystal Series Resistance (Rx)

The series resistance of the crystal has a strong effect on the design of the oscillator, primarily in loop gain. Rx limits the crystal's minimum impedance value (seen at series resonance). Since the impedances of Lx and Cx cancel each other at this frequency, the impedance of the crystal is entirely due to Rx. The voltage divider formed by the crystal and C_2 influences the loop gain. As the impedance of the crystal becomes larger, the gain loss due to the voltage divider becomes greater. Low-loop gain causes the oscillator to take longer to start up and can prevent oscillation if the overall loop gain falls below one. Higher crystal series resistance also reduces the overall oscillator circuit Q, resulting in poorer frequency stability. For these reasons, it is desirable to use the lowest Rx possible. Crystals with series resistance of 40 Ω or lower are recommended.

Load Capacitors

In the Pierce circuit used on the 'C5x, the load capacitors have a strong effect on how far above the series-resonant frequency the crystal will oscillate. The crystal's shunt-terminal capacitance, C_0, can be considered part of the crystal's external-load capacitance as far as the frequency controlling elements Cx and Lx are concerned. A parallel-resonance oscillator circuit operates at the frequency where the reactances of the crystal (Cx and Lx) cancel the reactances from the load (C_0, C_1, C_2). Consequently, changes in the external-load capacitance cause the oscillator to change frequency to compensate for the phase change. The following formula gives an approximate value for the frequency shift from the series-resonant frequency:

$$\Delta f \approx \frac{f_s C_O}{2r(C_O + C_L)} \quad where\ r = \frac{C_O}{C_x} \quad and\ C_L = C_1 + C_2$$

The derivative of this formula, as shown below is useful for determining frequency variance due to changes in the load capacitance. This can be applied to find the frequency range implied by load capacitance with a given tolerance. Also, if there is a need to adjust the operating frequency, use this formula to determine the appropriate value of a variable load capacitor.

$$\Delta f_r \approx \frac{\Delta C_L f_s C_O}{2r(C_O + C_L)^2}$$

Crystal manufacturers often accommodate requests for specific values for load capacitance to be used with their crystals, but values of 20 pF and 30 pF are commonly available. These load capacitance values represent C1+C2, so for a crystal designed for load capacitance of 20 pF, $C_1 = C_2 = 10$ pF would be used. Capacitance values higher than 30 pF increase attenuation, lowering the overall loop gain. Capacitance values this high may cause the circuit to stop oscillating. Load capacitance of 20-30 pF is recommended for high-frequency crystals. Ceramic resonators usually require higher load capacitance than

high-frequency crystals (refer to the manufacturer's recommendations). Load capacitance values are included in Table 5 on page 22 of this report.

Loop Gain

Overall loop gain must be greater than 1 for oscillation to be sustained. Otherwise, if this condition is met, loop gain primarily affects the startup time of the oscillator. Higher loop gain causes the oscillation amplitude to increase rapidly, therefore reducing the time necessary for the oscillator to reach its steady state.

The minimum gain measured for the 'C5x inverter was 5.6. To maintain an overall loop gain of 1, the external component network of C1-crystal-C2 must not introduce a loss of greater than 5.6. For this reason, the values of the load capacitance and crystal-series resistance have a strong effect on whether the circuit oscillates.

Drive Level/Power Dissipation

Another parameter specified when ordering a crystal is drive level or power dissipation. Higher frequency crystals generally have lower power dissipation ratings because the crystal is physically thinner and can be damaged by excessive voltages. Power dissipation also affects frequency stability because the crystal's frequency of operation is dependent on temperature. Excessive power dissipation causes crystal heating and frequency drift results.

There is not a convenient way to measure the power dissipation in the crystal. The series resistance (Rx) is the only power-dissipating component in the crystal. Measuring the external voltage on the crystal includes the voltage across Lx and Cx. Therefore, the power dissipation in Rx cannot be easily calculated directly from the voltage on the crystal. It is necessary to measure the current through the crystal using a current probe or to indirectly measure the current by measuring the voltage across a small resistor in series with the crystal. You may then calculate the power by using I^2R.

Once the drive level is known, if it is necessary to limit the drive level to the crystal, one of the simplest ways to do so is shown in Figure 17. A resistor (Rd) is added in series between X1 and the external components. This resistor drops part of the voltage driven by the 'C5x, and consequently lowers the drive voltage on the crystal. The disadvantage to this method is that the voltage drop reduces the overall loop gain of the oscillator circuit. So, the value of Rd should be large enough to bring the power dissipation of the crystal within the manufacturer's specification, but Rd should not be so large that the loop gain drops below 1 or the circuit will no longer oscillate. Using crystals with minimum power dissipation ratings of 1 mW is recommended.

The oscillator circuit solutions at the end of this report, when operated without Rd, yielded crystal-power dissipation measurements near 1 mW. Differences in circuit and crystal parameters may cause the power dissipation in the crystal to slightly exceed 1 mW. If crystal-power dissipation is critical, adding a resistor (Rd) with a value of 33 Ω to limit the crystal-power dissipation, or obtaining crystals with power dissipation ratings higher than 1 mW, is recommended. When operated with Rd = 33 Ω, each of the circuit solutions shown in Table 5 exhibited less than 1 mW crystal power dissipation.

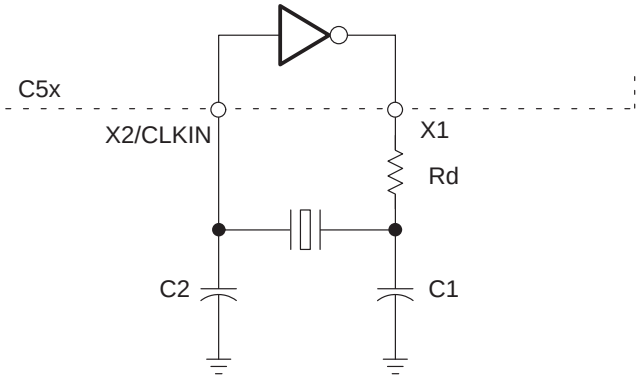

Figure 17. Addition of Rd to Limit Drive Level of the Crystal

Startup Time

Figure 18 shows that when the oscillator starts, low-amplitude oscillations gradually build until the linearity limit of the amplifier is reached. You will experience this startup time at power-up. Maximizing loop gain will minimize the startup time for the oscillator.

Startup time is dependent on the external components used, but generally requires at least 100 ms after power-up for the oscillator to stabilize. For this reason, a reset delay of 150-200 ms is recommended following power-up.

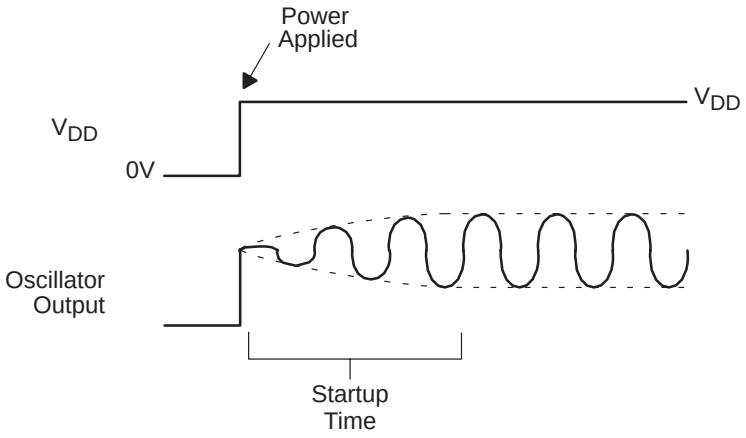

Figure 18. Oscillator Startup

Frequency-Temperature Characteristics of Crystals

The actual operating frequency of a crystal is dependent on temperature. The extent to which frequency changes with respect to temperature strongly relates to the cut of the crystal. AT- and SC-cut crystals behave differently from DT-, CT-, and BT-cut crystals. Even slight changes in the cut angle of the crystal can strongly affect the frequency-temperature characteristics.

Most crystals available in the frequency range of interest for DSPs are AT-cut crystals. The frequency-temperature characteristic for AT-cut crystals is a third-order function, similar to that shown in Figure 19. This graph shows the general temperature-frequency behavior of AT-cut crystals. Similar information is readily available from crystal manufacturers.

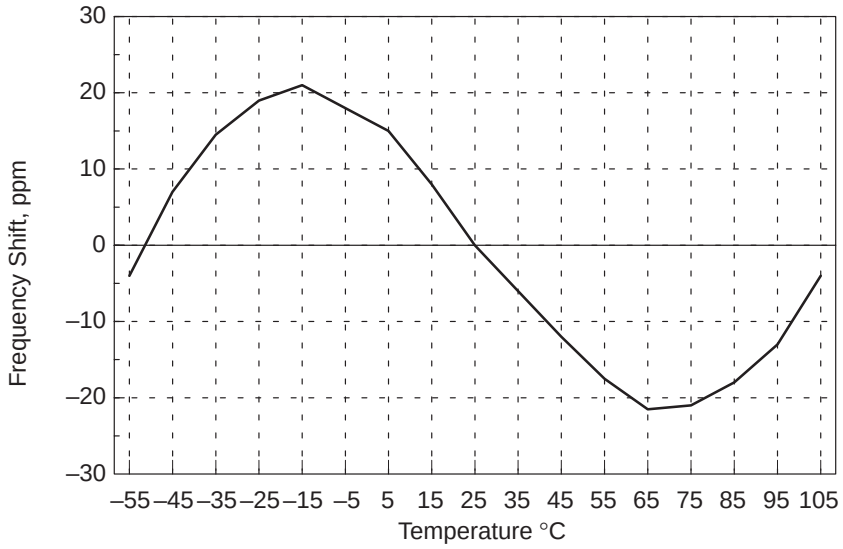

Figure 19. Example Frequency-Temperature Characteristic of AT-Cut Crystals

Crystal Aging

Crystal aging is the gradual change in the frequency of a crystal over time. This change occurs due to stress relief between the mounting structure and the electrodes and absorption (or de-absorption) of contaminants from the resonator surfaces. Changes in temperature accelerate both of these mechanisms. The major mechanism for aging in crystals above 1 MHz is mass transfer to and from the resonator surfaces. The most rapid aging occurs early in the crystal's lifetime, and then aging tends to stabilize. For example, a crystal that ages 10 – 60 ppm in a year may experience 5 ppm of that aging in the first month. Crystals are available (at additional expense) that have very low aging rates, due to cleaner fabrication and packaging processes. These crystals may have aging characteristics as low as 1×10^{-8} ppm per year. Complete information on aging characteristics is available from crystal manufacturers.

Oscillator Solutions for Common Frequencies

Oscillator Circuit Configurations and Component Requirements

This section provides several oscillator solutions for common frequencies of operation of Texas Instruments DSPs. Also listed are several manufacturers that supply crystals and ceramic resonators. The solutions were built and tested with samples from these manufacturers. These circuits were tested at room temperature and verified to operate correctly within the recommended range of V_{DD} (4.75 - 5.25 V).

The following circuits were used for ceramic resonators and fundamental-mode crystal resonators. The circuit in Figure 20 was used for all circuits marked *fundamental* mode in Table 5. The circuit of Figure 21 was used for all circuits marked *third-overtone* mode in Table 5. Crystals used in these circuits should be parallel-resonant with a series resistance of 40 Ω or less and should have a power dissipation rating of 1 mW or greater.

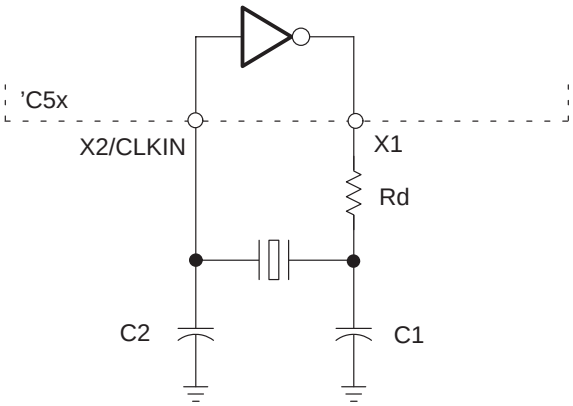

Figure 20. Fundamental-Mode Circuit

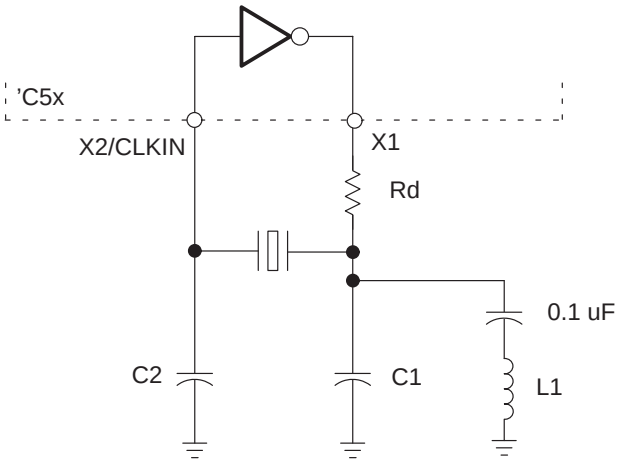

Figure 21. Third-Overtone Circuit

Resonators Tested and Associated Component Configurations

Table 5 lists the oscillator solutions by frequency:

Table 5. Oscillator Solutions by Frequency

FREQUENCY	MODE	TYPE	SUPPLIER	PART NUMBER	C_1, C_2	Rd	L_1
4 MHz	Fundamental	Ceramic	Murata	CSA4.00MG040	100 pF	100	–
4 MHz	Fundamental	Ceramic	Murata	CST4.00MGW040	†	100	–
8 MHz	Fundamental	Ceramic	Murata	CSA8.00MTZ040	100 pF	100	–
8 MHz	Fundamental	Ceramic	Murata	CST8.00MTW040	†	100	–
12 MHz	Fundamental	Ceramic	Murata	CSA12.0MTZ040	100 pF	100	–
12 MHz	Fundamental	Ceramic	Murata	CST12.0MTW040	†	100	–
25 MHz	Fundamental	Ceramic	Murata	CSA25.00MXZ040	30 pF	0	–
25 MHz	Fundamental	Ceramic	Murata	CST25.00MXZ0H5	†	0	–
40 MHz	Fundamental	Crystal	SaRonix	HFX series crystals	10 pF	0/33‡	–
40 MHz	Third-overtone	Crystal	Anderson	011-668-04663	10 pF	0/33‡	3.3 µH
50 MHz	Fundamental	Crystal	SaRonix	HFX series crystals	10 pF	0/33‡	–
50 MHz	Third-overtone	Crystal	SaRonix	SRX5223	10 pF	0/33‡	3.3 µH
57 MHz	Third-overtone	Crystal	Anderson	011-668-04664	10 pF	0/33‡	3.3 µH
60 MHz	Third-overtone	Crystal	Anderson	011-668-04725	10 pF	0/33‡	3.3 µH
80 MHz	Third-overtone	Crystal	Anderson	011-668-04724	10 pF	0/33‡	0.56 µH

† This resonator has built-in load capacitors, eliminating the need for C_1 and C_2.

‡ When these circuits are operated without Rd, they yield crystal power dissipation measurements near 1 mW. Differences in circuit and crystal parameters can cause the power dissipation in the crystal to slightly exceed 1 mW. If crystal power dissipation is critical, it is recommended to add Rd of 33 Ω to limit the crystal power dissipation, or obtain crystals with power dissipation ratings higher than 1 mW. When operated with Rd = 33 Ω, each of the circuits shown exhibited less than 1 mW crystal power dissipation.

Resonator Manufacturers

Crystals:

SaRonix
151 Laura Lane
Palo Alto, CA 94303

Telephone: 800-227-8974
415-856-6900
Fax: 415-856-4732

Anderson Electronics
Scotch Valley Rd.
Hollidaysburg, PA 16648

Telephone: 814-695-4428
Fax: 814-696-0403

Ceramic resonators:

Murata Electronics North America
2200 Lake Park Drive
Smyrna, Georgia 30080

Telephone: 800-831-9172
Fax: 404-436-3030

Summary

A wide range of clocking frequencies is required for the varied DSP applications. The ’C5x provides several different modes for clock generation. These are:

- External clock input with capability to divide the clock frequency by two
- External clock input to an on-board phase-lock loop (PLL) which can multiply the clock frequency by one, two, three, four, five, or nine
- Internal clock generation from an on-board oscillator with no external clock necessary

The PLL and internal oscillator modes are separate. They cannot be used in conjunction with one another.

For operation above 80 MHz, using an external IC crystal oscillator is recommended. These oscillators are available from several different manufacturers listed in this report.

The Pierce oscillator circuitry built into the ’C5x is designed for use with a quartz crystal or ceramic resonator as the frequency controlling element. Crystal resonators are more accurate but more expensive than ceramic resonators.

Most fundamental-mode crystals are made to operate at frequencies of 40 MHz or less. Overtone crystals usually are used to generate frequencies higher than 40 MHz.

There are several elements to consider when designing a method for clock generation. These include:

- The series resistance of the crystal
- The load capacitors in the on–board oscillator circuitry
- The overall loop gain
- The drive level or power dissipation
- The startup time
- The frequency-temperature characteristics of the crystal
- Crystal aging

References

1) *Crystal Oscillator Circuits.* Robert J. Matthys. Wiley, 1983.

2) *Electronic Engineers Handbook, Third Edition.* Donald G. Finh and Donald Cristiansen, editors. McGraw-Hill, 1989.

3) *TMS320C5x User's Guide* (literature number SPRU056). Texas Instruments Incorporated, 1993.