TCM320AC3x/4x
Voice-Band Audio Processors

Application Report

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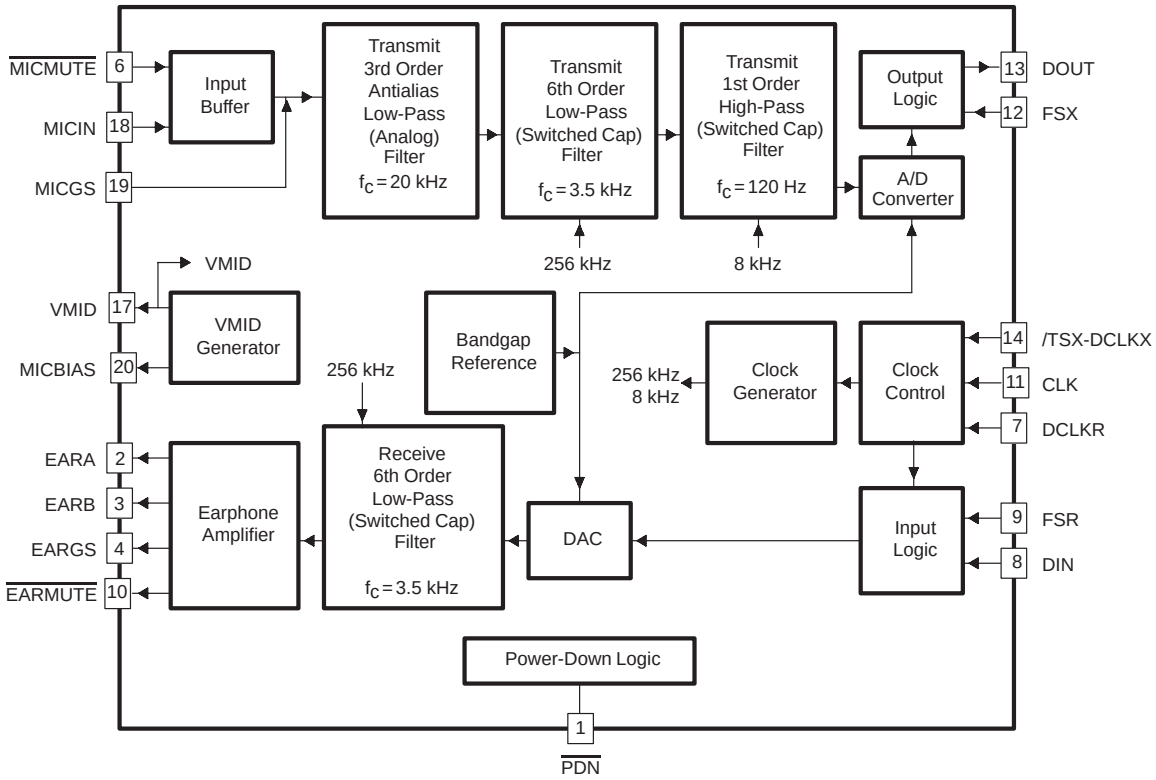
Introduction

The voice-band audio processor (VBAP) family of devices is a line of highly specialized single-supply voice codecs specifically designed for use in battery-powered personal communications systems. The VBAP uses the TI LinEPICZ1 1-µm semiconductor process, which results in very low power consumption. In addition, a patented TI process is used to maintain extremely low noise specifications. The VBAP device serves as an interface between a voice and a DSP and incorporates three major functions: transmit encoding (A/D conversion), receive decoding (D/A conversion), and transmit and receive filtering. The VBAP family supports a serial data connection in either 8-bit companded µ-Law or A-law mode, and a pin-selectable 13-bit linear conversion mode. The VBAP utilizes sophisticated switched capacitor filters to provide filtering that is compatible with most personal communication specifications, including the EIA/TIA/IS-54 for U.S. digital cellular telephones and the CCITT G.711 and G.712 µ-law and A-law filtering requirements. The VBAP also provides direct microphone and speaker interface.

VBAP devices are available in 20-pin N (dual in-line plastic) and DW (surface mount) packages, as well as soon-to-be-introduced QFP (quad flat pack <20-mm) packages.

Figure 1. VBAP Functional Block Diagram



NOTE: f_C is the –3-dB cutoff frequency.

Principles of Operation

To minimize crosstalk, the VBAP design utilizes independent converters, filters, and voltage references for the transmit and receive channels. Figure 1 shows a typical VBAP functional diagram with these features.

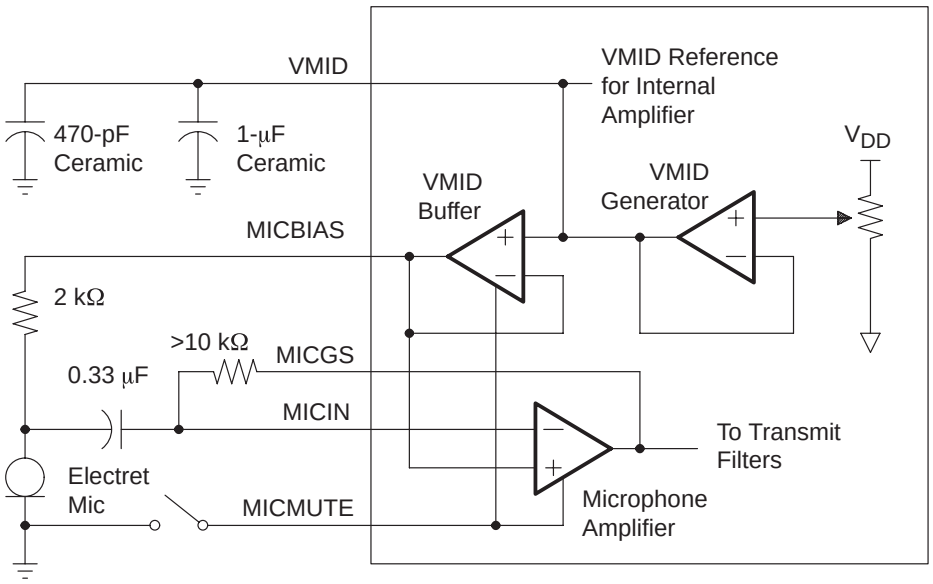
Transmit Channel

Microphone interface

A reference voltage equal to $V_{DD}/2$, called VMID, is used to develop the midlevel virtual ground for all amplifier circuits and the microphone bias circuits. Any power supply noise on VMID would normally be detected on the output of the VBAP; therefore, VMID is brought to an external pin so that the voltage can be filtered by using an external capacitor. The optimum capacitor combination is a 1-μF ceramic type in parallel with a 470-pF ceramic chip cap. A reference voltage at the MICBIAS pin can be used to supply bias current for the microphone. Because MICBIAS is also used internally to bias the microphone amplifier, the common-mode rejection results in a quiet bias voltage. For this reason, it is recommended that you use MICBIAS to bias only an electret microphone, as shown in Figure 2.

The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. This is accomplished by changing the value of the series capacitor and feedback resistor of the (uncommitted) microphone-inverting amplifier. While the configuration shown in Figure 2 will suit most applications, the steady-state impedance of the electret microphone and the 2-kΩ microphone bias resistor can be converted to a Thevenin's equivalent voltage source with a series impedance to calculate the microphone amplifier gain. A resistor can also be added in series with the 0.33-μF capacitor at the amplifier input to decrease the amplifier gain. Note that the 0.33-μF capacitor, along with the 2-kΩ resistor, yields a high-pass filter with a –3-dB cutoff of 240 Hz and –0.6 dB cutoff at 300 Hz, which is acceptable for voice-band communications.

Figure 2. VBAP Microphone Connection



Microphone Mute

The microphone mute function disables the microphone amplifier, and the input to the transmit filters is placed in a high-impedance state. With $\overline{\text{MICMUTE}}$ enabled, the output of the microphone amplifier is more than 80 dB down from the signal on MICIN (microphone input), and the digital circuitry will transmit zero code on DOUT. In addition, the VMID buffer is disabled, and the MICBIAS output is zero.

Transmit Filters

The amplified signal is passed through antialiasing and band-pass filters. The antialiasing filter is an analog (continuous time) first-order low-pass filter with a cutoff of 20 kHz and is used to attenuate any modulation components above half the sampling frequency *of the next stage* to avoid aliasing artifacts (Nyquist sampling theorem). The next stage is a switched capacitor filter with a sampling rate of 256 kHz, so the antialiasing filter provides a greater than 35-dB attenuation at half that sampling frequency, or 128 kHz.

The band-pass filters are composed of oversampled switched capacitor filters to avoid the effects of aliasing. The first band-pass filter is a sixth-order low-pass filter with a cutoff of 3.5 kHz, and the second is a first-order high-pass filter with a cutoff of 100 Hz, sampled at 256 kHz and 8 kHz, correspondingly. *The effective 0-dB bandpass of these filters is from 300 Hz to 3.4 kHz.* Because of the oversampling and because the clocks used by both these filters are synchronous, antialiasing products can be easily controlled and virtually eliminated.

Encoding (A/D Conversion)

The encoded data word structure is available in two formats: companded and linear conversion. The formats are pin selectable. When the device is in the companded mode, the analog signal is sent to the transmit filters and then input to a compressing analog-to-digital converter (COADC). The analog signal is encoded into 8-bit digital representation via the μ-Law and A-Law encoding scheme according to CCITT G.711; this equates to 12 bits of resolution for low-amplitude signals. When the linear conversion mode is selected, 13 bits of data are sent, padded with 0s to provide a 16-bit word. Both companded and linear conversion modes use 2s-complement words.

Data can be transmitted in either a fixed or variable data rate mode. See *Fixed and Variable Data Rate Modes* on page 6 for more detail.

The encoder internally samples the output of the transmit filter *at the middle of the frame* and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion (on a switched capacitor array), also starting in the *second half of the frame*. To minimize the delay across the VBAP, the actual conversion process does not complete until just *before* the next frame. Digital data representing the sample is then transmitted at the start of the *next* frame. The transmit data is output on the DOUT pin. Transmit data is clocked out on consecutive *positive* transitions of the transmit data clock, which is CLK in the fixed-data-rate mode and DCLKR in the variable-date-rate mode.

The master-clock-to-frame-sync ratio is critical and cannot be violated. Refer to *Timing and Clocking* on page 5 for more detail.

For both companded and linear modes, the sign bit is transmitted first, followed by the MSB, with the LSB transmitted last.

Since the A/D conversion rate is the master clock, and the band-pass switched capacitor filter clocks are integer submultiples of the master clock, unwanted aliasing products are prevented.

Transmit Auto Zero

The auto zero circuit corrects for any DC offset on the input signal to the encoder by using a sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the

input to the encoder. This acts as a form of feedback to track and correct for changing DC offsets. The auto zero circuitry is implemented after the high-pass transmit filter so that it will not mistakenly track low-frequency audio signals. The response time of the auto zero circuitry is about five frames from device power-up, or from standby to active.

Noise-Reduction Algorithm

The VBAP transmit circuitry incorporates patented TI circuits to reduce transmit noise to extremely low levels. These circuits reduce the transmit audio when the analog input falls below a set level; they are used in the companded mode *only*. The levels at which the noise reduction circuits are enabled include hysteresis for further improved performance; these levels are about –55 and –60 dB. When the VBAP detects these low audio input conditions, it puts out a zero code (1111 1111 in μ-Law and 0101 0101 in A-Law, according to CCITT G.711 specifications). This is different from the normal output under idle channel noise conditions, which typically consists of a random sequence of codes around 0 (LSB and/or second LSB and MSB sign bit toggling arbitrarily).

Receive Channel

Decoding (D/A Conversion)

Data can also be received in either a fixed or variable data rate mode. See *Fixed- and Variable-Data-Rate Modes* on page 6 for more detail.

In the companding modes, the serial data word is received at DIN on the first eight clock cycles in the fixed-data-rate mode or the last eight clock cycles in the variable-data-rate mode. The decoding section converts the 8-bit PCM data into an analog signal with 12 bits of dynamic range, according to CCITT G.711 specifications. In the linear mode, the serial data word is received in the first 13 clock cycles. In both the companded and linear modes, input data is clocked in on consecutive *negative* transitions of the receive clock, which is CLK in the fixed-data-rate mode and DCLKR in the variable-date-rate mode. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. The sample is then transferred to the receive filter during the next frame.

Receive Filters

The receive filter is a switched capacitor sixth-order low-pass filter with a cutoff of 20 kHz; it provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specifications and the CCITT recommendation for G.712. The filter also contains the (sinx)/x correction response of such decoders.

Receive Buffer/Volume Control

The receive buffer contains the volume control circuitry. When data is received in the linear mode, the 13 bits are read as data, and the remaining 3 bits are used as programmable volume control of the analog output. These volume control bits originate from a DSP or other device that is interfaced with the VBAP, and they serve to attenuate the speaker output of the VBAP in seven 3-dB steps. The volume control bits are *not* latched into the VBAP, so they must be present in each received data word. If they are missing, the VBAP circuitry will assume that the three volume control bits are 0 (0-dB attenuation). In the companded mode, programmable gain is not used. Table 1 illustrates the volume control bits required for a given attenuation.

Table 1. Receive-Channel Volume-Control Bits

Bits 14–16 in DIN Input Data Stream	Resulting Receive Channel Attenuation
000	0 dB
001	-3 dB
010	-6 dB
011	-9 dB
100	-12 dB
101	-15 dB
110	-18 dB
111	-21 dB

NOTE: The first bit is the MSB.

Speaker Amplifier Overview

The VBAP incorporates an analog output power amplifier. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration. In addition, the VBAP speaker output stage (in its differential configuration) allows for further volume control (in addition to the volume control bits), by connection of a resistor chain to the output terminal of the device.

The speaker amplifier output will typically assume a DC offset of approximately 40 mV. This is a normal consequence of using switched capacitors in the VBAP design. Potential biasing problems can be avoided by the use of an AC coupling capacitor.

Timing and Clocking

Master Clock and Frame Sync

The VBAP requires a master clock and frame sync. The master clock is used for many internal functions, most notably to clock the switched capacitor filters and the A/D-D/A conversion process in both the transmit and receive directions. The VBAP family (TCM320ACxx) accommodates a variety of master clock frequencies, as shown in Table 2.

Table 2. VBAP Master Clock Frequencies

Device Suffix (xx)	Master Clock (MHz)
36, 37, 46	2.048
39	2.6
41	1.152
42	1.944
44	1.536

Power-Down and Standby Operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power-down, an external low signal is applied to PDN. In the absence of a signal, PDN is internally pulled up to a high logic level, and the device remains active. In the power-down mode, the average power consumption is reduced to 1.25 mW.

The standby modes give you the option of putting the entire device on standby or putting only the transmit or receive channels on standby. The standby modes are entered by removing one or both of the frame syncs. Table 3 illustrates all VBAP modes of operation.

Table 3. Power-Down and Standby Procedures

Device Status	Procedure	Typical Power Consumption	Digital Output Status
Power on	PDN = high FSX = pulses FSR = pulses	40 mW	Active
Power down	PDN = low FSX/FSR = X/X	1.25 mW	TSX and DOUT in a high-impedance state
Entire device on standby	FSX = low FSR = low PDN = high	5 mW	TSX and DOUT in a high-impedance state
Receive only (transmit standby)	FSX = low FSR = pulses PDN = high	20 mW	TSX and DOUT in a high-impedance state within 5 frames
Transmit only (receive standby)	FSR = low FSX = pulses PDN = high	20 mW	Active

Fixed- and Variable-Data-Rate Modes

The VBAP is designed to operate in both the fixed and variable-data-rate modes. The mode of operation is pin selectable. In the fixed mode, the data is transmitted (or burst) and received at the rate of the master clock frequency and is sampled every frame. In the variable-data-rate mode, the data is transmitted or received at a rate slower than the master clock frequency and uses the data clock input DCLKR.

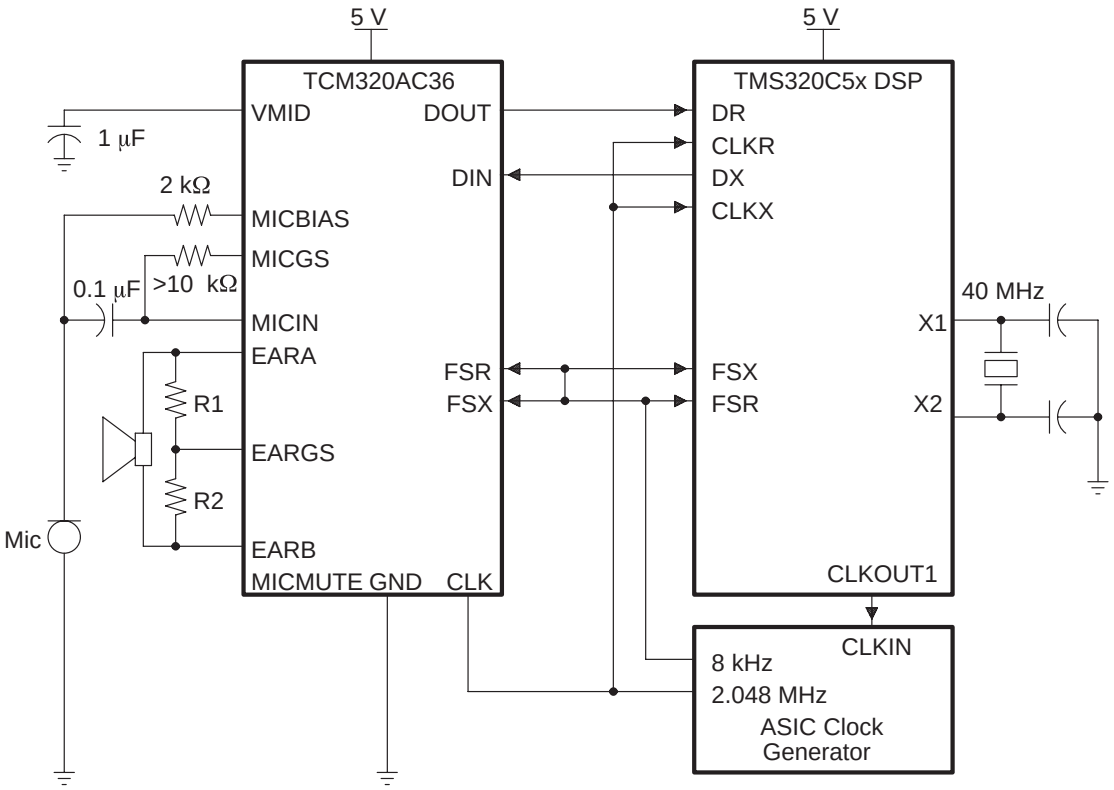
For example, suppose you are using the TCM320AC36 VBAP in the 8-bit companded mode and variable-data-rate configuration. This VBAP has a master clock frequency of 2.048 MHz and must use a frame sync of 8 kHz to maintain a 256 master-clock-to-frame-sync ratio. The data is sampled every 125 μs, but the speed at which the data is transmitted (or burst) and received, each 125 μs, can vary from 2.048 MHz to 64 kHz. Notice that the slowest speed of the data clock is 64 kHz; any slower speed would not allow a full 8-bit sample to be performed before the next frame begins. At 64 kHz, the complete frame is used to transmit or receive the data (8 bits $\times$ 8000 = 64 kbps). Likewise, the minimum variable-data-rate speed for the 16-bit linear mode would be 128 kHz (16 kHz $\times$ 8000).

Application Information

VBAP interfaced to a DSP

The most common application for the VBAP is as an interface to a DSP. The VBAP performs the analog-to-digital and digital-to-analog conversions, along with filtering, while the DSP performs more complex functions with the encoded speech. For example, in a cellular telephone application, the DSP would typically perform equalization and speech coding through the use of algorithms (code) executed by the DSP. The circuit in Figure 3 illustrates a typical VBAP-to-DSP interface.

Figure 3. VBAP Interfaced to a ’C5x DSP



Device Power-Up Sequence

The VBAP should be powered up and initialized as follows:

1. Apply GND
2. Apply V_{DD}
3. Apply low to PDN bar
4. Connect master clock
5. Connect data clock (if used)
6. Remove low to PDN bar
7. Apply FSX and/or FSR synchronization pulses

Grounding and Decoupling

Use a ground plane on the PCB, covering as much unused area as possible.

Bypass the VBAP with a high-quality 0.1-μF ceramic capacitor (such as a CK05) *directly across the VBAP power supply pins.* Ceramic capacitors have a low ESR (equivalent series resistance) or high Q; they are able to react to fast changes in voltage and are used to suppress high-frequency transients. High-frequency voltage transients result from instantaneous high current consumption during digital device switching. Since all power supplies have an internal impedance that prevents infinite current sourcing, power supply voltage ripple, or noise, will result. Capacitive loading on the power supply rail regulates the voltage of the supply.

Any power supply noise on VMID would normally be detected on the output of the VBAP; therefore, VMID is brought to an external pin so that the voltage can be filtered by using an external capacitor. The optimum capacitor combination is a 1-μF ceramic in parallel with a 470-pF ceramic chip cap.

Power Supply

A voltage regulator should always be used, even with battery power. Batteries in particular have a high internal impedance that allows the DC voltage to vary under instantaneous current consumption during digital switching. The resultant change in voltage manifests itself as noise on the power supply rail.

Use a 10-μF capacitor across the power supply rails on the PCB. This serves the same purpose as the ceramic capacitor, except that it responds well to lower frequency transients.

All power supply traces should be as close as possible to the ground plane. Proximity to the ground plane adds parallel capacitance.

Variable Data Rate at Master Clock Frequency

In some applications, it is desirable to run the VBAP in the variable-data-rate mode at a data rate equal to the master clock speed. This gives you the advantage of using the variable-data-rate mode (as with repeated data while frame sync is high) while still running the maximum data rate as in the fixed-data-rate mode (in fixed-data-rate mode, the data clock is internally run at the master clock speed).

If the device is operated in the variable-data-rate mode with the data clock run at the master clock frequency, the DCLKX and MCLK pins cannot be directly connected externally. If you choose to use the master clock as the DCLKX, you must buffer the output of the master clock before connecting it to DCLKX. This is necessary because the VBAP always powers up in the fixed-data-rate mode, and for the first several clock cycles, the DCLKX pin is actually an output ($\overline{\text{TSK}}$) as defined in the data sheet. The $\overline{\text{TSX}}$ output is a transmit time strobe that will pull the MCLK pin low; this will corrupt the MCLK input, if MCLK and DCLKX are directly connected externally to the device. Only after the first several master clock cycles does the device assume a fixed-data-rate mode and the DCLKX pin become an input. Therefore, the suggested method is to join MCLK and DCLKX *before* a buffering stage for the DCLKX line.

Typical PCM Output Expected From a Transmit VBAP

In an ideal situation, the 8- (and 13-bit) A/D converter in the VBAP is designed with a noise floor that equates to the transition of half the LSB. In the linear mode, a half bit represents approximately –75 dB, as shown below:

$$20 \times \log\left[\frac{2^{0.5}}{2^{13}}\right] = -75 \text{ dB} \quad \textbf{(1)}$$

This corresponds to the VBAP data sheet, which specifies the transmit noise in linear mode to be –74 dB. Therefore, using a VBAP in the receive mode, configured for a maximum output signal of 4 volts peak-to-peak ($V_{P–P}$, which is equal to 1.414 V_{rms}), the VBAP would encode this half bit of noise and experience about 250 μV_{rms} of noise on the speaker output terminals, as in this equation:

$$-75 \text{ dB} = 20 \times \log \frac{X}{1.414 V_{rms}} \quad \textbf{(2)}$$

where X = output that is 75 dB down from 1.414 V_{rms} (that is, X = 250 μV_{rms}).