

*TMS320 DSP  
DESIGNER'S NOTEBOOK*

# ***Interfacing a TMS320C2x, 'C2xx, or 'C5x DSP to an 8-Bit Boot EPROM***

---

---

*APPLICATION BRIEF: SPRA263*

*Gary Przyborski  
Digital Signal Processing Products  
Semiconductor Group*

*Texas Instruments  
October 1995*



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

## **TRADEMARKS**

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

## CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	<a href="mailto:dsph@ti.com">dsph@ti.com</a>

## Contents

Abstract .....	7
Design Problem.....	8
Solution.....	8

## Examples

Example 1. Example Code for a TMS320C52 .....	8
---	---



# Interfacing a TMS320C2x, 'C2xx, or 'C5x DSP to an 8-Bit Boot EPROM



## Abstract

This document describes how to interface a TMS320C2x, TMS320C2xx or TMS320C5x DSP to an 8-bit boot EPROM.



## Design Problem

How do you interface a 'C2x, 'C2xx, or 'C5x DSP to an 8-bit boot EPROM?

## Solution

For cost-conscious designs, the user may wish to use a TMS27C256 EPROM. However, for maximum flexibility, the use of the TMS27C512 allows for future software expansion, code evaluation, and increased availability of parts. The addition of an extra output to supply this A15 pin is often too much of a penalty since global memory exists for a maximum of 32K words or bytes, 0X8000 to 0XFFFF.

One approach to solve this problem is to use the FSX pin on the serial port. On power-up, this pin is three-stated so you need to add a pull-up resistor of 10K ohms on this line and then connect it to the  $V_{PP}$  pin of the TMS27C256 (see pages 7-15 of the 1995 TI MOS Memory Databook - SMYD095). The  $V_{PP}$  line on the TMS27C256 must be held at +5 V DC. This same pin is address A15 on the TMS27C512 (see pages 7-69 of the TI MOS Memory Databook).

On power-up with a TMS27C256, everything proceeds as usual. Address 0X7FFF in the TMS27C256 contains the boot routine selection byte, XXXXXX01b, typically 0x81 for a boot from 0X8000 global memory (0X000 in EPROM). The first four bytes of the EPROM memory contain the destination and length of the data to be transferred.

When using the TMS27C512, the operation is similar, except the boot routine byte is located at 0XFFFF in the EPROM. The starting four bytes of destination and length of transfer is located at 0X8000 in the TMS27C512. Now, the initialization code in your software will set the FSX pin to a low value and then transfer the rest of the code and/or data to RAM from 0X0000 up to 0X7FFF of the EPROM.

### *Example 1. Example Code for a TMS320C52*

```
Lacl #80h           ;Set global memory for maximum
Samm greg
Lamm spc           ;Set A15 of EPROM to a "0"
Or #00020h
Samm spc

                                transfer code from EPROM into RAM here

lamm spc           ; Return A15 of EPROM to a "1"
and #0FFDFh
samm spc
```