Implementing a Sensorless Brushless DC Motor Phase Advance Actuator Based on the TMS320C50 DSP

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Implementing a Sensorless Brushless DC Motor Phase Advance Actuator Based on the TMS320C50 DSP

Abstract

This application report describes the development of a sensorless brushless DC motor phase advance actuator system based on the Texas Instruments (TI™) TMS320C50 digital signal processor (DSP) and TMS320C50 evaluation module (EVM). Results show that applying a direct digital control methodology to the problem of controlled phase advance in a brushless DC machine substantially increases the effective speed range and facilitates a constant power profile. In addition, a further application to the control of torque ripple during controller saturation is demonstrated.

Phase advance techniques provide field-weakening operation for brushless machines and have been the subject of significant research over recent years.[1] [2] [3] Unlike previously documented methods that typically require a position encoder, the technique described in this paper renders such position sensing equipment redundant, reducing unit costs and increasing system reliability.

The ability to perform significant mathematical computations over relatively small sample periods (typically 50µs) allows precise control of electrical machine phase currents. A fast DSP hardware platform is thus paramount for investigating sensorless phase advance techniques. A desired system requirement is a fast data exchange capability with the external environment encompassing both integrated speed control, current, and phase advance actuation with diagnostic and supervisory procedures.

This document was part of the first European DSP Education and Research Conference that took place September 26 and 27, 1996 in Paris. For information on how TI encourages students from around the world to find innovative ways to use DSPs, see TI's World Wide Web site at www.ti.com.

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Introduction

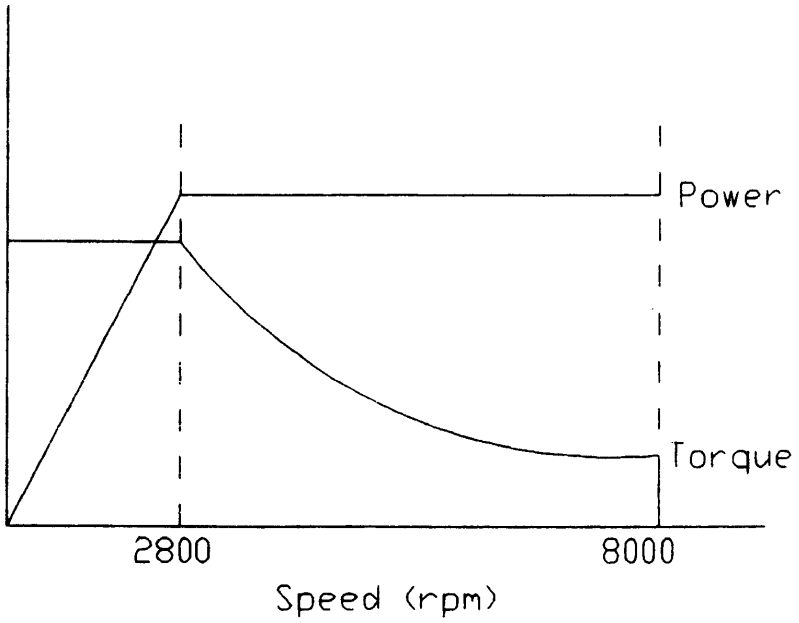
The application of DSP hardware has grown substantially during the last decade in the field of control applications, where the DSP's fast and efficient processing structures provide an ideal platform for the complex real-time algorithms often required for today's industrial problems. The mid-1980s saw the development of standalone control DSPs. This was later followed by faster fixed point units incorporating facilities to interface with the external environment and, more recently, the advent of powerful low-cost floating point architecture devices. [4]

Electrical machine control was one of the first research fields to take advantage of this continuing development with both AC and DC machines taking equal prominence in their application.[5] [6] As DSPs improved, algorithms not only achieved the desired control specification but also included safety and full tolerance features. More recently, system estimation and observer techniques have been included for acquiring immeasurable or inaccessible parameters, such as magnetic flux.

Although applications of DSP technology have become more diverse, only recently has interest occurred in the field of machine control for electric vehicles. This research concentrates on optimum power utilization and torque delivery mechanisms, with the induction machine and the brushless DC machine (BLDC) leading development.[7] [8] [9] Both topologies require relatively expensive sensors to achieve basic control, although the control algorithm for a BLDC machine is simpler than that for the induction machine.

The induction machine often utilizes complex AC transformation techniques.[10] However, for the control of an electric vehicle and other traction applications, the induction motor offers a desirable constant power operation as a result of its inherent ability to control the excitation flux (see Figure 1). Excitation flux control is often termed field weakening, and is not readily applicable to a BLDC machine due to the use of permanent magnets (PM) for the excitation field production.[11]

Figure 1. Typical Desirable Fraction Stem Operational Requirements.



This application report is organized in the following sections:

Field Weakening Operation of BLDC Motors provides an overview of the theory regarding field weakening of a brushless dc motor and an analysis of previous methods of phase advance actuation.[12 13]

DSP Hardware Specification and Design describes the hardware requirements and design, including the DSP interfacing and the realtime interrupt handling hardware.

Software Structure and Coding describes software structures for the control and actuation system, and the real-time execution of specific software routines.

Experimental Results includes results, which demonstrate the developed techniques on a prototype BLDC system with the application of the phase advance methodology.

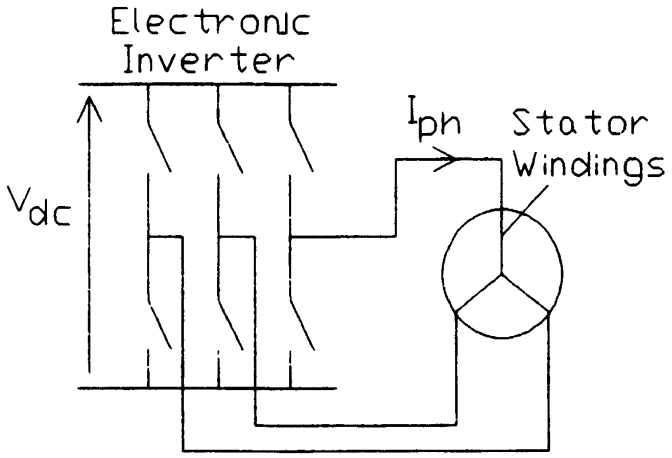
The results show the system performance under constant power operation and highlight a secondary application of the phase advance technique as a high-speed torque ripple reduction methodology that can be used during current controller saturation.

Field Weakening Operation of BLDC Motors

The basic elements of a brushless permanent magnet drive system are shown in Figure 2. The inverter is commutated to supply bi-directional current to the motor's three-phase, star-connected windings and create a rotating field in the motor's air gap.

Three discrete rotor position sensors and decode logic perform the commutation function. The interaction of the rotating air-gap field and the PM rotor field is the torque-producing mechanism of the machine. A three-phase configuration requires the rotor position information every 60 degrees electrical.

Figure 2. Brushless DC Drive System



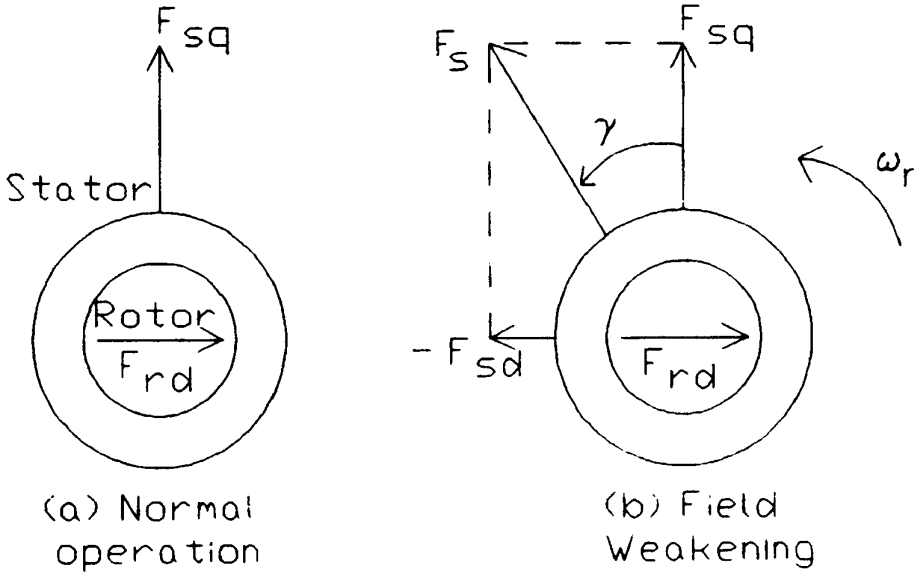
Under normal operating conditions, the speed is limited by the voltage rating of the driving inverter. The stator current is controlled to develop the maximum torque per amp. For a surface-mounted PM machine, this results in orthogonal displacement between the developed stator and rotor fields, which is maintained by controlling the commutation of the inverter (see Figure 3a). Using this methodology, the torque producing, or *quadrature*, component of current, i_q, is maximized, and the field producing, or *current*, component, i_d, is reduced to zero.

To achieve drive speeds above the nominal limit imposed by the inverter, the stator field is advanced by an angle, γ. This is accomplished by controlling the magnitude of the direct current vector to a negative value, resulting in a stator-supplied demagnetizing field that reduces the excitation field developed by the rotor magnets.

The value, i_d, is controlled to a value dependant on the extended speed required, and in turn, defines both the quadrature current and the required angle by which the commutation of the BLDC machine must be advanced, *Figure 3b.*

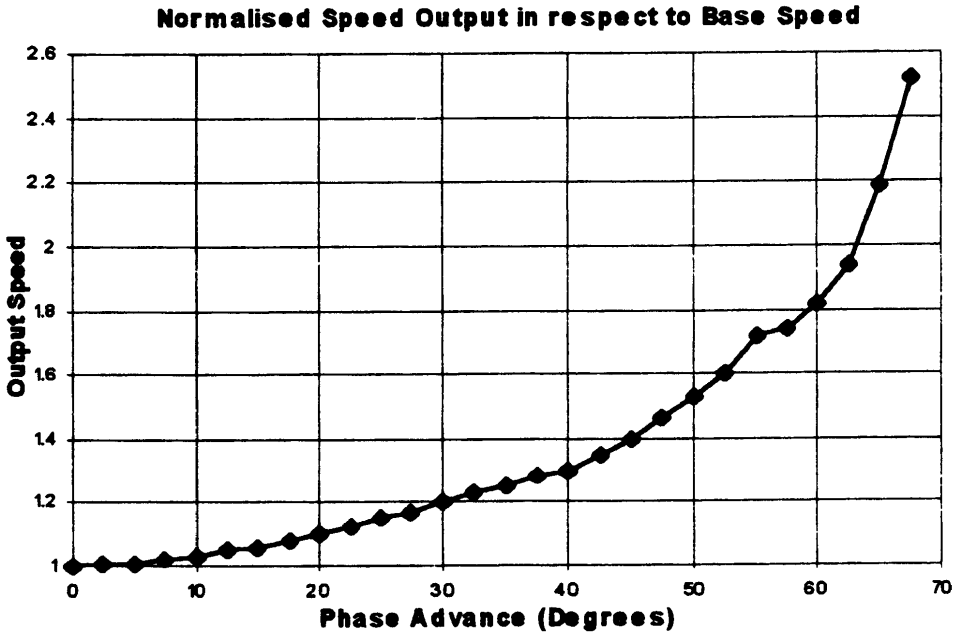
The speed response for a BLDC motor at varying advanced commutation angles is commonly determined by a combination of numerical simulation techniques and experimental testing of the machine. A vernier-based system is used to manually rotate the discrete position sensors.[14] However, this method is unusable in many practical environments because it cannot be accurately actuated. In addition, it is not mechanically sound with respect to vibration and other adverse conditions under which the desired system would operate.

Figure 3. Vector Representation of Field Weakening.



When applied to a BLDC machine, the phase advance methodology can provide a desired constant power characteristic for traction vehicles and spindle-drive based machine tool applications. For example, Figure 4 shows the normalized speed response to base speed for a commercial BLDC servo motor when subject to a phase advanced mode of operation.

Figure 4. Graph of Output Speed Vs Phase Advance of a Commercial Surface Mount Magnet BLDC Machine Under No-Load Conditions



However, while a *2.5:1* increase in rated motor speed has been shown, the potential exists for a much greater speed increase.[14] Given a minor change in rotor design achieved by insetting the magnets between small iron pole pieces, an improved field-weakening envelope and hence a better power speed envelope can be achieved (see Figure 5).

Also, a number of authors have shown that with appropriate motor design, an excellent constant power characteristic can be obtained for a standard surface-mount BLDC motor similar to the test machine (see Figure 6).[15] [16] [17]

Figure 4 also shows that a small change in phase advance can result in a large variation in motor speed, particularly at high phase advance. Hence, it is necessary to have a high-resolution rotor position measurement to achieve high-speed resolution. In servo systems, an additional position encoder often provides the position information. However, this adds considerable cost to the system implementation and also adds several constraints on the overall system performance, which typically suffer from poor mechanical properties (such as a limited tolerance to vibration) and inherent speed limitations.

Figure 5. Inset PM Rotor Magnet

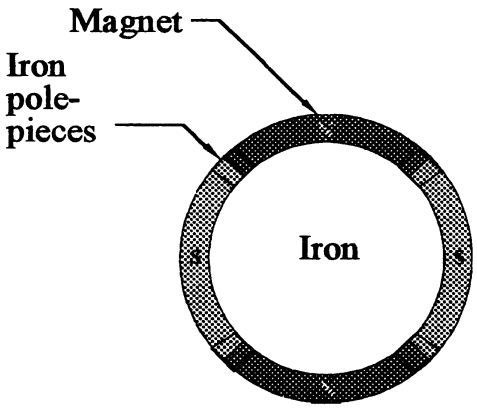
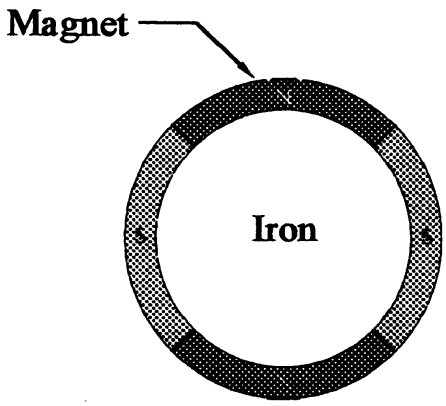


Figure 6. Surface Mount PM Rotor



If the system has sufficiently high relative inertia, as is the case for most traction applications, more than sufficient information is available from the existing discrete commutation sensors to estimate the rotor position to the required resolution. The processing required to determine the instant of inverter commutation can be performed in software using a dedicated hardware timer system. The resulting position resolution and hence speed resolution therefore becomes a function of the internal numerical representation of the software-based platform and any desecration techniques used in the control system.

DSP Hardware Specification and Design

The DSP-based development platform is designed around the TI TMS320C50 EVM. This PC-based module allows access to the control and data buses to interface to the external environment. In addition, the EVM offers 13 user-definable I/O ports and two maskable interrupt lines.

Additional hardware provides a flexible investigative and development platform, including

- 6 independent 12 bit (analog-to-digital) A/D channels

  Allow input from sensors and external commands

- 3*x* 12 bit D/A channels

  Monitor control variables under real-time conditions

- 16 digital bit I/0s
- Interrupt handling
- 2 additional 16 bit up/down timers
- 3 external timer registers for data and control

The expansion circuits are connected to the DSP control and data buses via a common backplane bus system terminated by a transceiver buffer card. The developed prototype system is shown in Figure 6.

The TMS320C50 EVM has two dedicated interrupt lines accessible by the user. Nevertheless, an external interrupt handler is required to provide an interrupt scheduling strategy. The specification requires prioritized interrupts for the following processes:

- External sample timer

  This unit controls the sample time for the 3-phase current control loop and acts as a selective *totalized seed* for the speed control loop. The sample timer uses a simple dual-inverter oscillator circuit and also performs safety functions for fault and thermal overload detection routines.

- External programmable timers

  The external timers required for the phase advance actuator are comparable to the internal DSP timer. They are 16 bit timers with reset and pre-load capabilities with a user-definable clock frequency ranging from a maximum of 16 MHz down to 31.25 kHz. Each timer has a dedicated external I/O

port for R/W operations. Both share a single write only external register for clock frequency selection. A disable bit for each respective timer is also included.

- Discrete position change

  The phase-advance algorithm requires that the DSP be interrupted at every transition point of the commutation logic. This is achieved using a summer with carry and a settable flip-flop, in which the flip-flop is set by the lACK signal once the interrupt routine is started.

- Internal programmable timer (using TINT)

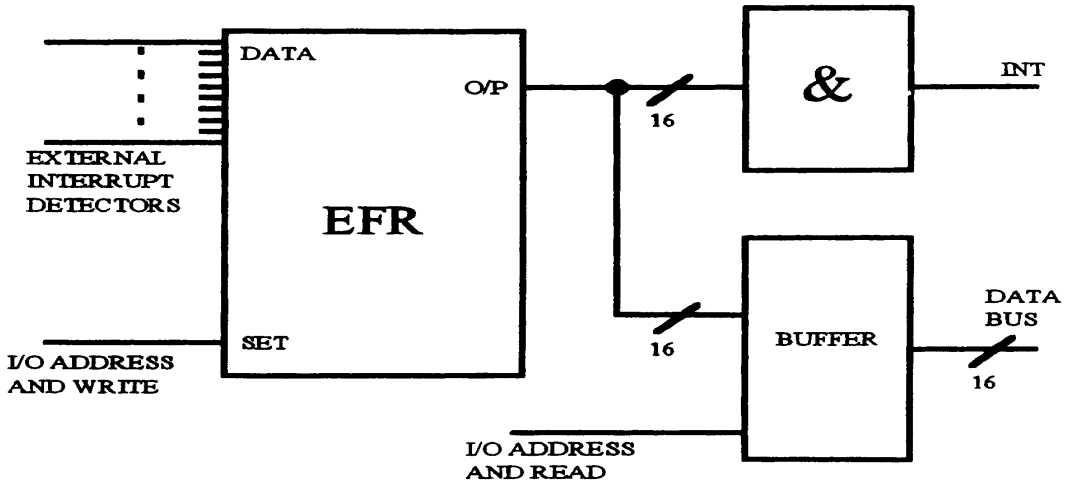
  This timer is used for the PWM inverter control within the current control loop and allows duty cycle control from zero to a full PWM period.

An external flag register allows the DSP to recognize and service all of the system interrupts. A dedicated external 16 bit register stores all the interrupt flags from the respective detection circuits and activates a DSP interrupt upon receipt.

The DSP subsequently services the routine and reads the external register to identity which action to take. It then clears the respective flag by writing back a masked copy to the external flag register. If more than one service is required, the register contents are preserved for the next interrupt service call. Consequently, if the register is sequentially bit tested, it allows the service calls to be prioritized with only a small processing overhead.

This technique allows a maximum of thirty-two user interrupts to be connected to the two available DSP interrupt lines and requires only two external I/O ports for the register addresses. However, it could easily be extended to allow 256 user interrupts per DSP interrupt line, although this number of interrupts may be beyond the serviceable capability of the DSP and would require four I/O external address ports.

Figure 7. Extended Interrupt Handling Circuit



Software Structure and Coding

The software structure comprises:

- An initialization routine
- Two mutually exclusive real-time speeds and current controllers
- A base routine to perform the phase advance actuation

The initialization procedure is executed to set up both the DSP and the external hardware platform, update system variables and interrupt flags, and perform an initial safety check and initial position measurement.

The execution hierarchy of the main program ensures that all interrupts and subroutines are executed in priority order, which is determined by execution timing constraints and safety requirements. However, when a fault condition is detected, all access and execution rites are revoked. The full detection and safety routines take control and either rectify the fault or bring the system into a controlled state of rest. System priorities are shown in descriptive form below, each layer mutually exclusive to the following layers, and the routines in the top layer subdivided by prioritized execution status:

1) INT 2: EFR Interrupts;
   a) Commutation: Change the 60° interval initial inverter switching state in respect to a change in position
   b) Timer 2: Selects the correct output sequence depending on current demand, position, and phase advance demand
   c) Sample: Set flag to signify time for current/speed control and check system safety limits
   d) Timer 1: Not used at present, reserved for later use

   TINT: Internal DSP Timer Interrupt : Outputs desired inverter switching sequence at correct phase advance location.
2) Current Controller (ISR20): User interrupt routine defined in interrupt branch table of TMS320C50 DSP, and found at interrupt address vector + 20H, specified during initialization;
3) Speed Controller (SPDCTRL): User interrupts routine executed on demand of the current controller, however, it is not defined within the DSP interrupt table.
4) Phase Advance Actuator (MAIN): Main Program routine that determines the change in inverter output state.

Example 1. External Flag Register (EFR) Interrupt Handler

```
ISR2:    LAR AR7,#EIFR
REREAD:  LAMM PA1O
         SAMM PA10
         AND #OFH
         SACL *
         LACL ~
         OR *
         SACL *
         ;
         ;External ISRs in priorty order
         ;
         BIT *,12
         BCND COMUTATE,TC
         BIT *,14
         BCND TIMER2,TC
         BIT *,15
         BCND SAMPLE,TC
         BIT *,l3
         BCND TIMER1,TC
         RETE
```

The EFR routine handles the sequential execution of the external interrupt demands and determines the execution priority according to the sequence of bit testing in the software routine. However, the default order is defined during the EFR circuit design. On finding an interrupt flag, a respective ranked value is written back to the EFR to clear the flag and preserve the other flags in the register.

On completion of the respective interrupt service routine, the EFR is rescanned for any subsequent interrupt demands and only exits once the EFR is empty. Hence, this methodology ensures that no external interrupts are overlooked due to the exclusive execution of each routine and minimum interrupt response latency is realized.

The speed and current controllers are based on the P1 structures with additional modifications to allow the application of variable or scheduled gains for steady state error elimination.[18] This is achieved by allowing the control parameter vectors to be updated at each interval and allowing a variation of the saturation constraints of both the proportional gain and integral terms.

Example 2. Variable Gain and Saturation Limits

```
ERROUT:
      ;
      ;CALCULATE KP(YSP-Y)
      ;
      SETC INTM
      LT *+    ;ERROR
      MPY *+      ;KP
      ;
      ; Check for Proportional Saturation & Scaling
      ;
      PAC
      CLRC IMTM
      SACB
      LEMMR TREG1,#SATSHR
      SETC SXM
      SATL
      CLRC SXM
```

The speed and current control routines are defined as user interrupt service routines and are called by both the current control interrupt and the INT2 DSP interrupt, respectively. Each routine performs a stack dump of the respective interrupt address; hence, on completing the interrupt, the DSP pops the stack into the program counter, forcing execution to start at the new interrupt prior to returning to its original address.

However, the DSP only performs a hardware context save during a hardware interrupt call; hence, the speed and current controller ISRs save the system status before execution is permitted and restores the previous condition on completion (see Example 3 and Example 4).

Each user-defined ISR maintains a predefined storage stack area. However, care must be taken to ensure that each routine cannot be called before its respective completion of the system state restoration. This prevents the previous state (and if enough DSP stack calls are executed, the return address) from being lost and a program execution error occurring. The product register is not included in the context save, as all multiplication operands are executed while under a disabled interrupt 'SETC INTM' condition as shown in Example 1; hence, the register can be changed by all routines, and no context save is required.

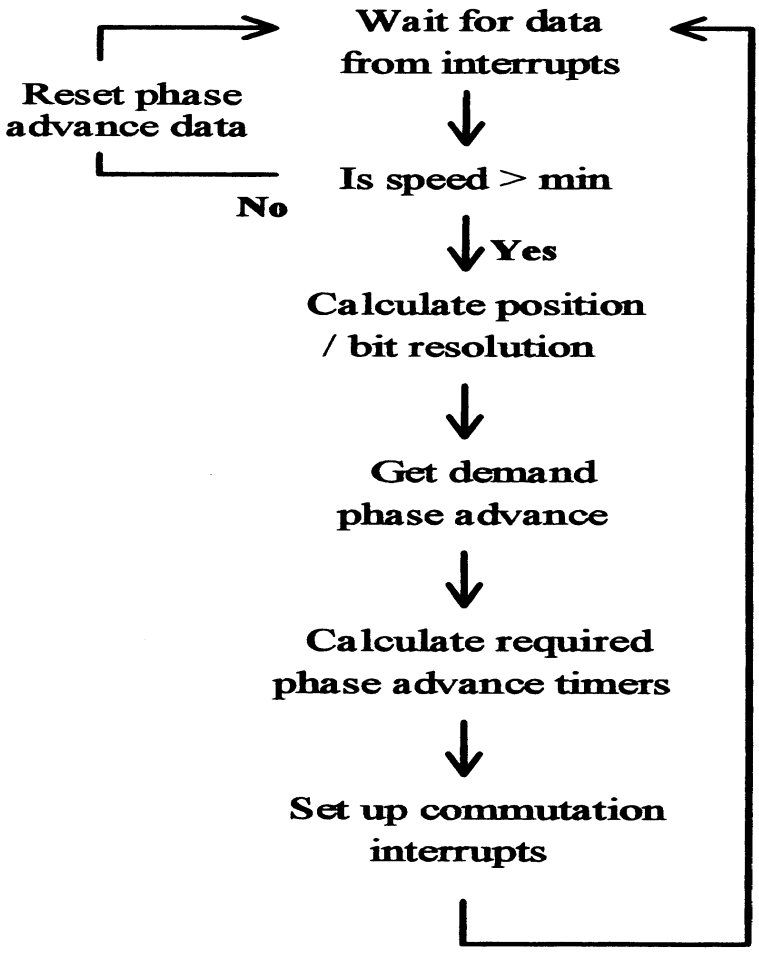
Example 3. Software Context Save of ACC, ACCB, ARO-7, TREGO-3, ARCR, INDX, SSTO-1, and PMST

```
SAVE: SETC INTM
      MAR *,ARO
      ;
      ;Software Context Safe: Register Preserved are
      ;ACC,ACCB,ARO-7,PMST,ARCR,TREGO-2,JNDX,STl
      ;
      SMMR AR0,#CURSTACK
      SMMR AR1,#CURSTACK+l
      SMMR AR2,#CURSTACK+2
      SMMR AR3,#CURSTACK+3
      SMMR PMST,#CURSTACK+4
      SMMR TREGO,#CURSTACK+5
      SMMR TREGl,#CURSTACK+6
      SMMR TREG2,#CURSTACK+7
      SMMR INDX, #CURSTACK+8
      SMMR ARCR,#CURSTACK+9
      LAR AR0,#CIRSTACK+10
      SST #0,+
      SST #l,+
      SACL *+
      SACH *+
      IACB
      SACL *+
      SACH *+
      CLRC INTM
```

Example 4. Software Context Restore of ACC, ACCB, ARO-7, TREGO-3, ARCR, INDX, SSTO-J, and PMST

```
RESTORE: SETC INTM
         LMMR AR0,#CURSTACK
         LMMR AR1,#CURSTACK+l
         LMMR AR2,#CURSTACK+2
         LMMR AR3,#CURSTACK+3
         LMMR PMST,#CURSTACK+4
         LMMR TREGO,#CURSTACK+5
         LMMR TREGl,#CURSTACK+6
         LMMR TREG2,#CURSTACK+7
         LMMR INDX, #CURSTACK+8
         SMMR ARCR,#CURSTACK+9
         LAR AR0,#CURSTACK+15
         LACC *-,16
         ADD *-
         SACB
         LACC *-,16
         ADD *-
         LST #1,*
         LMMR AR0,#CURSTACK
         CLRC INTM
```

Figure 8. Flowchart for Phase Advance Routine

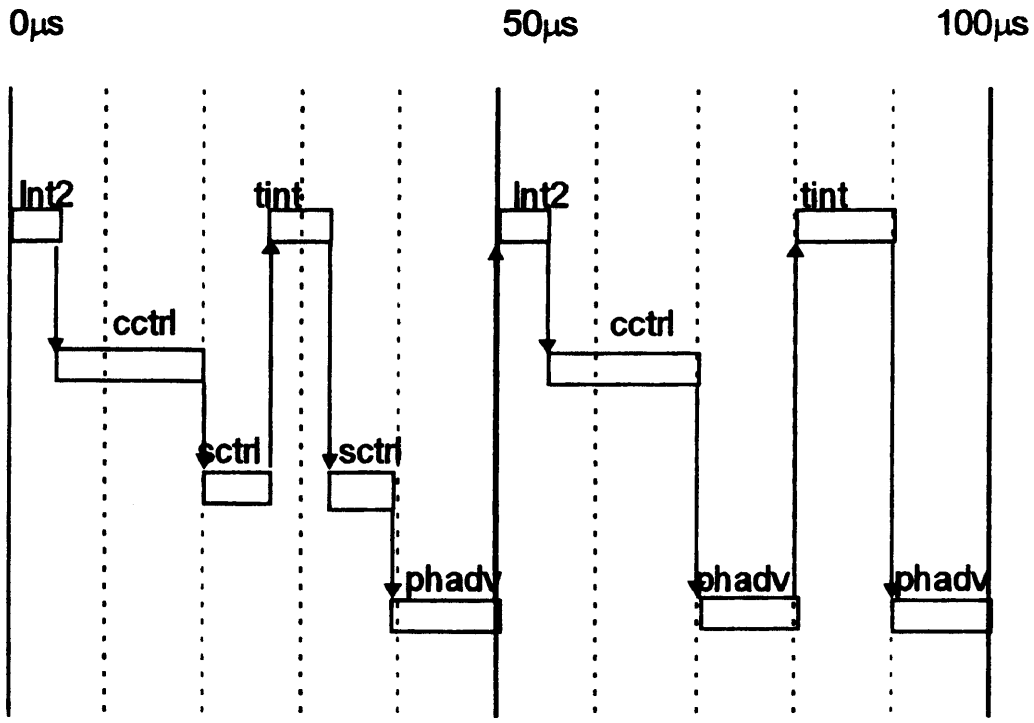


The main phase advance routine has the lowest priority because it only requires execution at commutation events. Hence, the time between subsequent executions is proportional to the motor speed.

However, the associated interrupts operate independently and gather the data required for the position estimation. The phase advance algorithm is represented by the flowchart in Figure 8, which shows the individual processes required to calculate the desired switching position.

A real-time time slice diagram for a typical execution of two sample cycles is shown in Figure 9.

Figure 9. Timing Diagram for Real-Time Operation



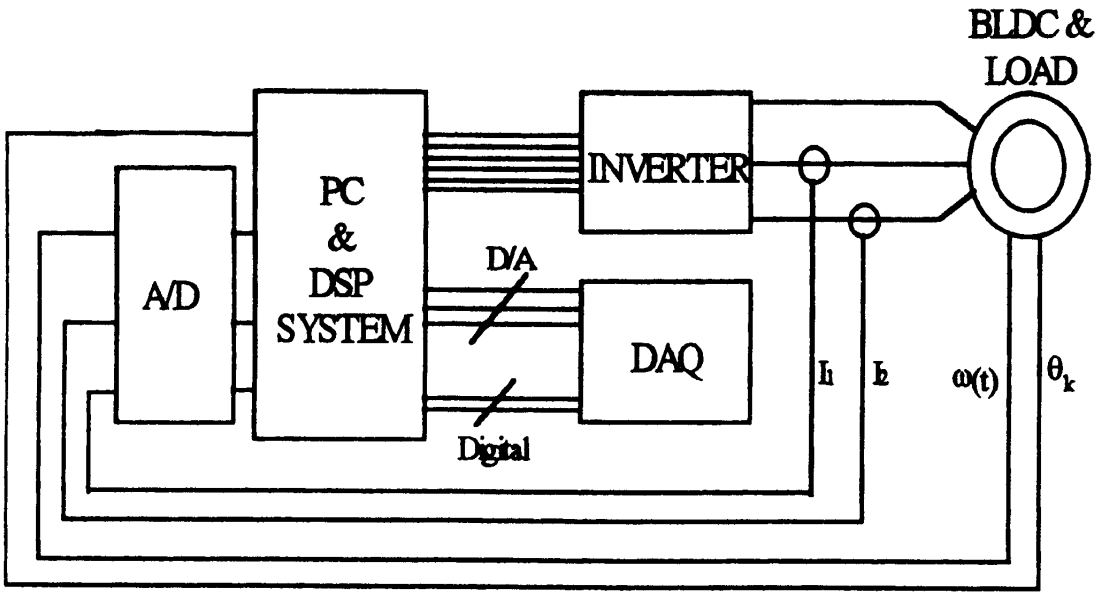
The top layer of priority can occur at any time during the 50 µs sample period, but the current controller is executed as soon as any interrupt activity is completed. This will activate the speed controller if the total speed equals the desired speed control sample period. Otherwise, execution returns to the main phase advance actuator program.

The speed and current controllers are executed within 12 µs and 15 µs respectively; hence, both routines can be executed within any one sample cycle inclusive of any latency from the interrupt routines. The phase-advance routine runs continually with execution pausing only between data measurement acknowledgements and system interrupts. Total execution time is 100 µs. Thus, the routine can operate up to a maximum speed of 10,000 commutation cycles per second, (≈50,000 RPM for a 4 pole BLDC machine).

Experimental Results

The DSP-based experimental test system setup is shown in Figure 10. The DSP system computes the required inverter switching sequence in response to the feedback of current, speed, and discrete position from the motor and dynamometer load system.[19]

Figure 10. Experimental DSP Test System Layout



Typically, only the DC link current is required to be fed back into a BLDC control system. However, to achieve increased control accuracy, two of the motor phase currents are fed back, the third phase current is generated using the following balanced circuit principle of a star-connected circuit:

$$I_3 = I_1 + I_2$$

The position feedback comprises a 3 bit digital signal of which the possible error states are 000 and 111 binary. Detection of these states invokes an error handling routine in the control system. The test machine is a commercial BLDC motor with a surface-mount PM rotor. The load is provided by a brushed DC motor-based dynamometer system. An inset PM rotor was also designed to allow testing of alternative rotor topologies.

Each rotor configuration is tested under constant input power conditions (constant DC link current) for a 40-volt supply. The shaft output power is measured by the dynamometer for incremental changes in phase advance demand. However, any system losses such as resistive and windage losses are not included.

A maximum step input speed demand is applied to fully excite both the speed and current controller routines and verify the operation of the DSP-based platform under nominal operating conditions.

The results of these tests surface mount and inset rotor motor topologies are shown in Figure 11 and Figure 12. The surface mount configuration provides a speed increase of *1.7:1* and the inset magnet configuration *2.5:1* with for the motors maximum obtainable speed at the respective load. Hence, the inset design gives a superior speed range extension compared to the surface mount design. Both results demonstrate the previously described condition of a large output speed change for a small increment phase advance at high phase advance angles.

Figure 11. Phase Advanced Output Power Profiles for Constant Input Power Conditions (Surface Mount Rotor)

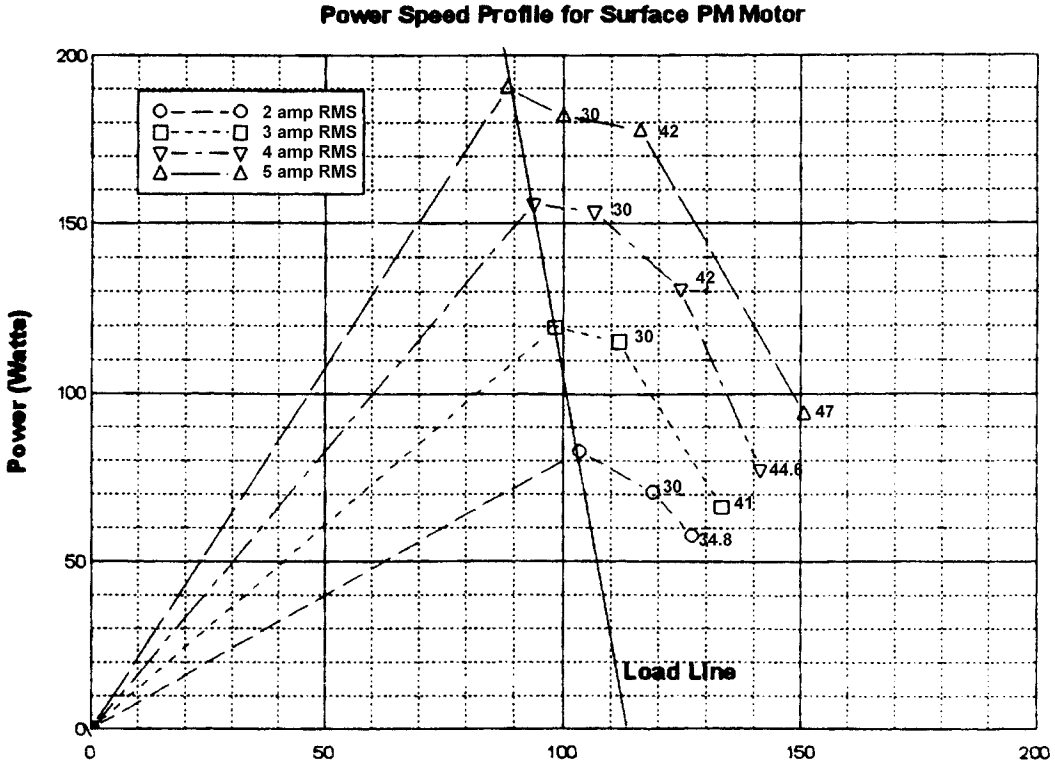
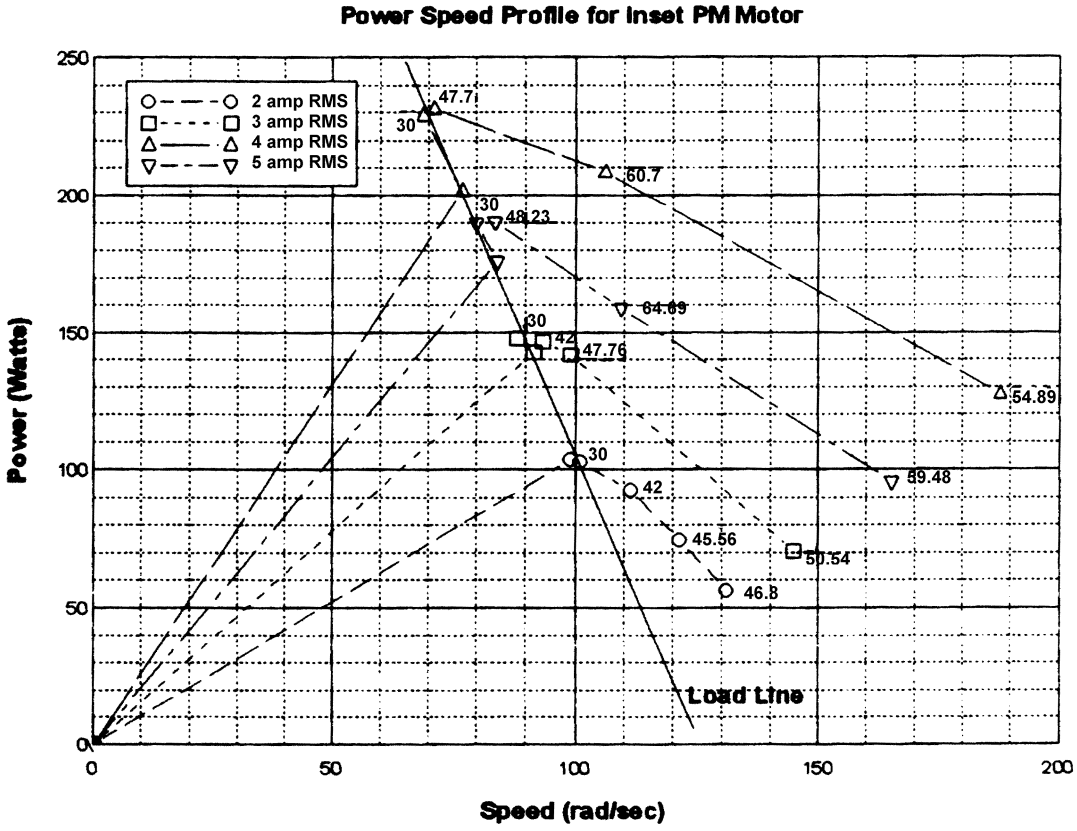


Figure 12. Phase Advanced Output Power Profiles for Constant Input Power Conditions (Inset Mount Rotor)



Further research is being undertaken into the reduction of torque ripple for a speed controller under high-speed operation using a controlled phase advance methodology.

Summary

This application report presented an overview of the TI TMS320C50 DSP-based hardware and software design for a phase advance actuator. Results from an experimental test system, showed that the system achieved an extended speed range of *1.7:1* for a commercial motor, further increasing to *2.5:1* for a non-optimized inset PM rotor design BLDC motor.

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