Application Report
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How to Begin Development Today With the TMS320C6411 DSP

Kimberly Daniel *C6000 Applications Team*

ABSTRACT

Development can begin now for the Texas Instruments TMS320C6411 high-performance digital signal processor (DSP) systems. Because of the compatibility between TMS320C6000™ generation devices, existing C6000™ software tools and development platforms can be used to develop code for the C6411 and other future devices. This capability allows for systems to be up and running when silicon becomes available.

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1 Introduction

The Texas Instruments TMS320C6000 generation of high-performance digital signal processors (DSPs) now includes the TMS320C6411. The TMS320C64x™ brings the highest level of performance in the C6000 generation of fixed-point DSPs. At clock rates of 300 MHz, the C6411 provides a low-cost, high-performance solution and can process information at a rate of 2400 MIPS (million instructions per second) at 1.2 core voltage.

Introduced in February 1997, the C6000 generation is based on TI's VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Advanced features of VelociTI architecture include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

The C64x™ employs VelociTI.2™ extension to the VelociTI architecture. The VelociTI.2 extension significantly improves performance with increased parallelism, orthogonality, packed data processing, and new instructions to accelerate performance in key applications.

The roadmap for the fixed-point C6000 DSP platform, shown in Figure 1, demonstrates TI's commitment to present highest-performance DSPs.

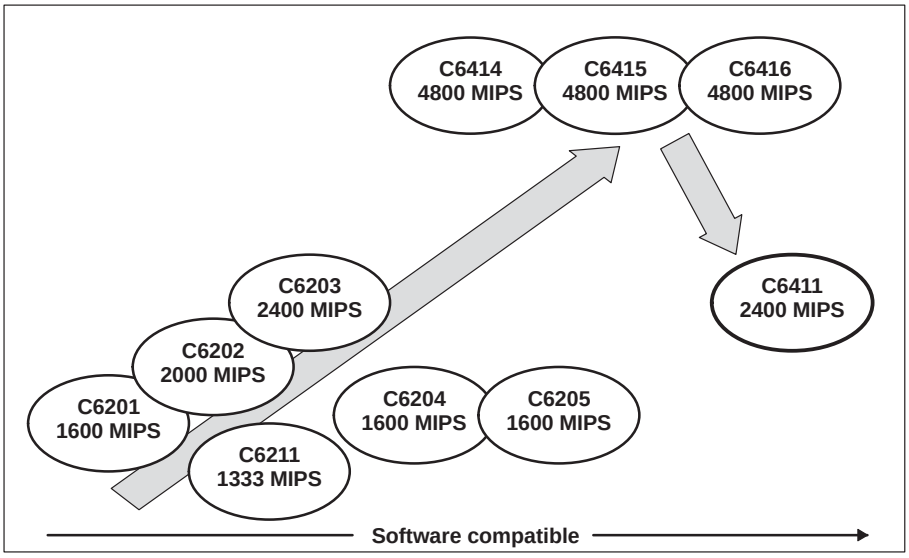

Figure 1. TMS320C6000 Highest-Performance Fixed-Point DSP Roadmap

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2 TMS320C60000 Compatibility

All C6000 generation devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (TMS320C67x™) members. The C64x DSP core is enhanced over the TMS320C62x™ DSP core designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI.2 provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to eight instructions during a single clock cycle—up to 2400 MIPS at 300MHz initial-device clock speed.

This common architecture allows designers to begin development with existing C6000 software tools for those devices currently in development. This also allows for migration from one C6000 processor to another, as design specifications require.

In addition to the DSP core, many of the on-chip peripherals are common between C6000 devices. Figure 2 shows a block diagram of the C6411. Most of these blocks reflect enhancements made over the C6211. See section 2.2 for details.

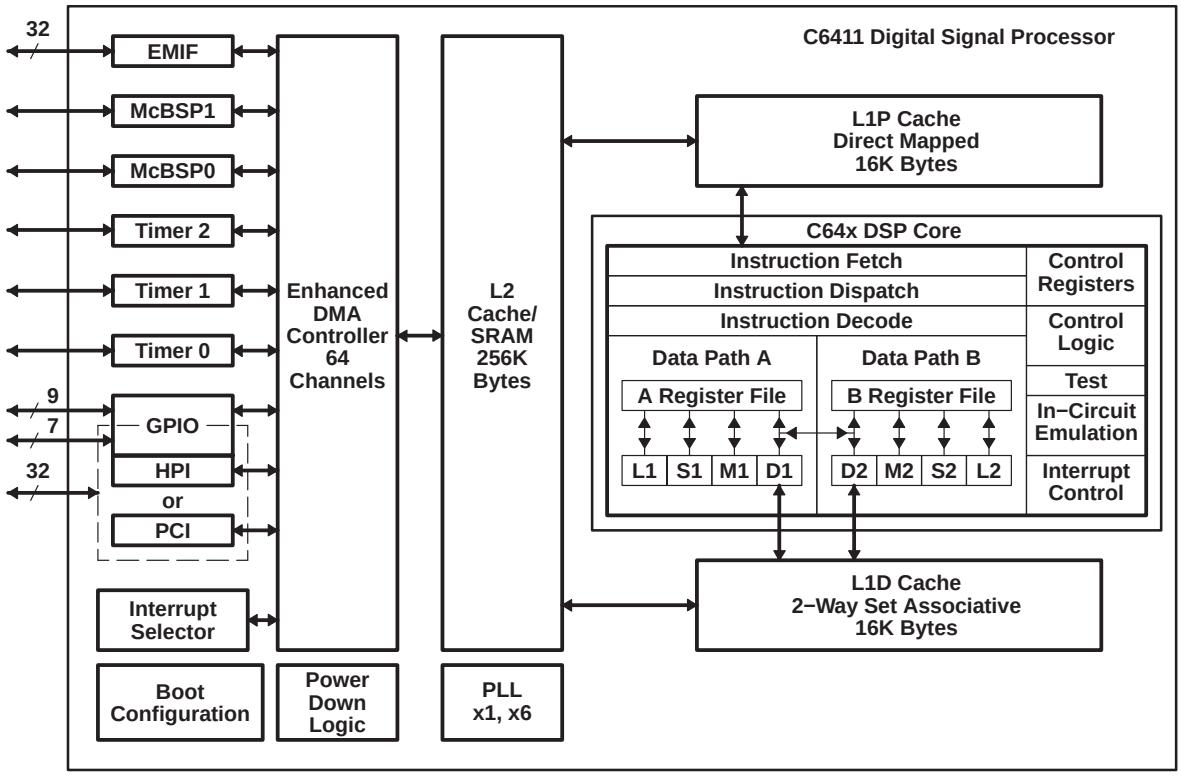

Figure 2. TMS320C6411 DSP Block Diagram

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2.1 C64x Advanced DSP Core

The C64x DSP core offers several enhancements over the C62x™ DSP core. They include:

- Register file enhancement
  - The register files have doubled in size. The C62x has 32 32-bit general-purpose registers, and the C64x has 64 32-bit general-purpose registers.
  - Register A0 can be used as a condition registers on the C64x in addition to A1, A2, B0, B1, and B2 condition registers available on the C62x.
  - The C62x register file supports packed 16-, 32-, and 40-bit data types. The C64x register file extends this by also supporting packed 8-, and 64-bit data types.
- Data path extensions
  - Each .D unit can load and store doublewords (64 bits) with a single instruction. The .D unit on the C62x cannot load and store 64-bit values with a single instruction.
  - The .D unit, as well as the .L, .M and .S functional units, can now access operands via a data cross-path. In the C62x, only address cross-paths on the .D unit are supported.
  - The C64x pipelines data cross path accesses. This allows the same register to be used as a data cross-path operand by multiple functional units in the same execute packet. In the C62x, only one cross operand is allowed per side.
- Advanced instruction packing

  The C62x VelociTI architecture contains instruction packing. Eight instructions are fetched every clock cycle. Of these instructions, any, some, or all may be executed in parallel. To allow maximum usage of parallel instructions, the VelociTI architecture does not allow execute packets to cross-fetch packet boundaries. The code generation tools handled this limitation by padding fetch packets with NOP instructions. The C64x VelociTI.2 architecture extensions eliminate this limitation by including advanced instruction packing in the instruction dispatch unit. This improvement removes all execute packet boundary restrictions, thereby eliminating all of the NOPs added to pad fetch packets, and helps to reduce code size.
- Packed data processing
  - Instructions have been added that operate directly on packed data to streamline data flow and increase instruction set efficiency. The C64x has a comprehensive collection of quad 8-bit and dual 16-bit instruction set extensions.
  - Extensive collection of pack and unpack instructions simplifies manipulation of packed data types.
- Additional functional unit hardware
  - Each .M unit can now perform two 16 x 16-bit multiplies or four 8 x 8-bit multiplies every clock cycle.
  - The .D units can now access words and doublewords on any byte boundary by using non-aligned load and store instructions. The C62x only provides aligned load and store instructions.
  - The .L units can perform byte shifts, and the .M units can perform bidirectional variable shifts, in addition to the .S unit's ability to do shifts. The bidirectional shifts directly assist voice-compression codecs (vocoders).

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  - The .L units can perform quad 8-bit subtracts with absolute value. This absolute difference instruction greatly aids motion-estimation algorithms.
  - Special communications-specific instructions, such as SHFL, DEAL and GMPY4 have been added to the .M unit to address common operations in error-correcting codes.
  - Bit-count and Rotate hardware on the .M unit extends support for bit-level algorithms such as binary morphology, image-metric calculations and encryption algorithms.
- Increased orthogonality
  - The .D unit can now perform 32-bit logical instructions in addition to the .S and .L units.
  - The .D unit now directly supports load and store instructions for doubleword data values. The C62x does not directly support loads and stores of doublewords, and the C67x™ only directly supports loads of doublewords.
  - The .L, and .D units can now be used to load 5-bit constants in addition to the .S unit's ability to load 16-bit constants.
  - On the C62x, one long source and one long result per data path could occur every cycle. On the C64x, up to two long sources and two long results can be accessed on each data path every cycle.

2.2 Difference Between the C6411 and C6211 DSPs

Significant enhancements have been made to the C6411 over the C6211, to allow the C6411 to be the low-cost, high-performance DSP. These include:

- **DSP core:** The C6411 DSP features the C64x DSP core, while the C6211 has the C62x DSP core.
- **Core supply voltage:** The C6211 requires 1.8 V of core supply voltage. The C6411 requires only 1.2 V of core-supply voltage.
- **Core frequency:** The C6211 runs up to 167 MHz, while the C6411 will run up to 300 MHz.
- **Phase-Lock Loop (PLL):** The PLL circuitry on the C6211 supports clock multiplier factors x1 and x4, while on the C6411, multiplier factors of x1 and x6 are supported.
- **Internal memory:** To support the high performance of the DSP core, the L1/L2 caches in C6411 have been increased four times in size over C6211, with 16 KB each in L1P and L1D caches, and 256 KB in the unified L2 cache/SRAM.
- **Enhanced Direct Memory Access (EDMA):** The C6211 has 16 independent EDMA channels. The C6411 improves the EDMA to 64 independent channels.
- **External Memory Interface (EMIF):** The C6211 and C6411 both have a 32-bit wide EMIF. In addition, the C6411 EMIF offers additional flexibility by replacing the SBSRAM mode with a programmable synchronous interface mode, which supports glueless interfaces to the following:
  - Zero bus turnaround (ZBT) SRAM
  - Synchronous FIFOs
  - Pipeline and flow-thru SBSRAM

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- **Timers:** The C6211 has 2 Timers. One 32-bit timer has been added to the C6411, bringing the total to three.
- **Multichannel Buffered Serial Port (McBSP):** Additional new features in the C6411 include:
  - Enhanced multichannel selection capability allows the McBSP to independently select up to 128 channels per phase frame.
  - Enhanced sample rate generator.
- **Host Port Interface (HPI):** The C6211 has a 16-bit HPI. The advanced 32-bit HPI available in the C6411 allows 32- and 16-bit mode of operation.
- **Peripheral Component Interconnect (PCI):** The C6211 does not have a PCI. The PCI on the C6411 supports 32-bit interface at 33 MHz.
- **General-Purpose Input/Output (GPIO):** On the C6211, GPIO pins are shared with timers and McBSP pins. The C6411 extends this capability by adding a dedicated GPIO module, with 16 GPIO pins. The GPIO peripheral can be programmed to generate different CPU interrupts and EDMA events.
- **Device and boot configurations:** The C6211 uses pullup/down resistors on the HPI pins to determine boot process and device configurations at reset. On the C6411, the pullup/down resistors on dedicated pins determine boot process and device configurations.
- **Package and technology:** The C6211 is based on 0.18 μm/5-level metal process technology in a 27 x 27 mm, 256-pin BGA package. The C6411 is based on 0.13 μm/6-level metal-process technology in a 23 x 23 mm, 532-pin BGA package.

2.3 Similarities Between the C6411 and C6415 DSPs

The following device components are identical between the three devices:

- C64x fixed-point DSP core
- Enhanced DMA (EDMA) controller: 64 independent channels
- Host port interface (HPI): 32-bit-wide data bus, capable of 32- and 16-bit modes of operation
- Peripheral component interconnect (PCI): 32-bit, at 33 MHz
- General-purpose input/output (GPIO)
- Timer: three 32-bit general-purpose timers
- Power-down logic

2.4 Differences Between the C6411 and C6415 DSPs

The low-cost C6411 DSP can be viewed as the subset of C6415. The following is the list of differences between the C6411 and C6415 DSPs:

- **L2 internal memory:** The C6415 DSP has 1024 KB of L2 memory. The L2 memory on the C6411 is reduced to 256 KB.
- **EMIF:** There is one 64-bit EMIF, and one 16-bit EMIF on the C6415. The low-cost C6411 has one 32-bit EMIF.
- **PLL mode:** The C6415 device supports x1, x6, and x12 PLL multiplier mode. On the C6411 device, the PLL modes supported are x1 and x6.

- **Core frequency:** The C6415 device runs up to 600 MHz, whereas the C6411 runs up to 300 MHz.
- **Core supply voltage:** The C6415 operates at core voltages of 1.2 or 1.4 volts. On the C6411, the core supply voltage is 1.2 V.
- **Universal tests and operations interface for ATM (UTOPIA):** This peripheral exists only on the C6415.
- **McBSP:** The C6415 DSP has three McBSPs. The C6411 has two.

To summarize these differences, Table 1 compares the C6411 with C6211 and C6415 DSPs. Gray cells indicate C6411 enhancements over the C6211 DSP. See section 2.2 for details.

Table 1. Comparisons Between C6211, C6411, and C6415 DSPs

	C6211	C6411	C6415
DSP core	C62x	C64x	C64x
L1P	4 KB	16 KB	16 KB
L1D	4 KB	16 KB	16 KB
L2	64 KB	256 KB	1024 KB
EMIF	(1) 32-bit	(1) 32-bit	(1) 64-bit (1) 16-bit
EDMA	16 channels	64 channels	64 channels
HPI	16-bit	32-/16-bit	32-/16-bit
PCI	–	32-bit 33 MHz	32-bit 33 MHz
McBSP	2	2	3
UTOPIA	–	–	(1) transmit (1) receive
Timer	2	3	3
GPIO	–	16	16
Core frequency	Up to 167 MHz	Up to 300 MHz	Up to 600 MHz
Core voltage	1.8 V	1.2 V	1.2, 1.4 V
PLL modes	x1, x4	x1, x6	x1, x6, x12
Package	256-pin BGA 27 x 27 mm GFN suffix	532-pin BGA 23 x 23 mm GLZ suffix	532-pin BGA 23 x 23 mm GLZ suffix
Process technology	0.18 μm	0.13 μm	0.13 μm

For detailed information about device configurations and peripherals selection of C6411, see *TMS320C6411 Fixed-Point Digital Signal Processor* (SPRS196).

3 Highest-Performance DSP

The TMS320C64x DSP core scales operating speeds beyond 1 GHz and achieves 10x performance improvements over the industry's previous DSP performance leader, the TMS320C62x DSP. Chips in development couple this processing performance, with new memory and peripheral systems designed to accelerate real-time throughput for higher system performance.

The efficient on-chip cache architecture of the C641x allows system designers to use slower, cheaper external-memory devices for data and program storage, while keeping the high performance capabilities of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market.

The enhanced direct-memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the C641x memory map, the EDMA controller transfers data in the background of DSP core operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA controller offers 64 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA controller channel is synchronized by an event to allow minimal intervention by the DSP core.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. The C641x has 288K bytes of on-chip memory, with 32K bytes serving as a level-one (L1) cache that the DSP core can directly access. The L1 cache is divided into 16K bytes of program (L1P) and 16K bytes of data (L1D) cache memory. The remaining 256K bytes of on-chip memory are unified program and data memory space. It can serve as a level-two (L2) cache, be directly mapped as internal memory, or serve as a combination of these functions.

L1P is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a 256-bit-wide data path to the DSP core, so that the DSP core may fetch eight instructions (one fetch packet) every cycle.

L1D is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both DSP core data ports, so that the DSP core can load or store two 64-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations on a cache miss.

The 256K bytes L2 memory can be configured as memory-mapped SRAM, or a combination of SRAM and 4-way associative cache. The L2 memory can be programmed to be 0-, 32-, 64-, 128-, or 256K-byte 4-way associative cache, with the remaining set to memory-mapped SRAM. Blocks of L2 that are selected as cache are not included in the C6411 memory map. The mapability of L2 blocks, as addressable locations, allows critical code and data to be locked into internal memory.

TI has run extensive tests on this L1/L2 architecture to determine how it performs with an enhanced full-rate GSM vocoder, system-level applications in ADSL, V.90 modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent. In other words, only one instruction or data word in fifty needs to be fetched from L2 or external memory.

The high L1 hit rate, combined with the flexibility of L2 memory organization, means that this architecture can operate at more than 80 percent of the cycle performance of a more expensive device, with a traditional memory organization where all system memory is on the chip. This high degree of efficiency allows systems to rely on inexpensive external memory for program and data storage, while at the same time performing high-speed, number-crunching routines in real time.

4 Begin Writing Code for the C6411 Today

Full object-code compatibility with existing C6000 DSPs allows system developers to begin development of C64x DSP systems today. The code-compatible, fixed-point DSP cores in the C620x, C6211, and C641x devices allow for code to be written for the C6411 using existing C6000 tools. By taking advantage of the C6000 software and hardware tools currently available, C6411 systems can have a running start for when silicon becomes available.

The C6000 compiler may be used for all members of the C6000 device platform. Fixed-point devices are object code compatible, so the C64x may use code written for the C62x.

The C6000 simulator may be used to provide a cycle-accurate account of device performance and to provide a good environment to learn the C6000 VLIW architecture. The available C6415 configuration of the simulator is the closest configuration to model the C6411 device. EMIF and L2 configurations need to be adjusted to reflect the C6411 model. The C6415 configuration also models the cache performance of the device. Using this configuration, it is possible to optimize code structure and data organization to take advantage of the C6411 cache structure. C6411 designs may be worked out in detail on the simulator prior to purchasing actual silicon.

For a development start in hardware, the C6416 Test and Evaluation Board (TEB) may be used to understand the C6411 functionality. In this environment, code can be debugged while DSP core and peripherals are running in real time. The C6411 can be considered a subset of the C6416, therefore making the TEB the best tool to understand how to incorporate the peripherals into a real-time system. Applications running on the C6416 TEB with C6411 configuration will be 100% cycle accurate to a C6411 system. The identical architectures of the C6416 and C6411 devices allow for many system-level issues to be resolved prior to obtaining C6411 silicon.

Using these development platforms, as well as the C6000 literature currently available, will enable C6411 systems to be completed soon after C6411 silicon is made available.

4.1 C6000 Tools Support

C6000 tools are available now for use in all C6000 designs. The C6000 development tools available today for the C6411 are:

- C6000 simulator software
- C6000 Optimizing C Compiler/Assembler
- TMDX3260E6416 − C6416 test and evaluation board (TEB), bundled with Code Composer Studio™ and Spectrum Digital 510PP+

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- TMDX3260E6416E − C6416 test and evaluation board (TEB), bundled with Code Composer Studio and Spectrum Digital 510PP+ with European power cord
- XDS510 C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable

For the latest information of available tools, see the TI web site at http://www.ti.com

5 Literature Available

A great deal of literature is available today for the C6000 devices.

1. *TMS320C6411 Fixed-Point Digital Signal Processor* (SPRS196).
2. *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).
3. *Manual Update Sheet for TMS320C6000 CPU and Instruction Set Reference Guide* (SPRZ168).
4. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
5. *TMS320C64x Technical Overview* (SPRU395).
6. *Code Composer Studio User's Guide* (SPRU328).
7. *TMS320C6000 Code Composer Studio Tutorial* (SPRU301).
8. *TMS320C6000 Programmer's Guide* (SPRU198).
9. *TMS320C64x Image/Video Processing Library Programmer's Reference* (SPRU023).
10. *TMS320C64x DSP Library Programmer's Reference* (SPRU565).
11. *TMS320C6000 Chip Support Library API Reference Guide* (SPRU401).
12. *TMS320C6000 Assembly Language Tools User's Guide* (SPRU186).
13. *TMS320C6000 Optimizing Compiler User's Guide* (SPRU187).
14. *TMS320C6x C Source Debugger User's Guide* (SPRU188).
15. *TMS320C6x C Source Debugger For SPARC* (SPRU224).
16. *TMS320C6000 DSP/BIOS User's Guide* (SPRU303).
17. *TMS320C6000 DSP/BIOS Application Programming Interface (API) Reference Guide* (SPRU403).
18. *TMS320 DSP Algorithm Standard Rules and Guidelines* (SPRU352).
19. *TMS320 DSP Product Family Glossary* (SPRU258).
20. *TMS320 DSP Algorithm Standard Developer's Guide* (SPRU424).

Many application reports also exist for assistance with C6411 applications. Here are just a few:

1. *Guidelines For Software Development Efficiency on the TMS320C6000 VelociTI Architecture* (SPRA434).
2. *Getting the Most Performance When Porting TMS320C62x Code to the TMS320C64x Platform* (SPRA678).
3. *Reed Solomon Decoder: TMS320C64x Implementation* (SPRA686).
4. *Cache Usage in High Performance DSP Applications with the TMS320C64x* (SPRA756).
5. *TMS320C6414/15/16 Power Consumption Summary* (SPRA811).
6. *TMS320C6411 Power Consumption Summary* (SPRA373).
7. *TMS320C6000 EMIF-to-External SDRAM Interface* (SPRA433).
8. *TMS320C6000 BGA Manufacturing Considerations* (SPRA429).
9. *TMS320C6000 Board Design: Considerations for Debug* (SPRA523).
10. *TMS320C6x Thermal Design Considerations* (SPRA432).
11. *Using the TMS320C6000 McBSP as a High Speed Communication Port* (SPRA455).
12. *TMS320C6000 Simulator User's Guide* (SPRU546).

For more information, see the TI web site at http://www.ti.com

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265