EVM Application #2

Creating a Sine Modulated PWM Signal Using the TMS320F240 EVM

APPLICATION REPORT: SPRA411

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Abstract

This document describes the EVM Application #2, which generates an asymmetrical pulse width modulated (PWM) signal with a varying duty cycle. This application is implemented using C2xx Assembly code. Included in this document are:

- Modules used
- Input and output information
- Background information on how the sine wave is implemented and generated
- Code used with the target system, the Texas Instruments (TI™) TMS320F240 Evaluation Module (EVM)

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *Digital Signal Processing Applications with the TMS320 Family: Theory, Algorithms, and Implementations Volume 1*, Literature number SPRA012A

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Overview

This application generates an asymmetrical pulse width modulated (PWM) signal with a varying duty cycle. The period of the PWM signal is 0.05ms, which is equivalent to a 20kHz signal. The duty cycle is modulated with a sine function that can be varied in frequency. The implementation of the sine wave modulation is through a look-up table. This application is implemented using C2xx Assembly code. The algorithm described in this application report was implemented using the TI TMS320F240 EVM.

Module(s) Used

- Event Manager Module
- General Purpose Timer 1

Input

None

Output

T1PWM / T1CMP

Background and Methodology

The implementation of the sine wave modulated PWM signal is simply a modification of Application #1 (PWM0.ASM) except that the compare registers are modified periodically instead of being held constant.

The generation of the sine wave is performed using a look up table. To be able to control the frequency of the modulation with some accuracy, a method based on the modulo mathematical operation is used (i.e. any overflow is disregarded and only the remainder is kept)[1].

In this application a 16-bit counter is used to determine the location of the next value. A step value is added to the counter every time a new value from the sine table is to be loaded. By changing the value of the step, one can accurately control the frequency of the sine wave.

Although a 16-bit counter is used, the upper byte determines the location of the next sine value to be used; thus, by changing how quickly values overflow from the lower byte (i.e., manipulating the step value), the frequency of the sine wave can be changed. The modulo mathematical operation is used when there is overflow in the accumulator from the lower word to the upper word. When an overflow occurs, only the remainder (lower word) is stored.

For example, the counter is set to 0000h and the step value is set to 40h. Every time a value is to be looked up in the table, the value 40h is added to the counter; however, since the upper byte is used as the pointer on the look up table, the first, second, and third values will point to the same location. In the fourth step, which results in an overflow into the upper byte, the value that is loaded will change. Since the upper byte is used as the pointer, the look-up table has 256 values, which is equivalent to the number of possibilities for an 8-bit number: 0 to 255. Additionally, since the upper word of the accumulator is disregarded, the pointer for the sine look up table does not need to be reset.

[1] For more information reference the Texas Instruments application note, *Digital Signal Processing Applications with the TMS320 Family: Theory, Algorithms, and Implementations Volume 1*, literature number SPRA012A.

Table 1. Look-Up Table Example 1

Step	Accumulator	Counter	Pointer	Step Value = 40h
0	0000 0000h	0000h	00h	1st value of sine table
1	0000 0040h	0040h	00h	
2	0000 0080h	0080h	00h	
3	0000 00C0h	00C0h	00h	
4	0000 0100h	0100h	01h	2nd value of sine table
•	•	•		•
•	•	•		•
•	•	•		•
n	0000 FFC0h	FFC0h	FFh	256th value of sine table
n+1	0001 0000h	0000h	00h	1st value of sine table
n+2	0000 0040h	0040h	00h	

The step size controls the frequency that is output; as a result, the larger the step, the quicker the overflow into the upper byte, and the faster the pointer traverses through the sine look-up table.

Table 2. Look-Up Table Example 2

Step	Counter	Pointer	Step Value = C0h
0	0000h	00h	1st value of sine table
1	00C0h	00h	
2	0180h	01h	2nd value of sine table
3	0240h	02h	3rd value of sine table
4	0300h	03h	4th value of sine table

Although the step size indicates how quickly the pointer moves through the look up table, the step size does not provide much information about the approximate frequency that the sine wave will be modulating the PWM signal. To determine the frequency of the sine wave, determine how often the value in the compare register will be modified.

In this application, the routine to load a new value in the compare register is accessed every time that the timer value matches the value in the period register. Consequently, the routine will be accessed at the same frequency as the PWM signal (20kHz). Because the compare register will be updated each time that the period register and the timer values are equal, the routine that modifies the compare register will be implemented as an interrupt service routine. As a result, the proper registers, EVIMRA and the core IMR need to unmask the proper interrupt levels so that the compare register can be updated.

The frequency that the sine wave will be modulated at can be calculated from the following formula

$$f(step) = \frac{step}{T_S \times 2^n}$$

where:

f(step) = desired frequency

T_S = the time period between each update (in this case, the PWM period)

n = the number of bits in the counter register

step = the step size used

The frequency that the PWM signal will be modulated is proportional to the step size and inversely proportional to the size of the counter register and the period at which the routine is accessed. Thus, to increase the resolution that one can increment or decrement the frequency of the PWM modulation, one needs to have a larger counting register or access the routine at a slower frequency by increasing the period.

Since this program is interrupt driven, once the registers have been set for the PWM signal, the program can be ended with an unconditional branch and the output will continue because of the interrupt structure. The output will stop when the user halts the program or the software masks the corresponding interrupt levels.

Adding the following watch in the debugger environment

wa *FREQSTEP,,u

will allow one to modify the step size to change the frequency of modulation.

```
;*****************************************************************
; File Name:     pwm1.asm
; Originator:    Digital Control systems Apps group - Houston
; Target System: 'C240 Evaluation Board
;
; Description:   Pulse Width Modulator - Sets up the registers
;                for an asymmetric PWM output.  The output is a
;                square wave with a sine wave modulated duty cycle.
;                PWM Period is 0.05ms => 20kHz
;
;                Entering the command
;                   wa *FREQSTEP,,u
;                Allows one to change the step size to change
;                the frequency in the debugger environment
;
; Last Updated:  20 June 1997
;
;*****************************************************************
                   .include f240regs.h

;-----------------------------------------------------------------
; Vector address declarations
;-----------------------------------------------------------------
                   .sect ".vectors"

RSVECT           B    START    ; Reset Vector
INT1             B    PHANTOM  ; Interrupt Level 1
INT2             B    SINE     ; Interrupt Level 2
INT3             B    PHANTOM  ; Interrupt Level 3
INT4             B    PHANTOM  ; Interrupt Level 4
INT5             B    PHANTOM  ; Interrupt Level 5
INT6             B    PHANTOM  ; Interrupt Level 6
RESERVED         B    PHANTOM  ; Reserved
SW_INT8          B    PHANTOM  ; User S/W Interrupt
SW_INT9          B    PHANTOM  ; User S/W Interrupt
SW_INT10         B    PHANTOM  ; User S/W Interrupt
SW_INT11         B    PHANTOM  ; User S/W Interrupt
SW_INT12         B    PHANTOM  ; User S/W Interrupt
SW_INT13         B    PHANTOM  ; User S/W Interrupt
SW_INT14         B    PHANTOM  ; User S/W Interrupt
SW_INT15         B    PHANTOM  ; User S/W Interrupt
SW_INT16         B    PHANTOM  ; User S/W Interrupt
TRAP             B    PHANTOM  ; Trap vector
NMINT            B    PHANTOM  ; Non-maskable Interrupt
EMU_TRAP         B    PHANTOM  ; Emulator Trap
SW_INT20         B    PHANTOM  ; User S/W Interrupt
SW_INT21         B    PHANTOM  ; User S/W Interrupt
SW_INT22         B    PHANTOM  ; User S/W Interrupt
SW_INT23         B    PHANTOM  ; User S/W Interrupt
```

```
;=====================================================================
; M A I N   C O D E  - starts here
;=====================================================================
                .text
                NOP
START:    SETC  INTM            ;Disable interrupts
                SPLK  #0002h,IMR ;Mask all core interrupts
                                 ; except INT2

                LACC  IFR        ;Read Interrupt flags
                SACL  IFR        ;Clear all interrupt flags

                CLRC  SXM        ;Clear Sign Extension Mode
                CLRC  OVM        ;Reset Overflow Mode
                CLRC  CNF        ;Config Block B0 to Data mem

;-----------------------------------
; Set up PLL Module
;-----------------------------------
                LDP   #00E0h

;The following line is necessary if a previous program set the PLL
;to a different ;setting than the settings which the application
;uses.  By disabling the PLL, the CKCR1 register can be modified so
;that the PLL can run at the new settings when it is re-enabled.

                SPLK  #0000000001000001b,CKCR0 ;CLKMD=PLL Disable
                                               ;SYSCLK=CPUCLK/2

;                      5432109876543210
                SPLK  #0000000010111011b,CKCR1
                                ;CLKIN(OSC)=10MHz,CPUCLK=20MHz

;CKCR1 - Clock Control Register 1
;   Bits 7-4     (1011)  CKINF(3)-CKINF(0) - Crystal or Clock-In
;                           Frequency
;                           Frequency = 10MHz
;   Bit 3        (1)   PLLDIV(2) - PLL divide by 2 bit
;                           Divide PLL input by 2
;   Bits 2-0     (011) PLLFB(2)-PLLFB(0) - PLL multiplication ratio
;                           PLL Multiplication Ration = 4

;                      5432109876543210
                SPLK  #0000000011000001b,CKCR0 ;CLKMD=PLL Enable
                                               ;SYSCLK=CPUCLK/2

;CKCR0 - Clock Control Register 0
;   Bits 7-6     (11)  CLKMD(1),CLKMD(0) - Operational mode of
;                           Clock Module
;                           PLL Enabled; Run on CLKIN on exiting low
;                           power mode
;   Bits 5-4     (00)  PLLOCK(1),PLLOCK(0) - PLL Status.
```

```
;                               READ ONLY
;   Bits 3-2      (00)  PLLPM(1),PLLPM(0) - Low Power Mode
;                               LPM0
;   Bit 1         (0)   ACLKENA - 1MHz ACLK Enable
;                               ACLK Disabled
;   Bit 0         (1)   PLLPS - System Clock Prescale Value
;                               f(sysclk)=f(cpuclk)/2


;                        5432109876543210
                  SPLK  #0100000011000000b,SYSCR ;CLKOUT=CPUCLK

;SYSCR - System Control Register
;   Bit 15-14     (01)  RESET1,RESET0 - Software Reset Bits
;                               No Action
;   Bits 13-8     (000000) Reserved
;   Bit 7-6       (11)  CLKSRC1,CLKSRC0 - CLKOUT-Pin Source
;                               Select
;                               CPUCLK: CPU clock output mode
;   Bit 5-0       (000000)Reserved


                  SPLK  #006Fh, WDCR  ;Disable WD if VCCP=5V
                                      ;(JP5 in pos. 2-3)
                  KICK_DOG                ;Reset Watchdog

;-------------------------------------
; Set up Digital I/O Port
;-------------------------------------
                  LDP   #225  ;DP=225, Data Page to Configure OCRA
;                        5432109876543210
                  SPLK  #0011100000000000b,OCRA

;OCRA  - Output Control Register A
;   Bit 15        (0)   CRA.15 - IOPB7
;   Bit 14        (0)   CRA.14 - IOPB6
;   Bit 13        (1)   CRA.13 - T3PWM/T3CMP
;   Bit 12        (1)   CRA.12 - T2PWM/T2CMP
;   Bit 11        (1)   CRA.11 - T1PWM/T1CMP
;   Bit 10        (0)   CRA.10 - IOPB2
;   Bit 9         (0)   CRA.9 - IOPB1
;   Bit 8         (0)   CRA.8 - IOPB0
;   Bits 7-4      (0000)   Reserved
;   Bit 3         (0)   CRA.3 - IOPA3
;   Bit 2         (0)   CRA.2 - IOPA2
;   Bit 1         (0)   CRA.1 - IOPA1
;   Bit 0         (0)   CRA.0 - IOPA0


;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
;- Event Manager Module Reset
;*
```

```
;-   This section resets all of the Event Manager Module Registers.
;*   This is necessary for silicon revision 1.1; however, for
;-   silicon revisions 2.0 and later, this is not necessary
;*
;-
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*

   LDP           #232       ;DP=232 Data Page for the Event Manager
   SPLK          #0000h,GPTCON ;Clear General Purpose Timer Control
   SPLK          #0000h,T1CON  ;Clear GP Timer 1 Control
   SPLK          #0000h,T2CON  ;Clear GP Timer 2 Control
   SPLK          #0000h,T3CON  ;Clear GP Timer 3 Control
   SPLK          #0000h,COMCON ;Clear Compare Control
   SPLK          #0000h,ACTR
                       ;Clear Full Compare Action Control Register
   SPLK          #0000h,SACTR
                       ;Clear Simple Compare Action Control Register
   SPLK          #0000h,DBTCON
                       ;Clear Dead-Band Timer Control Register

   SPLK          #0000h,CAPCON ;Clear Capture Control

   SPLK          #0FFFFh,EVIFRA;Clear Interrupt Flag Register A
   SPLK          #0FFFFh,EVIFRB;Clear Interrupt Flag Register B
   SPLK          #0FFFFh,EVIFRC;Clear Interrupt Flag Register C

   SPLK          #0000h,EVIMRA ;Clear Event Manager Mask Register A
   SPLK          #0000h,EVIMRB ;Clear Event Manager Mask Register B
   SPLK          #0000h,EVIMRC ;Clear Event Manager Mask Register C

;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
;-               End of RESET section for silicon revision 1.1    *
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*

;-----------------------------------
; Set up Event Manager Module
;-----------------------------------

T1COMPARE       .set  0          ; T1Compare Initialized to 0
T1PERIOD        .set  1000       ; T1Period Initialized to
                                 ;1000 = 20kHz value

                .text
                LDP   #232       ;DP=232, Data Page for
                                 ;Event Manager Addresses

                SPLK  #T1COMPARE,T1CMPR;T1CMPR = 0

;                      2109876543210
                SPLK  #0000001010101b,GPTCON

;GPTCON - GP Timer Control Register
```

```
;   Bit 15       (0)   T3STAT - GP Timer 3 Status.  READ ONLY
;   Bit 14       (0)   T2STAT - GP Timer 2 Status.  READ ONLY
;   Bit 13       (0)   T1STAT - GP Timer 1 Status.  READ ONLY
;   Bits 12-11   (00)  T3TOADC - ADC start by event of GP Timer 3
;                         No event starts ADC
;   Bits 10-9    (00)  T2TOADC - ADC start by event of GP Timer 2
;                         No event starts ADC
;   Bits 8-7     (00)  T1TOADC - ADC start by event of GP Timer 1
;                         No event starts ADC
;   Bit 6        (1)   TCOMPOE - Compare output enable
;                         Enable all three GP timer compare outputs
;   Bits 5-4     (01)  T3PIN - Polarity of GP Timer 3 compare
;                         output
;                         Active Low
;   Bits 3-2     (01)  T2PIN - Polarity of GP Timer 2 compare
;                         output
;                         Active Low
;   Bits 1-0     (01)  T1PIN - Polarity of GP Timer 1 compare
;                         output
;                         Active Low

                SPLK  #T1PERIOD,T1PR   ; T1PR = 1000
                SPLK  #0000h,T1CNT     ; Initialize Timer 1
                SPLK  #0000h,T2CNT     ; Initialize Timer 2
                SPLK  #0000h,T3CNT     ; Initialize Timer 3


;                      5432109876543210
                SPLK  #0001000000000110b,T1CON

;T1CON - GP Timer 1 Control Register
;   Bits 15-14   (00)  FREE,SOFT - Emulation Control Bits
;                         Stop immediately on emulation suspend
;   Bits 13-11   (010) TMODE2-TMODE0 - Count Mode Selection
;                         Continuous-Up Count Mode
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                         Divide by 1
;   Bit 7        (0)   Reserved
;   Bit 6        (0)   TENABLE - Timer Enable
;                         Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                         Internal Clock Source
;   Bits 3-2     (01)  TCLD1,TCLD0 - Timer Compare Register
;                         Reload Condition
;                         When counter is 0 or equals period
;                         register value
;   Bit 1        (1)   TECMPR - Timer compare enable
;                         Enable timer compare operation
;   Bit 0        (0)   Reserved

;                      5432109876543210
                SPLK  #0000000000000000b,T2CON ;Not used
```

```
;T2CON - GP Timer 2 Control Register
;   Bits 15-14   (00)  FREE,SOFT - Emulation Control Bits
;                         Stop immediately on emulation suspend
;   Bits 13-11   (000) TMODE2-TMODE0 - Count Mode Selection
;                         Stop/Hold
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                         Divide by 1
;   Bit 7        (0)   TSWT1 - GP Timer 1 timer enable bit
;                         Use own TENABLE bit
;   Bit 6        (0)   TENABLE - Timer Enable
;                         Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                         Internal Clock Source
;   Bits 3-2     (00)  TCLD1,TCLD0 - Timer Compare Register
;                         Reload Condition When counter is 0
;   Bit 1        (0)   TECMPR - Timer compare enable
;                         Disable timer compare operation
;   Bit 0        (0)   SELT1PR - Period Register select
;                         Use own period register

;                       5432109876543210
                SPLK  #0000000000000000b,T3CON  ;Not Used

;T3CON - GP Timer 3 Control Register
;   Bits 15-14   (00)  FREE,SOFT - Emulation Control Bits
;                         Stop immediately on emulation suspend
;   Bits 13-11   (000) TMODE2-TMODE0 - Count Mode Selection
;                            Stop/Hold
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                            Divide by 1
;   Bit 7        (0)   TSWT1 - GP Timer 1 timer enable bit
;                         Use own TENABLE bit
;   Bit 6        (0)   TENABLE - Timer Enable
;                         Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                         Internal Clock Source
;   Bits 3-2     (00)  TCLD1,TCLD0 - Timer Compare Register
;                         Reload Condition When counter is 0
;   Bit 1        (0)   TECMPR - Timer compare enable
;                         Disable timer compare operation
;   Bit 0        (0)   SELT1PR - Period Register select
;                         Use own period register

                SBIT1 T1CON,B6_MSK     ;Sets Bit 6 of T1CON

;T1CON - GP Timer 1 Control Register
;   Bit 6        (1)   TENABLE - Timer Enable
;                         Enable Timer Operations

         SPLK    #0FFFFh,EVIFRA   ;Clear all pending interrupts
         SPLK    #0080h,EVIMRA    ;Enable Timer 1 Period Interrupt
```

```
;-----------------------------------
; Generate Sine Wave Modulated PWM
;-----------------------------------

                .bss  TABLE,1     ;Keeps address of the pointer in
                                  ;the SINE Table
                .bss  TOPTABLE,1  ;Keeps the reset value for the
                                  ;pointer
                .bss  COMPARET1,1 ;A register to do calculations
                                  ;since the
                                  ;T1CMPR register is double
                                  ;buffered
                .bss  FREQSTEP,1  ;Frequency modulation of the sine
                                  ;wave
                .bss  MODREG,1    ;Rolling Modulo Register
                .bss  SINEVAL,1   ;Value from look up table

NORMAL .set     500

                .text

                LDP   #0               ;DP = 0
                SPLK  #0000h,TABLE     ;Initialize Pointer to Top
                SPLK  #STABLE,TOPTABLE ;Initialize TOPTABLE to
                                       ; address of sine table
                SPLK  #4,FREQSTEP      ;Set the step size to 4
                SPLK  #0000h,MODREG    ;Initialize the 16 bit
                                       ; counter register

                CLRC  INTM          ;Enable interrupts

END             B  END              ;End of Program

;-----------------------------------------------------------------------
; Generate PWM Sine Wave ISR
;-----------------------------------------------------------------------

SINE            LDP   #0          ; DP = 0
                LACC  MODREG      ; ACC = 16 bit Counter Register
                ADD   FREQSTEP    ; ACC = Counter + Step
                SACL  MODREG      ; Counter assigned new value
                LACC  MODREG,8    ; ACC = Counter shifted to left
                                  ; by 8
                SACH  TABLE       ; TABLE = upper byte of
                                  ; counter = pointer
                LACC  TABLE       ; ACC = TABLE = Pointer
                ADD   TOPTABLE    ; Offset Addr from top of table
                TBLR  SINEVAL     ; Read sine value and store to
                                  ; SINEVAL
```

```
;Normalization of the Sine value to prevent the compare value from
; being negative

   LT            SINEVAL       ; TREG = SINEVAL (Q15)
   MPY           #NORMAL       ; PREG = TREG * NORMAL (Q30)
                               ; NORMAL = T/2
   PAC                         ; ACC = PREG (Q30)
   SACH          COMPARET1,1   ; COMPARET1 = PREG (Q15)
   LACC          COMPARET1     ; ACC = COMPARET1
   ADD           #NORMAL       ; ACC = COMPARET1 + NORMAL

   LDP           #232          ; DP = 232
   SACL          T1CMPR        ; T1CMPR = ACC = Normalize Sine
                               ; Value

;Clear the interrupt flags of the Event Manager Module

   LACC          EVIFRA        ; ACC = EVIFRA
   SACL          EVIFRA        ; EVIFRA = ACC; resets the
                               ; interrupt flag
   CLRC          INTM          ; Enable core interrupts
   RET                         ; Return to end of program
```

```
;---------------------------------------------------------------------
; Sine look-up table
; No. Entries     : 256
; Angle Range     : 360 deg
; Number format   : Q15 with range -1 < N < +1
;---------------------------------------------------------------------
                ;SINVAL      ;        Index       Angle  Sin(Angle)
STABLE  .word      0         ;          0           0     0.0000
        .word    804         ;          1        1.41     0.0245
        .word   1608         ;          2        2.81     0.0491
        .word   2410         ;          3        4.22     0.0736
        .word   3212         ;          4        5.63     0.0980
        .word   4011         ;          5        7.03     0.1224
        .word   4808         ;          6        8.44     0.1467
        .word   5602         ;          7        9.84     0.1710
        .word   6393         ;          8       11.25     0.1951
        .word   7179         ;          9       12.66     0.2191
        .word   7962         ;         10       14.06     0.2430
        .word   8739         ;         11       15.47     0.2667
        .word   9512         ;         12       16.88     0.2903
        .word   10278        ;         13       18.28     0.3137
        .word   11039        ;         14       19.69     0.3369
        .word   11793        ;         15       21.09     0.3599
        .word   12539        ;         16       22.50     0.3827
        .word   13279        ;         17       23.91     0.4052
        .word   14010        ;         18       25.31     0.4276
        .word   14732        ;         19       26.72     0.4496
        .word   15446        ;         20       28.13     0.4714
        .word   16151        ;         21       29.53     0.4929
        .word   16846        ;         22       30.94     0.5141
        .word   17530        ;         23       32.34     0.5350
        .word   18204        ;         24       33.75     0.5556
        .word   18868        ;         25       35.16     0.5758
        .word   19519        ;         26       36.56     0.5957
        .word   20159        ;         27       37.97     0.6152
        .word   20787        ;         28       39.38     0.6344
        .word   21403        ;         29       40.78     0.6532
        .word   22005        ;         30       42.19     0.6716
        .word   22594        ;         31       43.59     0.6895
        .word   23170        ;         32       45.00     0.7071
        .word   23731        ;         33       46.41     0.7242
        .word   24279        ;         34       47.81     0.7410
        .word   24811        ;         35       49.22     0.7572
        .word   25329        ;         36       50.63     0.7730
        .word   25832        ;         37       52.03     0.7883
        .word   26319        ;         38       53.44     0.8032
        .word   26790        ;         39       54.84     0.8176
        .word   27245        ;         40       56.25     0.8315
        .word   27683        ;         41       57.66     0.8449
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;=====================================================================
; I S R  -  PHANTOM
;
; Description:   Dummy ISR, used to trap spurious interrupts.
;
; Modifies:      Nothing
;
; Last Update:   16 June 95
;=====================================================================
PHANTOM          KICK_DOG         ;Resets WD counter
                 B  PHANTOM
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