Application Report
SPRA470

Introduction to the TMS320VC5410

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ABSTRACT

The TMS320VC5410 is a high performance, highly integrated member of TI's growing 'C54x product line. The 'VC5410 delivers 80 or 100 MIPS performance with a 2.5V core power supply (I/O voltage remains at 3.3V). The 'VC5410 devices provide 64K words of on-chip SRAM, 16K words of on-chip ROM, 3 multi-channel buffered serial ports, a host port interface, and a timer. The 'C5410 was developed to service a variety of end-equipment in the wireless and wireline communications market that require high performance, very low power dissipation, and small physical size.

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TMS320C54x Architectural Overview

The TMS320C54x offers some of the most efficient MIPS in the industry with up to 40% higher quality MIPS in relation to other 16-bit DSPs and comparable MIPS efficiency to 24-bit instruction DSPs. There are several reasons behind this. The combination of an enhanced Harvard architecture, parallel bus structure, and optimized core empowers a sophisticated instruction set, with many single cycle and parallel instructions.

Parallelism of the CPU is readily evident by inspection of the 'C54x internal hardware. The CPU employs a non-pipelined MAC (multiply accumulate) unit with a 17x17 multiplier and a dedicated adder. In addition, a 40-bit ALU can perform various arithmetic or bit manipulation functions with the output connected to dual 40-bit accumulators. In general, multiple accumulators can contribute to improved coding efficiency by avoiding storage of intermediate results to memory. More importantly though, a particular advantage of this feature is made by several of the signal processing instructions in which two accumulators function as destination registers for concurrent operations. For example, the square distance instruction (SQDST) uses the B accumulator as the destination for a vector difference calculation while the A accumulator keeps a running sum of prior differences.

Equally important as the CPU parallelism is having bus bandwidth to support multiple memory operands. The 'C54x has 4 sets of internal buses which can support 1 program fetch, 2 data memory reads, and 1 data memory write in a single cycle.

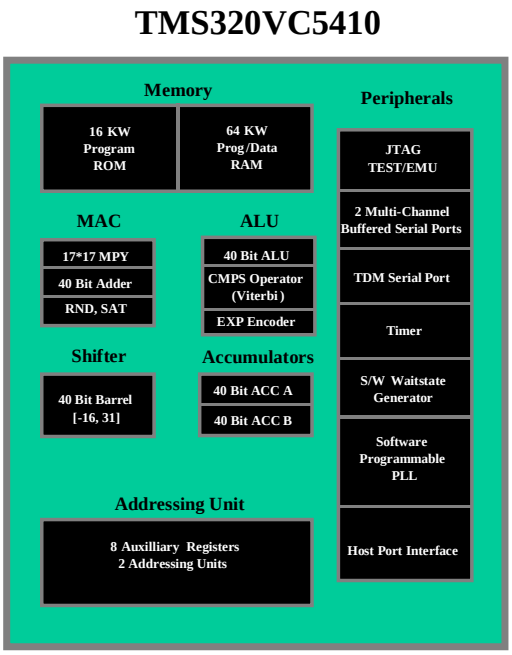
Other core highlights include:

- Split mode ALU which facilitates single cycle 32 bit sum or dual 16-bit sums (this feature is extremely useful in Viterbi decoder ACS butterfly calculations).
- H/W exponent detector which allows single cycle exponent encoding and single cycle mantissa normalization (this feature is useful in many vocoder applications).
- Non-pipelined MAC unit supporting single cycle 17-bit unsigned or 16-bit signed multiplication with or without rounding (rounding feature is advantageous for GSM applications).
- General purpose Compare, Select & Store Unit to facilitate Viterbi channel decode or MLSE equalization ACS butterfly calculations
- Software stack implemented by Stack Pointer register (SP)
- Industry's most efficient fixed-point C Compiler may be used to speed development of less time critical functions.
- Extensive interrupt support in the form of 4 prioritized external interrupts, one non-maskable interrupt, and one reset interrupt. Interrupt processing is

directed by a software interrupt vector table and interrupts can be nested to any depth.

Figure 1 shows the block diagram for the TMS320VC5410

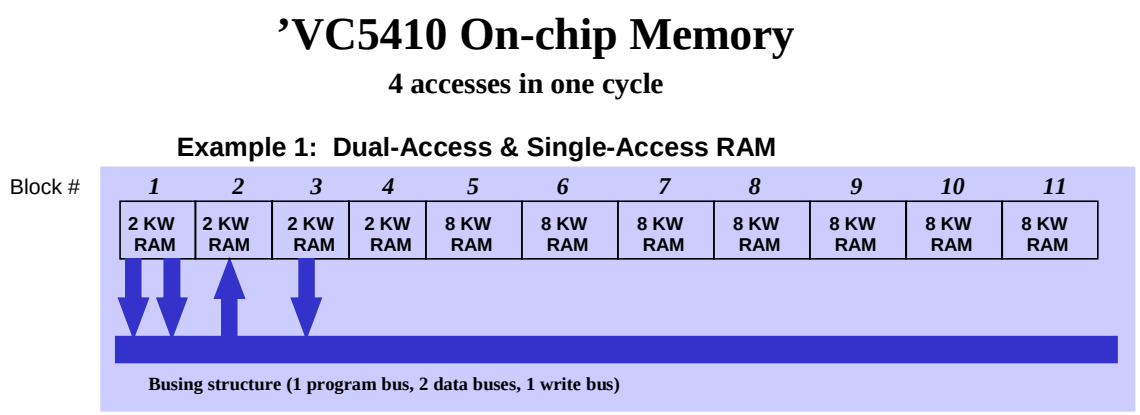
’C5410: Increasing on-chip integration



- **TMS320C54x CPU @ 100 MIPS**
- **Core Voltage: 2.5V**
- **16K x 16 bit Single Access On-chip ROM with boot code**
- **64K words of on-chip SRAM consisting of:**
  - ***8K x 16 bit Dual Access On-chip Program/Data RAM***
  - ***56K x 16 bit Single Access On-chip Program/Data RAM***
- ***3 Multi-Channel Buffered Serial Ports w/ DMA***
- ***Host Port Interface w/ DMA controller***
- **Timer**
- **Extended Program Addressing**
- **Software Programmable PLL**
- **Low Active Mode Power Dissipation**
- **JTAG with Boundary Scan**
- **144-pin TQFP or 176 u*BGA; footprint compatible with the 548 or 549 (with 144-pin TQFP)**

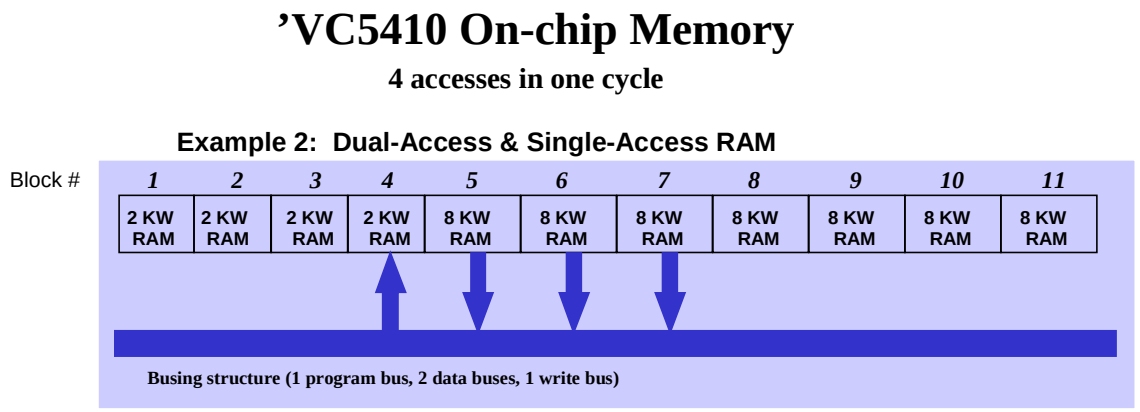
The ’VC5410 at 2.5V is a very high performance 16-bit DSPs with a large integration of on-chip memory and peripherals. As you can see from figure 1, the ’VC5410 has 64K words of on-chip RAM. 8K words of this is dual-access RAM (broken into four 2K word blocks) and 56K words is single-access RAM (broken into seven 8K word blocks). This memory integration, in conjunction with the advanced busing structure, allows 4 accesses in one cycle. The following two diagrams display just a couple of the numerous possibilities of the ’C5410 architecture. Blocks 1,2,3, and 4 can each support 2 accesses in a single instruction cycle. Blocks 5,6, 7, 8, 9, 10, and 11 are 8K word blocks that allow 1 access per instruction cycle.

Figure 2



- 64K words total on-chip
- 1 program fetch from block 3
- 2 data reads from block 1
- 1 data write into block 2

Figure 3



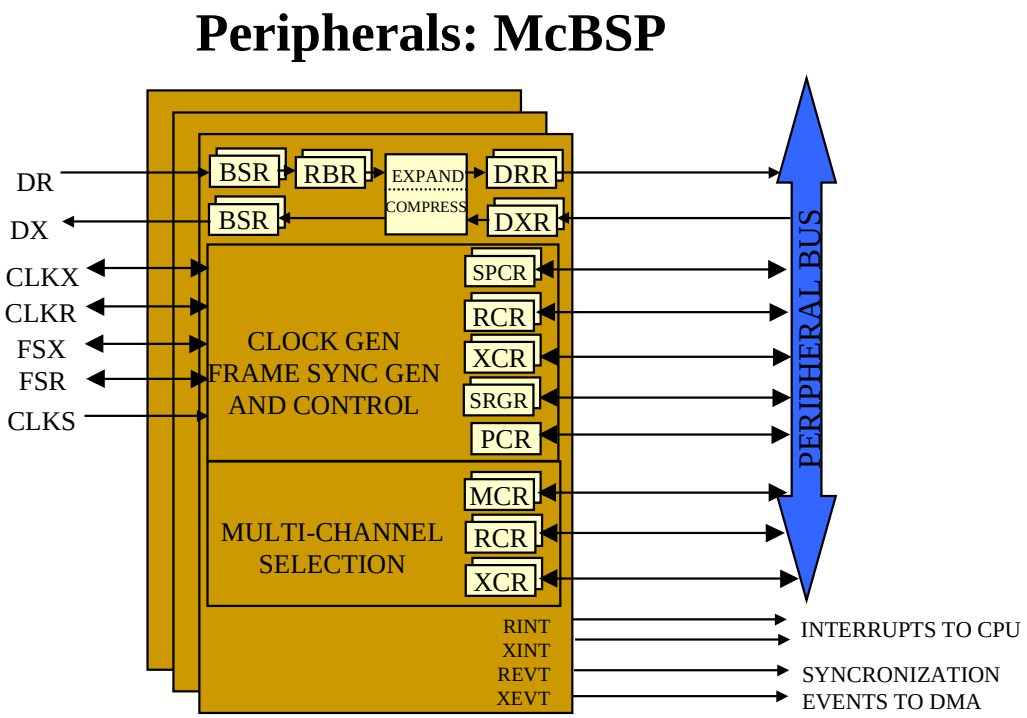
- 64K words total on-chip
- 1 program fetch from block 7
- 1 data read from block 5
- 1 data read from block 6
- 1 data write into block 4

The previous examples are only a couple of the possibilities of utilizing the on-chip memory of the 'VC5410. It is important to note from the busing and memory examples above that the 'VC5410 does not suffer from the bandwidth problems that would affect many other architectures.

Up to this point, this document has shown how the core architecture of the 'C54x, the busing structure, and the large on-chip memory all collaborate to enable the '5410's high quality of MIPS. A discussion on MIPS quality would not be

complete without the inclusion of the peripheral set. The ’VC5410 peripherals also greatly enhance MIPS quality.

Figure 4



The TMS320VC5410 has three multi-channel buffered serial ports (McBSPs). The diagram above describes the components of one of the three McBSPs. Each McBSP provides direct communication with T1/E1 framers, serial A/D converters, codecs, and other serial devices with minimal hardware requirements. The McBSP is a high speed, full-duplex, serial port interface that offers programmable frame generation, internal clock, and polarity for both frame synchronization and data clocks. Multi-channel selection gives the McBSP the capability to transmit and receive up to 128 channels. Because the McBSP has access to data, program, and I/O memory spaces, data can be directly written to or read from memory. This provides increased flexibility, improved data rates, and an unburdened CPU. The McBSP contains an on-chip companding hardware feature that allows the compression or expansion of data in either A-law or u-law formats. As a result, code size is reduced by not having to reference look-up tables or perform companding equations in software. The throughput of the McBSP is 50 Mbits/sec for a ’VC5410 running at 100 MIPS. Because the McBSP operates independently of the CPU, the CPU can actually be placed into an IDLE mode while the McBSP continues to operate and spool data into or out of on-chip memory.

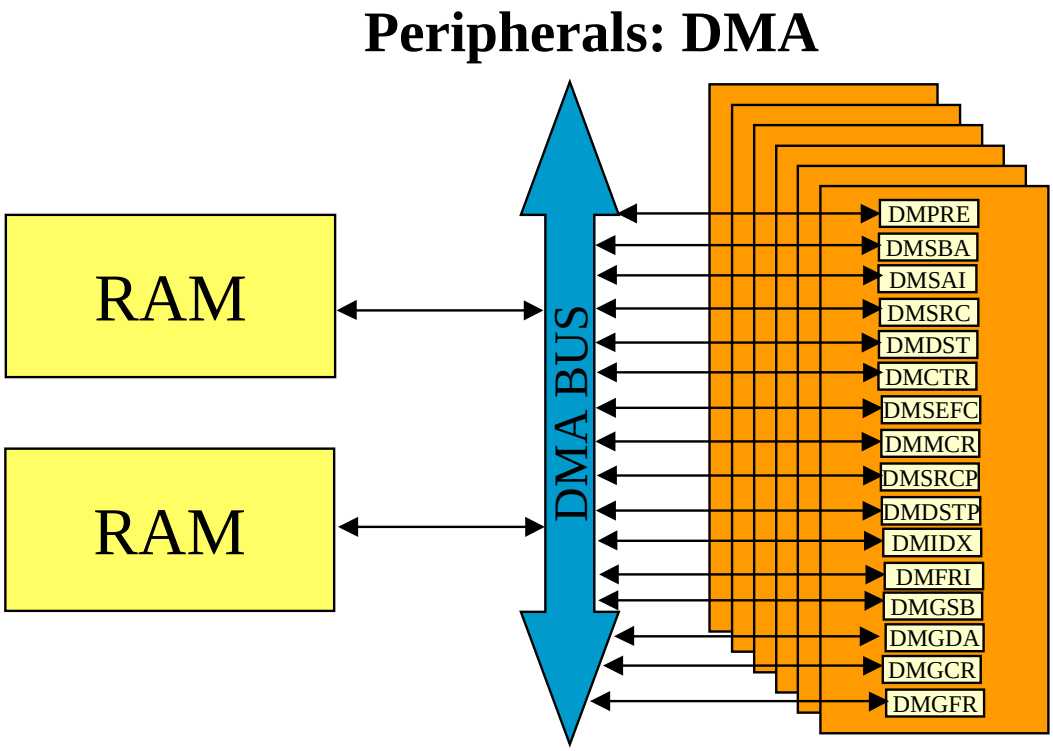


Figure 5

The ’LC5410 Direct Memory Access (DMA) controller allows movements of data between internal program and data memory, internal peripherals (e.g. McBSP), or external memory devices to occur without intervention by the CPU. With six independent programmable channels, the DMA has the ability to keep track of the contexts of six independent block transfers.

The Host Port Interface (HPI) is an 8 line parallel bus that is used to interface to a host processor (for example a microcontroller). The DMA bus allows information to be exchanged between the DSP device and the host processor throughout the entire on-chip memory. The extended on-chip program memory is also accessible by host and DSP. The HPI can operate in two modes: shared access mode (SAM) or host-only mode (HOM). In SAM mode, both the host and the ’VC5410 can access memory with asynchronous host accesses being resynchronized internally. If a conflict occurs, the CPU will wait. In this mode, the transfer rate is 64 Mbits/sec (or 8 Mbytes/sec). In the HOM mode, the transfer rate for the HPI is 160 Mbits/sec (or 20 Mbytes/sec).

Other peripherals on the ’VC5410:

- Standard 16-bit timer

- Wait State Generator: extends the external bus cycles up to 7. It is fully software programmable in order to interface to slower external memories
- Phase Locked Loop (PLL): The PLL allows the ’VC5410 to operate at a high on-chip frequency with a lower external frequency clock. The PLL is software programmable and has 31 different multiplier options ranging from x1/4 to x15.

Applications:

A useful way of segmenting the applications for the ’VC5410 is to look at three basic types:

’C54x Application Types

- Single channel / high performance: a single high performance algorithm or application (e.g. 40-50 MIPS algorithm on a 50 MIPS DSP)

- Channel stacking: ability to add more “channels” of a particular algorithm on 1 DSP (e.g. 32 channels of DTMF)

- Function stacking: ability to absorb functionality of multiple dedicated processors or ASICs into 1 DSP (e.g. 1 DSP does fax, data modem, telephony, audio algorithms simultaneously)

Often times, a processor’s MIPS numbers represent its “peak” performance. This is the performance of the processor given that all buses are used adequately, instructions and operands are in the correct memory locations, and slower off-chip accesses are minimized. Any instances of bus contention, memory bottlenecks, or ineffectual external accesses serve to decrease a processor’s quoted “peak” MIPS number. The resulting MIPS number becomes a more realistic measure of a processor’s “sustained” performance. Because of the very high quality of MIPS on the ’VC5410, the “peak” performance MIPS numbers and the “sustained” performance MIPS numbers are nearly identical. This makes the ’VC5410 an excellent DSP for performance enabling applications. These are applications where increased MIPS, larger amounts of on-chip memory, and intelligent peripherals are necessary to handle high performance applications in the wireless and wireline communications segments.

Channel stacking is a concept of adding more “channels” of a particular algorithm that was previously performed on multiple processors. Server line cards and telecom switching equipment are examples where many channels of relatively simple algorithms (DTMF, echo cancellations, low level fax/modem code, etc.) can be handled by a single ’VC5410.

Function stacking is a system-cost reducing concept of combining the functionality and algorithms performed by multiple dedicated processors or ASICs into a single high performance, heavily integrated DSP, like the ’VC5410. Some applications use “fixed-function” processors that are cost-effective at handling a dedicated function. However, when several of these processors are used in conjunction with ASICs or FPGAs, it starts to make sense to integrate these into a single, high-performance ’VC5410 that has the MIPS and on-chip memory to accommodate the total application. The end-result is a decrease in board size, component cost, and system power.

The ‘VC5410’s added features makes a tremendous difference in applications. Because of the added on-chip memory, power consumption is dramatically reduced. This additional memory and decrease in power will allow at least 4 channels of G.723.1 VoIP media stream signal processing to be executed on a single 100 MIPS ‘VC5410. The 5410’s McBSP has an A-bis interface that is useful in transporting data between the Base station Transceiver Station (BTS) and the Base Station Controller (BSC) in GSM infrastructures. The DMA contains registers that can handle the data-sorting function of TDM data streams like T1/E1. The figure below shows an example of data sorting a T1 data stream.

T1 Receive Data Sort

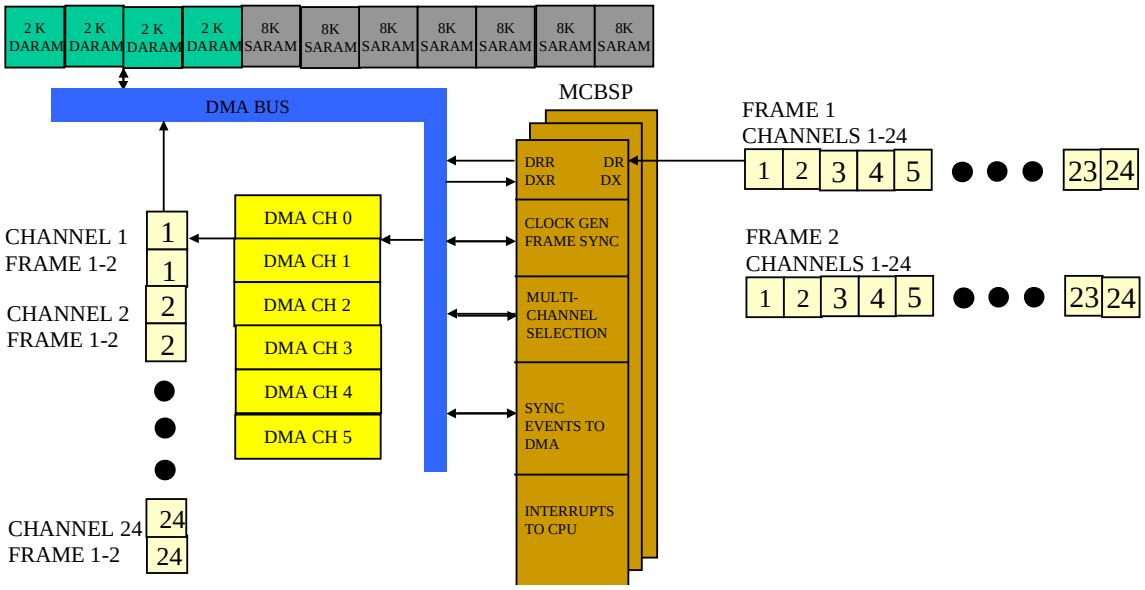


Figure 6

The ’VC5410 has 23 address lines which allow for up to 8M address range for the program space. This enables many code modules and algorithms to be stored in low-cost, external, 8-bit EPROM. Different segments of code can be stored into the 64K words of on-chip SRAM and executed at the full-speed on the processor. This “reconfigurable” concept is useful for applications that require the use of multiple algorithms that must run zero wait-state. Algorithms can be loaded into on-chip memory when needed and discarded when it becomes necessary for the next algorithm to be loaded on-chip.

Power Dissipation

One of the important design considerations for the ’VC5410 was low power dissipation. As a result, there are multiple power reducing features on the ’VC5410. Several of these are listed below:

MECHANISMS TO LOWER POWER DISSIPATION ON THE ’C54x

- **Bus Keepers / Holders -- maintain state of ext. bus**
- **External Bus off control -- disables the external bus**
- **Static design - lower clock to DC**
- **IDLE 1, 2, 3 modes -- drop into various power down modes**
- **S/W PLL (31 options on ’C5410)--use lower system clock**
- **MIPS efficiency -- fewer MIPS enables**

Active Core Power for the ’LC54x devices is, on average, .6 mA/MIPS while is is .45 mA/MIPS for ’VC54x devices.

The ’C54x incorporates 3 power down modes within its architecture: IDLE1, IDLE2, and IDLE3. These decrease power consumption when the CPU is not processing. The 3 power down modes have different degrees of power savings:

- IDLE1: core CPU shutdown, peripherals still active, 7.93 mA @ 3V/66MIPS
- IDLE2: core and peripherals shutdown, PLL still active, 2 mA @ 3V/66MIPS
- IDLE3: complete shutdown, <1 uA @ 3V/66MIPS

As the graphic shows, the ’VC5410 devices exhibit, on average, .6 mA/MIPS active core supply power. However, the true measure of power dissipation also takes into account the processor’s quality of MIPS.

THE TRUE MEASURE OF POWER DISSIPATION IS :

mA / MIPS

x

MIPS / algorithm

x

voltage

=

mW / algorithm

The typical power dissipation for ’VC5410 using on-chip resources (CPU and on-chip memory) is:

.45 mA/MIPS x 100 MIPS x 2.5V= 112.5 mW

Why is mW per function a more accurate measurement?

- mA/MIPS by itself disregards a processor’s quality of MIPS and the supply voltage
- a DSP’s power dissipation while performing the actual application or algorithm is the most accurate measurement
- if a DSP can complete a given task in fewer MIPS than another DSP, then it can get into IDLE mode sooner, thus lowering power dissipation even further.

The ’VC5410 operates with a dual power supply to achieve superior power performance. The internal logic, including the CPU and all peripheral logic, is supplied with 2.5V, while the external logic is supplied with 3.3V. The dual-power supply allows the ’VC5410 to maintain high performance at 100 MIPS, while achieving the lowest power dissipation possible.

Overall, the ’VC5410 has the high performance, large on-chip memory, and highly integrated peripheral set to meet the needs of a wide variety of wireless and wireline, data and voice, communications systems. In addition, the quality of the available MIPS and the ultra low power dissipation make the ’VC5410 a compelling choice for the ever demanding requirements of these systems.

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