

High-Density Design With MicroStar BGAs

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ABSTRACT

The consumer electronics industry constantly faces new challenges to design their solutions smaller and less expensive. One of the industry's most limiting design factors is board real estate and its increasing cost. The cost can be thought of in purely dollar terms or, more importantly, can be indirectly related to the lost revenue caused by a competitive disadvantage when the competition's solution is smaller, better and does more.

As a result, today's semiconductor, packaging and printed circuit board (PCB) manufacturing technologies make it possible to fit camcorders in the palm of your hand and cell phones in your shirt pocket. These applications require PCBs to be densely populated with components on the top and bottom sides of the board. One solution is to use CSPs (Chip Scale Packages) such as the MicroStar Ball Grid Array (MicroStar BGA™).

This application report describes a mounting technique that can increase a board's chip density, while decreasing the routing complexity associated with fine-pitch BGA packages.

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1 Introduction

For the most part, designing boards with BGA packages is not a difficult task. Designing high-density boards that maximize board space can be tricky. A common problem when designing with BGA packages is the total area required for the package and via density around the chip periphery. The total space for mounting a BGA can approach the area needed for a TQFP (Thin-Quad-Flat-Pack).

Why go through the pain of changing packages if there are no space-saving benefits? Actually, companies that have migrated to BGAs find that BGAs are not the hassle once thought. By using a few high-density techniques, the PCB designer can find that BGAs offer an opportunity for high-density boards, with the design and manufacturing ease of a TQFP.

1.1 MicroStar BGA Packages

MicroStar BGA packages are all considered fine-pitch. This application report focuses on the GGU (144-pin), GGW (176-pin), and GHH (179-pin) packages. All three packages have 0.8 mm pitch, but each is distinctly different in array style. The GGW ball array has wide channels in the four corners, providing the inner balls with space for routing and V_{CC} connectivity. See Appendix A for mechanical drawings of the MicroStar BGA packages. The GGU package has a solid four-row array configuration, and the GHH package has a solid five-row array configuration. The GGU and the GHH packages can cause difficulties when routing the inner rows.

1.2 Conductor Width/Spacing

As a general default, many of today's circuit board layouts are based on at most an 8 mil conductor (line) width and 8 mil spacing. Given the MicroStar BGA pin pitch of roughly 15 mils between ball pads, it is impossible to satisfy both line width and spacing requirements when routing between the balls. PCB manufacturers can now reduce the line width to 4 mil with 4-5 mil spacing. This allows at least one signal to be routed between ball pads. The 15 mil ball spacing is worst-case, and is calculated by assuming that the diameter of the solder ball land is 16 mils (0.41 mm).

1.3 Via Density

Via density, as mentioned previously, can be a limiting factor when designing a high-density board. *Via density* is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 1, has solved many of the problems associated with via density.

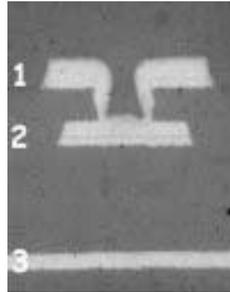


Figure 1. Laser-Drilled, 4 mil Microvia

Microvias are often created by using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4 mil thick dielectric layer, creating a 4 mil diameter microvia with a 4 mil depth (see Figure 1). The layout designer can now route to the first internal board layer. If routing to the first two layers is necessary, an 8 mil diameter microvia with an 8 mil depth can be laser-drilled by penetrating the first two layers (each 4 mil thick).

1.4 Optimal Layers

The number of board layers increases as board chip density and functional pin count increase. As an example, the TMS320VC549GGU digital signal processor (DSP) is in a 144-pin GGU package and uses 32 pins for power and ground. Roughly 112 signals can be routed on three layers. The power and ground planes increase the board thickness to five layers. The sixth layer can be used on the bottom side to place discrete components. Furthermore, by increasing the board layers, high-density applications are possible with as little as 20 mils between the chips.

Mounting two TMS320VC549 DSPs on directly opposite sides of the board is estimated to take 14 layers, assuming the sharing of VCC and ground planes. Double-sided boards will have double the functionality if a DSP is on each side. Unfortunately, the placement of bypass capacitors on power pins is required and can slightly reduce the board's overall chip density. (See section 2.3 for information on placement of bypass capacitors.)

2 Designing Vertically

The relatively large via density on the chip periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the chip, design the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 2. Mechanical drilling of 10 mil vias between the pads on the board and working vertically creates a “pick-and-choose” method – pick your layer and choose your route. A dog-bone method is used to connect the thru-hole via and the pad.

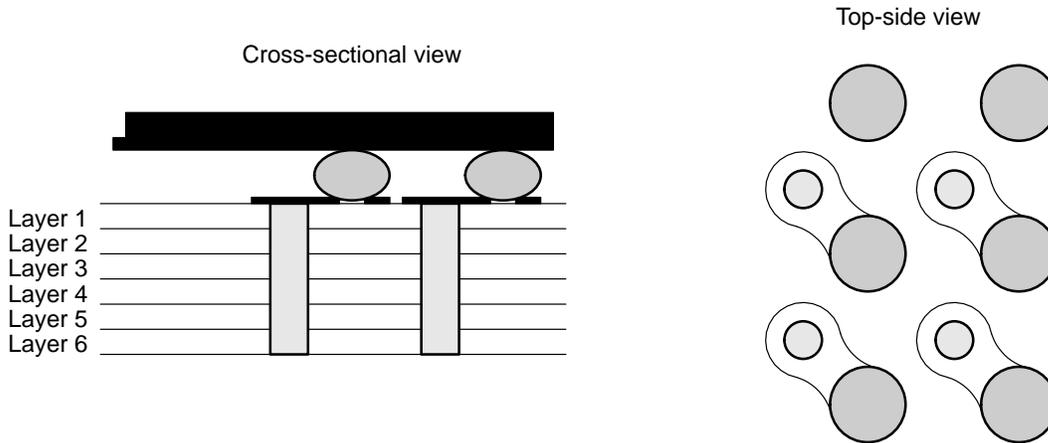


Figure 2. Dog Bone Connecting Thru-Hole Via

This time-consuming method requires a very small mechanical drill to create 144, 176, or 179 vias, based on the package. Although this method is the least expensive, a disadvantage is that the vias go through the board, creating a matrix of vias on the bottom side of the board. Ideally, the bottom layer is used to place the bypass capacitors close to the power pins.

Another disadvantage is that the clearance of these vias can reduce (and in some case eliminate) the copper between the pads. The area of copper between the pads is critical for the connection between power plane and power pins that are not located on the outside row of the grid array. Furthermore, the thru-hole via is bare copper, which can exacerbate problems with solder ball collapse.

2.1 Burying the Dog Bone

The other option, which is the purpose of this application report, is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 3 illustrates this method using 4 mil, laser-drilled microvias in the center of the pads and burying the dog bone on layer 2. This technique minimizes the probability of complications from solder-ball collapse.

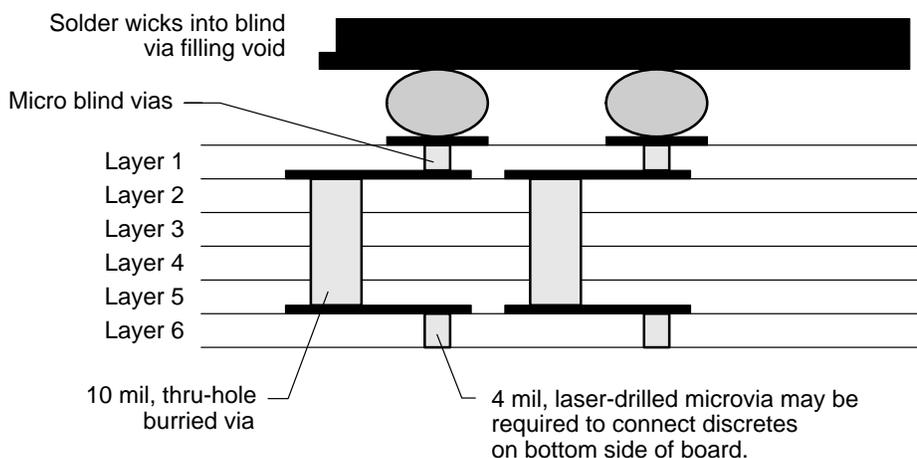


Figure 3. Burying the Dog Bond on Layer 2

Furthermore, since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias (if needed) to connect the bypass capacitors and other discrete components to the bottom side. The buried via is a 10 mil (reducible to 8 mil) mechanical drilled hole with a 9 mil annular ring. This corresponds to a $10 + 9 + 9 = 28$ mil area diameter.

It is recommended that designers use non-solder masked defined (NSMD) solder lands where the balls adhere to the PCB. The non-solder mask clearance should have an annular ring of 1 to 3 mils. The solder land diameter can range from 14 to 18 mils. A solder land of 16 mils was chosen for the referenced board in this application report.

2.2 Power Plane Considerations

Ideally, power pins should be connected to as much uniform copper on the plane as possible. However, because mechanically drilled vias, (i.e., buried and thru-hole) are much larger than microvias, copper width and spacing requirements can become marginal. Consequently, there is no guarantee that solder lands dedicated to the device's power pins will connect to the power plane. Power pins most affected by this problem are the internal balls (that is, pins not on the outer row) adjacent to pins with buried vias. Figure 4 shows the Clean ($V_{CC} = 2.5$ V) and Dirty ($V_{DD} = 3.3$ V) power pins of the TMS320VC549GGU and their location relative to signal and ground pins.

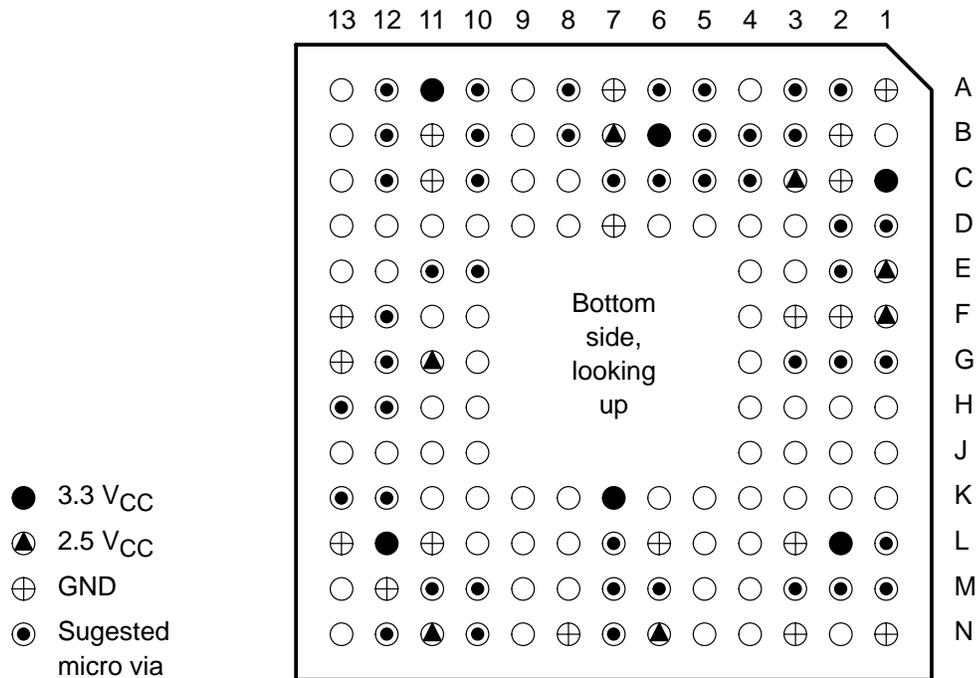


Figure 4. Clean Power, Dirty Power, and Ground Pinout

Carefully selecting the pins that are routed on layers one and two can dramatically increase the routability of power pins. Using laser-drilled microvias, route signals adjacent to power pins and the signals that lead to the periphery of the chip on layers one and two. These signals do not require buried vias, creating a wider copper channel between the balls on the power planes. For example, Figure 4 shows specific balls (balls with black dots) that should be considered for microvia routing on layers one or two.

Layer stack-up can also help power plane routability. Power planes that reside on the first (4 mil microvias) or first two (8 mil microvias) layers can be routed easier, since the buried vias start on the next layer. The same design rule applies to the bottom side of the board.

2.3 Placing Discrete Components

With the advent of buried capacitance and buried resistance, future discrete components, such as bypass capacitors and pullup resistors, will not require physical surface space. Until then, board layout and component density will be limited by certain physical form factors. The board x-ray in Figure 5, oriented from bottom side looking toward the top layer, shows a VC549GGU (144-pin BGA) package mounted on top. The bypass capacitors are mounted directly underneath the package on the underside of the board. Depending on the required capacitive loading, all of the bypass capacitors may fit within the physical form factor of the GGU package (12 mm x 12 mm). The dark rectangles are the bypass capacitors connected to the power pins of a GGU package.

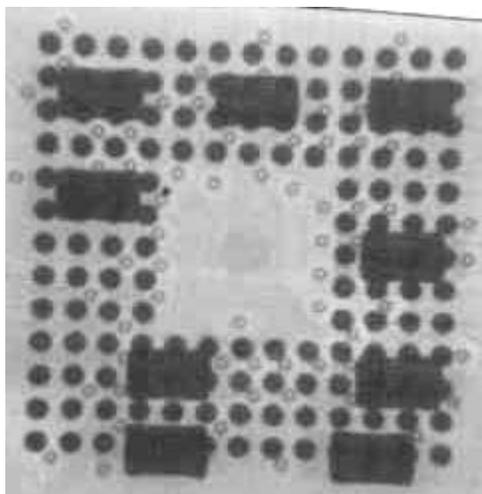


Figure 5. X-Ray of TMS320VC549GGU Alignment

An alternative is to populate the top side of the board with bypass capacitors around the periphery of the chip, leaving the underside for other discretives and integrated circuits (ICs). In either solution, some component density is lost.

2.4 Cost Analysis

Many applications, especially in the consumer electronics industry, are particularly sensitive to changes in manufacturing costs. Increasing layers of the PCB can cost anywhere from 10 to 20 percent per two layers. A premium of 10 to 15 percent per set of blind/buried vias can be expected. However, both options dramatically increase the PCB's routability.

These premiums mentioned above are from a 75 board manufacturing build of the referenced design in this report. The premiums are only estimates and vary depending on the manufacturer, manufacturing volumes, and sets of blind/buried vias.

3 Surface Mount Criteria

3.1 Solder Paste

Once the design is complete and boards are ready to be populated (reflowed), it is strongly recommended to use solder paste on the BGA solder lands. In manufacturing builds not using solder paste, up to a 10x-failure rate is possible.

There are several advantages to using solder paste. Some people believe using high silver (2%) solder paste can make a better reflow connection. Additionally, solder paste can alleviate some coplanarity problems between the solder ball and solder lands. Furthermore, if the volume of solder in the ball is questionable due to the wicking effect of the 4 (8) mil microvias, solder paste can counteract this by adding solder to the reflow.

3.2 IR Reflow Profile

A wide variety of reflowing furnaces can be used for the MicroStar BGA packages. The optimal solution is a full convection furnace, which helps to minimize temperature differences on the board. The reflow parameters for the plastic MicroStar BGA packages are:

- Method: Air reflow
- Temp and time: RT to 140°C for 60-90 seconds
 - 140°C to 180°C for 60-120 seconds
 - Time above 183°C is 60-150 seconds.
- Peak temp: 230°C ±5 °C
- Time within 5°C of peak temp is 10-20 seconds.
- Ramp-down rate is a maximum of 6°C/second.

3.3 Solder Ball Collapse

In some packages solder ball collapse can occur, creating interconnects between adjacent balls. The overall package standoff is a function of the following:

- Size of solder ball (fixed)
- Solder paste volume on board land (controllable)
- Board land diameter (see next paragraph)
- Package weight (fixed)

A typical standoff is 14 mils for the GGU package. The designer should not attempt to change this standoff by controlling the diameter of the PCB land. To ensure proper reliability and manufacturability, use a board land 14 to 18 mils in diameter. Reducing the land diameter increases the package standoff but decreases the cross-section area of the joint.

3.4 PCB Finish

The PCB finish is to minimize any coplanarity problems between the solder balls and the solder lands. The Immersion Gold finish is recommended due to its uniform application to the copper lands. However, Immersion Gold may be inferior to the Organic Solder Preservative (OSP) finish. This is outside the scope of this report and should be investigated at your discretion.

3.5 Package Alignment

A very reliable byproduct of reflowing MicroStar BGAs is the package's capability to automatically self-align over the board solder lands. Figure 5 shows package-land alignment that is close to ideal. This feature is caused by the surface tension of the solder balls pulling the device over the pads. In the past, packages were too heavy for the surface tension to overcome, and alignment was completely dependent on placement machinery. The MicroStar BGA packages are very lightweight. In fact, the MicroStar packages (GGU and GHH, to be more specific) have been seen to auto-align when placement machinery is off by 30-40 percent.

3.6 Reliability

The MicroStar BGAs and other CSPs have a characteristic that can cause reliability problems if not addressed from the design stage. The characteristic involves joint fatigue failures during temperature cycling. The coefficients of thermal expansion (CTEs) for the chip and PCB are very different. The large CTE disparity causes different expansion rates of compounds and creates joint fatigue between the PCB's FR4 and the package. The package CTE can be defined as being silicon, since the majority of the package is the silicon die. Epoxy resins, glass fibers, and copper influence the PCB's FR4. Table 1 shows the differences in the CTEs for silicon and FR4.

Table 1. Coefficients of Thermal Expansion

Material	Silicon	PCB FR4
CTE @ 25°C (PPM/°C)	3.0	16 – 18

As a general rule for optimal joint reliability, the PCB land diameter should be equal to the diameter of the MicroStar BGA package via. The package via, which is approximately 15 mils in diameter, connects the ball and the package substrate. Matching the two diameters increases the board level reliability by optimizing the package standoff and reducing the effects of thermal expansion.

In most cases, the PCB land diameter will never match the package via exactly. Furthermore, PCB manufacturers may require a 5 mil annular ring when laser-drilling the PCB lands. These restrictions would require a minimum land diameter of 14 mils, with 4 mil microvias ($5 + 4 + 5 = 14$) or an 18 mil land diameter with 8 mil microvias. The PCB land diameter should not exceed 18 mils.

To further minimize the probability of joint-fatigue failures, it is important to follow the surface mount process and reflow parameters mentioned in this report.

4 Summary

It is important to remember that the design technique mentioned in this report is only one option. Any combination of blind vias, buried vias, and via depths are all valid design options. In the future, MicroStar package pin-out may be more configurable due to the flex-circuit on the polyimide layer. The signals connected to the die could be routed on the flex-circuit to more convenient ball locations (i.e., the outer row).

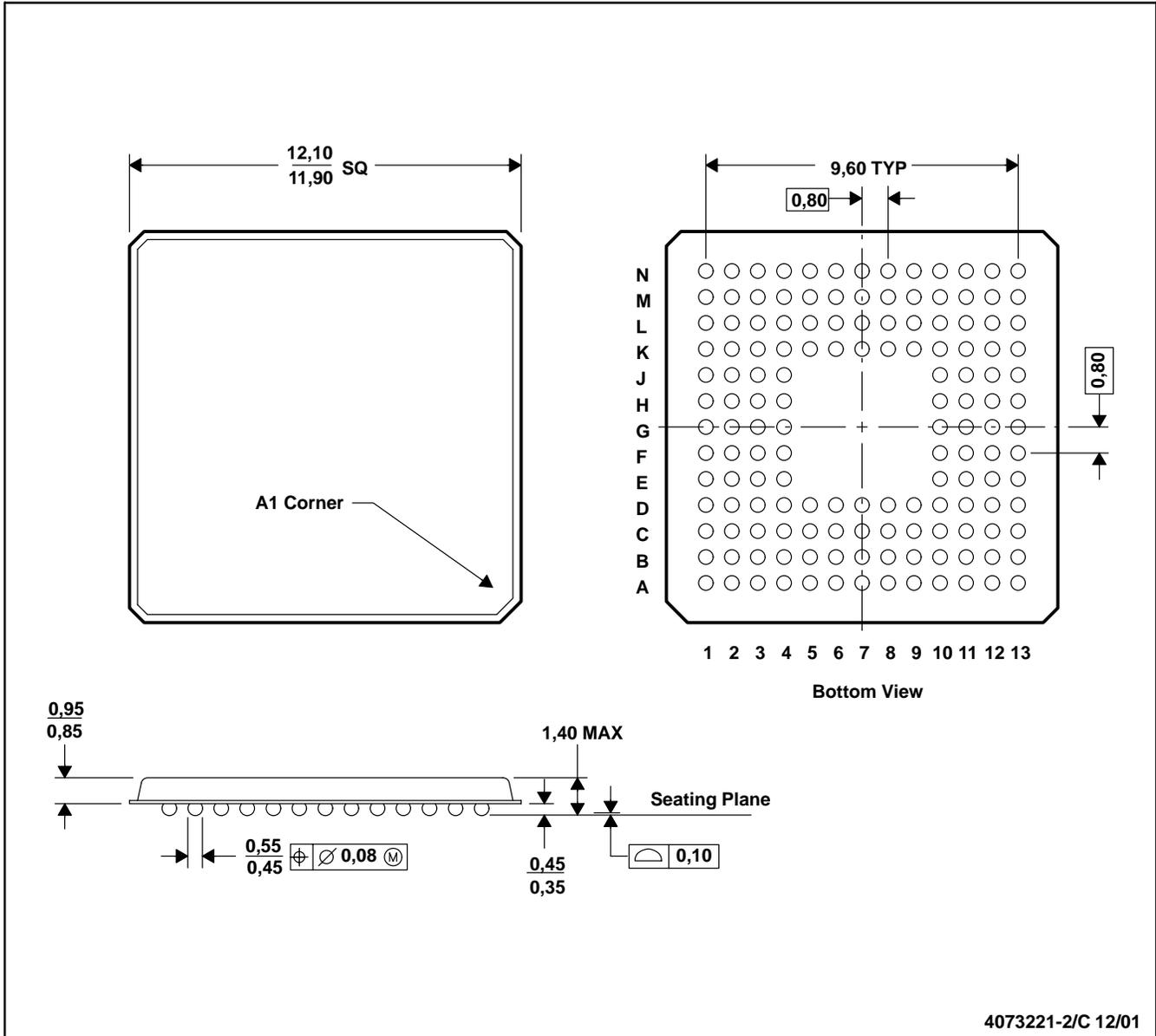
Chip Scale Packages, such as the GGW, GGU or GHH MicroStar BGAs, offer a whole new set of PCB design possibilities. On the other hand, they introduce a whole new set of design rules. By following simple design rules, PCB designers can create applications with levels of component density never seen before in the industry. Use of PCB surface space can be increased effectively, allowing functionality per square inch to shoot through the roof.

Furthermore, with continued innovations in laser drilling, blind/buried vias, buried components and semiconductor integration, new smaller packaging technology will be required. Texas Instruments is dedicated to lead the industry with exciting, new packaging technologies and believes in giving customers “more for your buck” by continued semiconductor integration and innovation.

5 References

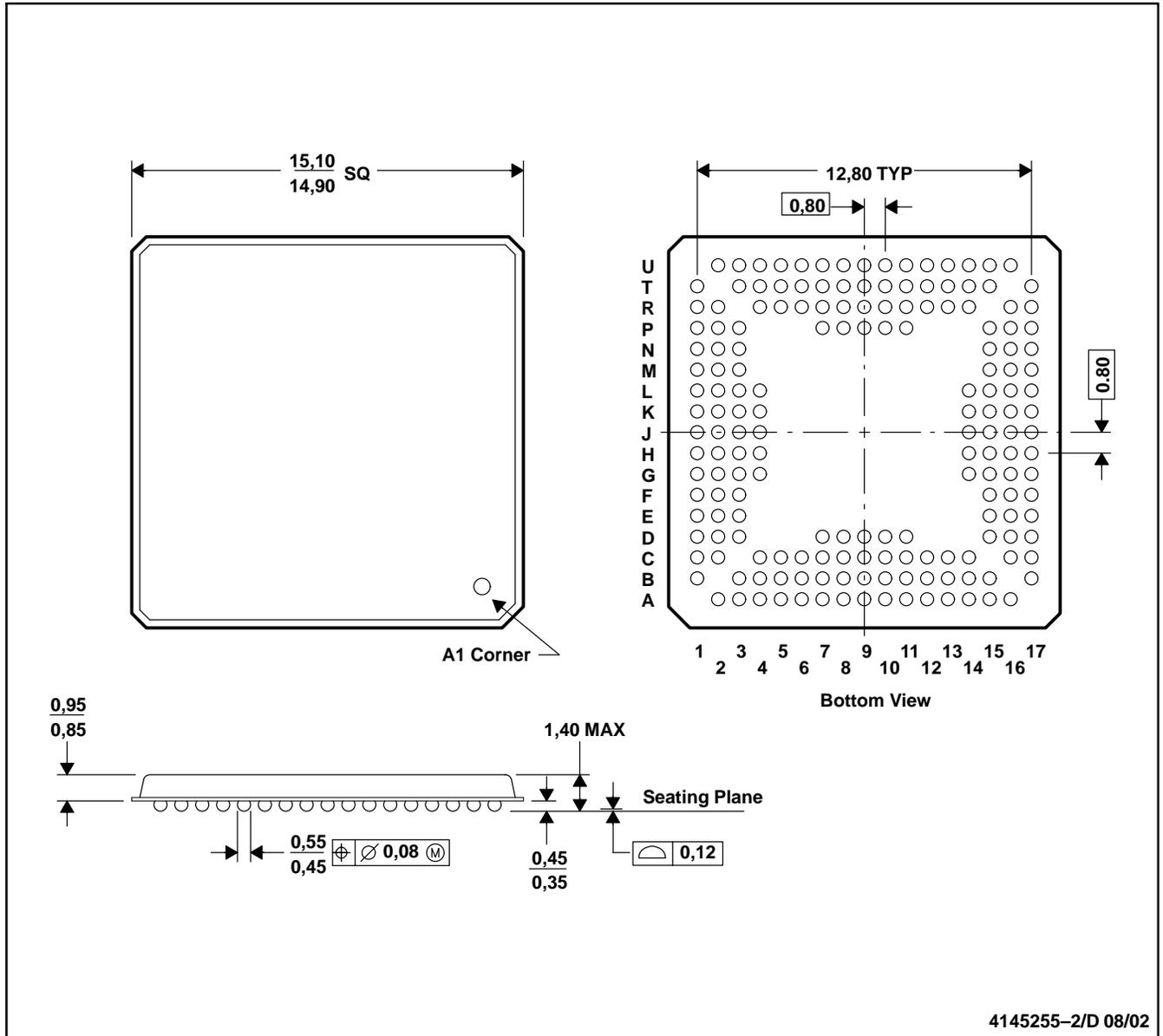
1. Lyne, Kevin. *Ball Grid Arrays from Texas Instruments*, Texas Instruments, December 1993.

Appendix A GGU, GGW, and GHH Package Drawings



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar BGA configuration

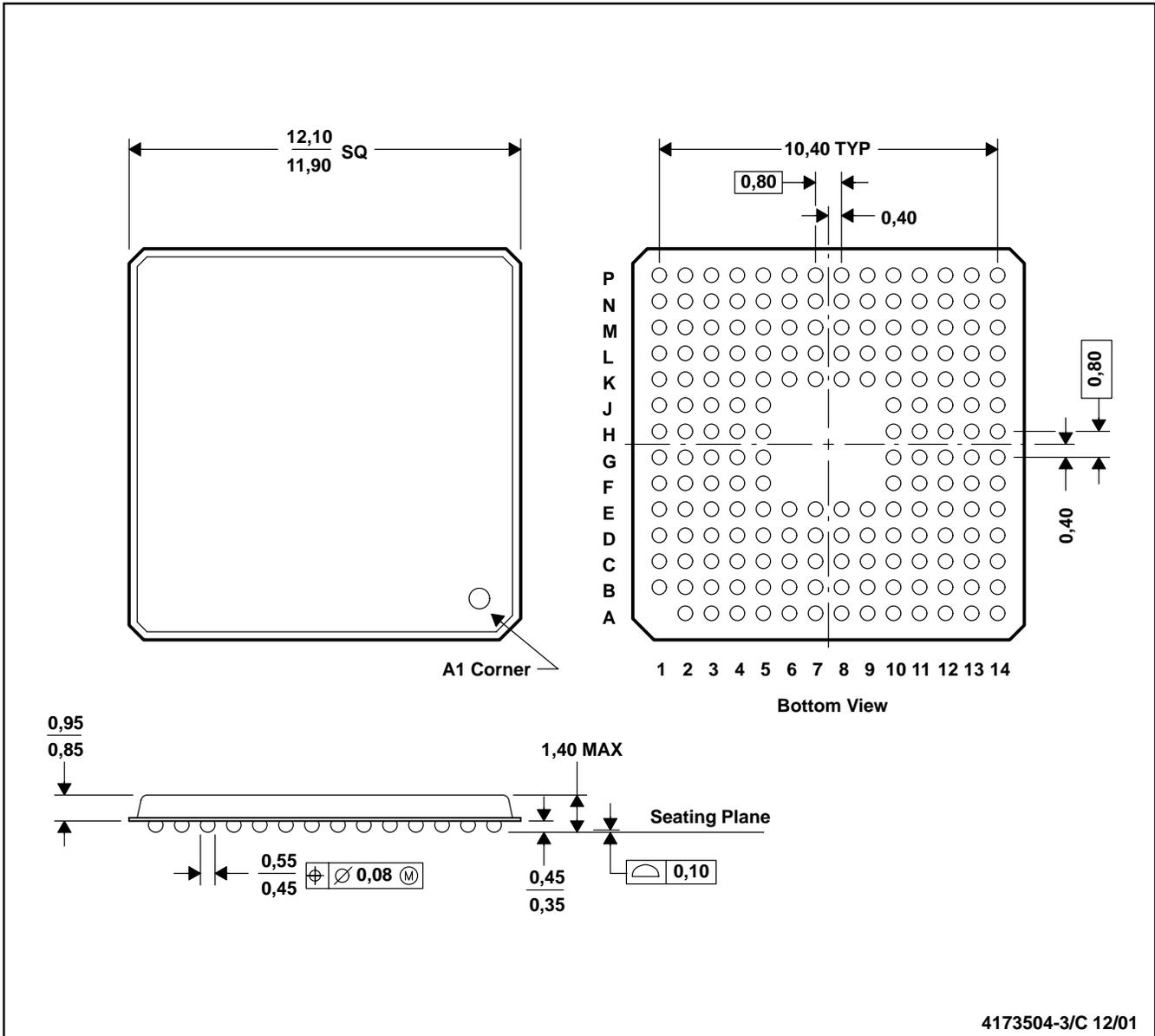
Figure A-1. GGU 144-Pin Package



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- NOTES: D. All linear dimensions are in millimeters.
 E. This drawing is subject to change without notice.
 F. MicroStar BGA™ configuration.

Figure A-2. GGW 176-Pin Package



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- NOTES: G. All linear dimensions are in millimeters.
 H. This drawing is subject to change without notice.
 I. MicroStar BGA configuration.

Figure A-3. GHH 179-Pin Packaging

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