# TMS320C62x/C67x Power Consumption Summary

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**ABSTRACT**

This document discusses the power consumption of the Texas Instruments TMS320C6201B, TMS320C6701, TMS320C6202, TMS320C6202B, TMS320C6203, TMS320C6204, TMS320C6205, TMS320C6211, and TMS320C6711 digital signal processors (DSPs) for typical applications. The C6201B, C6701, C6202, C6211, and C6711 DSPs are manufactured on TI's advanced 0.18-micron process and operate with a core voltage of 1.8 V. The C6202B, C6203, C6204, and C6205 are manufactured on TI's 0.15-micron process, and operate with a core voltage of 1.5 V. All TMS320C62x™ and TMS302C67x™ devices operate with 3.3-V input/output (I/O) supply, to be compatible with the widest selection of external devices. The low core voltage and other power design optimizations allow these DSPs to operate with industry leading performance and a low power-performance ratio.

The data presented in this document is actual measured power consumption for the C6201, C6202,C6701, and C6211. The C6202B, C6203, C6204, and C6205 power consumption is based on design simulations and extrapolations from the C6202. The C6711 typical activity data is based on extrapolations from C6211 and C6701 measurements.

| | | | Typical Activity | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Power at Frequency (W) | | | Power per Frequency (mW/MHz) | | |
| Device | Core Voltage Level | Frequency | CPU | Internal | Internal + External | CPU | Internal | Internal + External |
| C6201B | 1.8 V | 200 MHz | 0.4 | 1.3 | 1.7 | 2.2 | 6.7 | 8.5 |
| C6202 | 1.8 V | 250 MHz | 0.6 | 2.1 | 2.3 | 2.2 | 8.3 | 9.3 |
| C6202B | 1.5 V | 250 MHz | 0.2 | 1.1 | 1.4 | 0.9 | 4.4 | 5.5 |
| C6203 | 1.5 V | 300 MHz | 0.3 | 1.3 | 1.5 | 0.9 | 4.4 | 5.1 |
| C6204 | 1.5 V | 200 MHz | 0.2 | 0.8 | 1.2 | 0.9 | 4.0 | 5.8 |
| C6205 | 1.5 V | 200 MHz | 0.2 | 0.8 | 1.2 | 0.9 | 4.0 | 5.8 |
| C6211 | 1.8 V | 150 MHz | 0.3 | 0.9 | 1.1 | 2.2 | 6.0 | 7.2 |
| C6701 | 1.8 V | 167 MHz | 0.6 | 1.4 | 1.8 | 3.8 | 8.6 | 10.5 |
| C6711 | 1.8 V | 150 MHz | 0.6 | 1.1 | 1.3 | 3.8 | 7.5 | 8.8 |

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# 1 Activity Level Models

TMS320C62x and TMS320C67x power consumption can be modeled as a combination of two levels of activity—high DSP activity and low DSP activity. An accurate prediction of an application's power consumption can be developed based on weighted averages of the two activity levels.

## 1.1 High Activity Model

Table 1 shows the characteristics associated with high DSP activity for all C62x™/C67x™ DSPs. High DSP activity represents a finite impulse response (FIR) filter, fast Fourier transform (FFT), or other fully optimized algorithm.

Depending on the specific DSP, a different high activity model is used to compare the power consumption of the C662x/C67x DSPs on an equivalent basis. For example, the C6202 has three times more internal memory than the C6201B; the C6203 has seven times more internal memory than the C6201B. For typical applications, the C6202 and C6203 can maintain most of the necessary code and data in internal memory, reducing the amount of sustained I/O activity necessary to implement an algorithm. This is reflected in the high activity definitions shown in Table 1 and Table 2.

**NOTE:** For power consumption at increased I/O activity levels, refer to Table 9.

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**Table 1. Summary of High Activity Levels**

| High DSP Activity | CPU Activity Level | Program Memory Access Rate | Data Memory Access Rate | Memory I/O 30-pF Load |
|---|---|---|---|---|
| C6201B/C6701/ C6204/C6205 | 8 instructions | 100% | 100% CPU 50% DMA | 100% access at 1/2 CPU Speed |
| C6211/C6711 | 8 instructions | 100% | 100% CPU 50% DMA | 100% access at 100 MHz |
| C6202/C6202B | 8 instructions | 100% | 100% CPU 17% DMA | 33% access at 1/2 CPU Speed |
| C6203 | 8 instructions | 100% | 100% CPU 7% DMA | 14% access at 1/2 CPU Speed |

**Table 2. High Activity Details**

| Module | C6201B/C6211/ C6204/C6205 High DSP Activity | C6202/C6202B High DSP Activity | C6203 High DSP Activity | C6701/C6711 High DSP Activity |
|---|---|---|---|---|
| DMA/ EMIF | 50% writes/50% reads to/from SDRAM | 17% writes/17% reads to/from SDRAM/ 66% idle | 7% writes/7% reads to/from SDRAM/ 86% idle | 50% writes/50% reads to/from SDRAM |
| I/O | 32 bits/CLKOUT2 (ECLKOUT)† cycle | 32 bits/3 CLKOUT2 cycles | 32 bits/7 CLKOUT2 cycles | 32 bits/CLKOUT2 (ECLKOUT)† cycle |
| Data Memory via DMA | 50% DMA = 32 bits/ 2 cycles via DMA | 17% DMA = 32 bits/ 6 cycles via DMA | 7% DMA = 32 bits/ 14 cycles via DMA | 50% DMA = 32 bits/ 2 cycles via DMA |
| CPU | 8 instructions/cycle with 2 LDW instructions | | | 8 instructions/cycle with 2 LDDW instructions and 4 floating point operations |
| Data Memory via CPU | 100% CPU = 64 bits/cycle via LDW instructions | | | 100% CPU = 128 bits/cycle via LDDW instructions |
| Program Memory | 100% = 1 fetch packet/cycle = 256 bits/cycle | | | |
| McBSP | 2 channels @ E1 rate | | | |
| Timers | 2 timers @ max rate (1/8 CPU clock) | | | |

† C6211/C6711 measurements are made with 150 MHz CPU and 100 MHz ECLKIN frequency.

## 1.2 Low Activity Model

The low activity model used for the C62x/C67x generations of DSPs is identical for each device. This activity level is summarized in Table 3. Low DSP activity represents the time spent setting up registers or executing other less optimized code segments.

The actual code used to model the activity levels is described in detail in Table 4.

**Table 3. Summary of Low Activity Levels**

| Low DSP Activity | CPU Activity Level | Program Memory Access Rate | Data Memory Access Rate | Memory I/O 30-pF Load |
|---|---|---|---|---|
| All C6000 DSPs | 2 instructions | 25% | 25% (12.5%) CPU† | 0% access |

† The low-DSP-activity test cases are identical for the C67x and C62x. This test case does one LDH per cycle, which represents 25% of the C62x internal data memory bandwidth and 12.5% of the C67x internal data memory bandwidth.

**Table 4. Low Activity Levels**

| Module | C6000 Low DSP Activity |
|---|---|
| CPU | 2 instructions/cycle with 1 LDH instruction |
| Data memory | 25% (12.5%)† = 16 bits/cycle via CPU LDH instruction |
| Program memory | 25% = 1 fetch packet/4 cycles = 256 bits/4 cycles |
| DMA/EMIF | DMA services McBSPs |
| EMIF I/O | None |
| McBSP | 2 channels @ E1 rate |
| Timers | 2 timers @ Max rate (1/8 CPU clock) |

† The low-DSP-activity test cases are identical for the C67x and C62x. This test case does one LDH per cycle, which represents 25% of the C62x internal data memory bandwidth and 12.5% of the C67x internal data memory bandwidth.

# 2 Power Measurement Results for C62x/C67x DSPs

Real-world applications typically spend between 50 and 75 percent of their time performing high-DSP-activity operations, and the remainder of their time performing low-DSP-activity operations. The 75% high/25% low and 50% high/50% low categories represent these applications. Depending on the particular application, an estimate of the ratio of high/low activity must be made to predict power consumption.

The following tables show the measured power consumption for the C6201B, C6701, C6202, and C6211 devices, and the estimated power consumption for the C6202B, C6203, C6204, C6205, and C6711. Table 5 details the power consumption of the C6000 devices at 50% high/50% low activity. Table 6 details the power consumption of the C6000 devices at 75% high/25% low activity levels.

I/Os consume a significant amount of total power. If most code and data can be stored in internal memory, thus reducing the required I/O, power consumption can be further reduced. In addition, all test measurements are based on a high load (30pF). With less load, the I/O power consumption is reduced accordingly.

## Table 5. Power Consumption at 50% High/50% Low Activity Details

| 50% High Power 50% Low Power | | CPU and Memory | | | Peripherals | | | | Core Total | I/O | | I/O Total | TOTAL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CPU | Internal Memory | Total | External Memory I/O | Peripheral Activity | Baseline Clocking | Total | | Baseline | I/O Activity | | |
| C6201B 200 MHz | Power (W) | 0.45 | 0.37 | 0.82 | 0.07 | 0.01 | 0.44 | 0.52 | 1.34 | 0.10 | 0.26 | 0.36 | 1.70 |
| | % Total | 26% | 22% | 48% | 4% | 1% | 26% | 31% | 79% | 6% | 15% | 21% | |
| C6202 250 MHz | Power (W) | 0.56 | 0.62 | 1.18 | 0.04 | 0.01 | 0.84 | 0.89 | 2.07 | 0.10 | 0.16 | 0.26 | 2.33 |
| | % Total | 24% | 27% | 50% | 2% | 0% | 36% | 38% | 89% | 4% | 7% | 11% | |
| C6202B 250 MHz | Power (W) | 0.21 | 0.43 | 0.65 | 0.02 | 0.00 | 0.42 | 0.45 | 1.09 | 0.13 | 0.16 | 0.29 | 1.38 |
| | % Total | 15% | 31% | 47% | 2% | 0% | 30% | 32% | 79% | 9% | 12% | 21% | |
| C6203 300 MHz | Power (W) | 0.26 | 0.52 | 0.77 | 0.03 | 0.01 | 0.50 | 0.53 | 1.31 | 0.10 | 0.12 | 0.22 | 1.53 |
| | % Total | 17% | 34% | 51% | 2% | 0% | 33% | 35% | 86% | 7% | 8% | 14% | |
| C6204 200 MHz | Power (W) | 0.17 | 0.27 | 0.44 | 0.02 | 0.00 | 0.34 | 0.36 | 0.79 | 0.10 | 0.26 | 0.36 | 1.15 |
| | % Total | 15% | 23% | 38% | 1% | 0% | 29% | 31% | 69% | 9% | 23% | 31% | |
| C6205 200 MHz | Power (W) | 0.17 | 0.27 | 0.44 | 0.02 | 0.00 | 0.34 | 0.36 | 0.79 | 0.10 | 0.26 | 0.36 | 1.15 |
| | % Total | 15% | 23%. | 38% | 1% | 0% | 29% | 31% | 69% | 9% | 23% | 31% | |
| C6211 150 MHz | Power (W) | 0.34 | 015 | 0.49 | 0.05 | 0.01 | 0.35 | 0.40 | 0.89 | 0.06 | 0.13 | 0.19 | 1.08 |
| | % Total | 31% | 14% | 45% | 4% | 1% | 32% | 37% | 82% | 6% | 12% | 18% | |
| C6701 167 MHz | Power (W) | 0.64 | 0.31 | 0.95 | 0.07 | 0.01 | 0.42 | 0.50 | 1.44 | 0.10 | 0.21 | 0.31 | 1.75 |
| | % Total | 36% | 18% | 54% | 4% | 1% | 24% | 28% | 82% | 6% | 12% | 18% | |
| C6711 150 MHz | Power (W) | 0.57 | 0.15 | 0.73 | 0.05 | 0.01 | 0.35 | 0.40 | 1.13 | 0.06 | 0.13 | 0.19 | 1.32 |
| | % Total | 43% | 12% | 55% | 4% | 1% | 26% | 31% | 86% | 5% | 10% | 14% | |

**Table 6. Power Consumption at 75% High/25% Low Activity**

| 50% High Power 50% Low Power | | CPU and Memory | | | Peripherals | | | | Core Total | I/O | | I/O Total | TOTAL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CPU | Internal Memory | Total | External Memory I/O | Peripheral Activity | Baseline Clocking | Total | | Baseline | I/O Activity | | |
| C6201B 200 MHz | Power (W) | 0.51 | 0.44 | 0.95 | 0.11 | 0.01 | 0.44 | 0.56 | 1.50 | 0.10 | 0.34 | 0.44 | 1.94 |
| | % Total | 26% | 23% | 49% | 5% | 1% | 23% | 29% | 78% | 5% | 17% | 22% | |
| C6202 250 MHz | Power (W) | 0.63 | 0.76 | 1.39 | 0.06 | 0.01 | 0.84 | 0.91 | 2.31 | 0.10 | 0.19 | 0.29 | 2.60 |
| | % Total | 24% | 29% | 54% | 2% | 0% | 32% | 35% | 89% | 4% | 7% | 11% | |
| C6202B 250 MHz | Power (W) | 0.24 | 0.53 | 0.78 | 0.03 | 0.00 | 0.42 | 0.46 | 1.23 | 0.13 | 0.19 | 0.32 | 1.55 |
| | % Total | 16% | 34% | 50% | 2% | 0% | 27% | 29% | 79% | 8% | 12% | 21% | |
| C6203 300 MHz | Power (W) | 0.29 | 0.64 | 0.93 | 0.04 | 0.00 | 0.50 | 0.55 | 1.48 | 0.10 | 0.12 | 0.22 | 1.69 |
| | % Total | 17% | 38% | 55% | 2% | 0% | 30% | 32% | 87% | 6% | 7% | 13% | |
| C6204 200 MHz | Power (W) | 0.20 | 0.33 | 0.52 | 0.03 | 0.00 | 0.34 | 0.36 | 0.89 | 0.10 | 0.34 | 0.44 | 1.32 |
| | % Total | 15% | 25% | 40% | 2% | 0% | 25% | 28% | 67% | 8% | 25% | 33% | |
| C6205 200 MHz | Power (W) | 0.20 | 0.33 | 0.52 | 0.03 | 0.00 | 0.34 | 0.36 | 0.89 | 0.10 | 0.34 | 0.44 | 1.32 |
| | % Total | 15% | 25% | 40% | 2% | 0% | 25% | 28% | 67% | 8% | 25% | 33% | |
| C6211 150 MHz | Power (W) | 0.38 | 0.18 | 0.56 | 0.07 | 0.01 | 0.35 | 0.43 | 0.99 | 0.06 | 0.06 | 0.25 | 1.24 |
| | % Total | 31% | 15% | 46% | 6% | 1% | 28% | 35% | 80% | 5% | 5% | 20% | |
| C6701 167 MHz | Power (W) | 0.77 | 0.37 | 1.14 | 0.10 | 0.01 | 0.42 | 0.53 | 1.67 | 0.10 | 0.10 | 0.37 | 2.04 |
| | % Total | 38% | 18% | 56% | 5% | 0% | 21% | 26% | 82% | 5% | 5% | 18% | |
| C6711 150 MHz | Power (W) | 0.69 | 0.18 | 0.87 | 0.07 | 0.01 | 0.35 | 0.43 | 1.30 | 0.06 | 0.06 | 0.25 | 1.55 |
| | % Total | 45% | 12% | 57% | 5% | 1% | 22% | 28% | 84% | 4% | 4% | 16% | |

## 2.1 Low Power Modes

Table 7 reports the power consumption for several special operating conditions with the peripherals unused. IDLE is an instruction that effectively executes continuous NOPs. The advantage with the IDLE instruction is that program fetches do not occur until an interrupt occurs. The other power-down modes (PD1, PD2, and PD3) enable and disable the clock at different portions of the DSP. These low power modes are the optimal way of saving power during pauses in an application. (For more information on low power modes, see the *TMS320C6000 Peripherals Reference Guide*, literature number SPRU190.)

**Table 7. Low Power Modes for C6000 Devices**

| | | Idle | | PD1 | | PD2† | PD3† |
|---|---|---|---|---|---|---|---|
| | | W | mW/MHz | W | mW/MHz | mW | mW |
| C6201B | 200 MHz | 0.82 | 4.10 | 0.62 | 3.10 | < 10 | < 10 |
| C6202 | 250 MHz | 1.17 | 4.67 | 0.90 | 3.60 | < 10 | < 10 |
| C6202B | 250 MHz | 0.56 | 2.25 | 0.45 | 1.80 | < 10 | < 10 |
| C6203 | 300 MHz | 0.69 | 2.30 | 0.54 | 1.80 | < 10 | < 10 |
| C6204 | 200 MHz | 0.43 | 2.15 | 0.36 | 1.80 | < 10 | < 10 |
| C6205 | 200 MHz | 0.43 | 2.15 | 0.36 | 1.80 | < 10 | < 10 |
| C6211 | 150 MHz | 0.51 | 3.42 | 0.35 | 2.36 | < 10 | < 10 |
| C6701 | 167 MHz | 0.82 | 4.90 | 0.58 | 3.50 | < 10 | < 10 |
| C6711 | 150 MHz | 0.57 | 3.83 | 0.35 | 2.36 | < 10 | < 10 |

† Frequency independent

Table 8 reports the power savings realized for the low-power peripheral modes of the C6202, C6203, C6204, and C6205. These modes allow the clock for specific peripherals of the device to be turned off when a peripheral is not in use. (For more detailed information on the peripheral power down modes, refer to the *TMS320C6000 Peripherals Reference Guide*, literature number SPRU190.)

**Table 8. Peripheral Power Down – Power Savings for C6202, C6202B, C6203, C6204, and C6205**

| | C6202 250 MHz | C6202B 250 MHz | C6203 300 MHz | C6204 200 MHz | C6205 200 MHz | Units |
|---|---|---|---|---|---|---|
| DMA | 0.163<br>0.65 | 0.080<br>0.32 | 0.096<br>0.32 | 0.064<br>0.32 | 0.064<br>0.32 | W<br>mW/MHz |
| EMIF | 0.095<br>0.38 | 0.048<br>0.19 | 0.057<br>0.19 | 0.038<br>0.19 | 0.038<br>0.19 | W<br>mW/MHz |
| McBSP1 | 0.030<br>0.12 | 0.015<br>0.06 | 0.018<br>0.06 | 0.012<br>0.06 | 0.012<br>0.06 | W<br>mW/MHz |
| McBSP2 | 0.030<br>0.12 | 0.015<br>0.06 | 0.018<br>0.06 | 0.012<br>0.06 | 0.012<br>0.06 | W<br>mW/MHz |
| McBSP3 | 0.030<br>0.12 | 0.015<br>0.06 | 0.018<br>0.06 | 0.012<br>0.06 | 0.012<br>0.06 | W<br>mW/MHz |

# 3 DMA Driven I/O Activity

Table 9 details the power consumption resulting if DMA (direct memory access) activity to and from external memory for the C6202, C6202B, and C6203 is increased relative to the high and/or low activity test cases. The high power model for the C6202, C6202B, and C6203 assumes that because a greater amount of internal memory is present, less I/O activity will be required. This holds true for most applications.

**NOTE:** C6201/C6701 test cases incorporate the full range of I/O activity. This data can be extrapolated from Table 5 and Table 6. Therefore, no equivalent to Table 9 is necessary for the C6201B and C6701 to estimate I/O power at any activity level.

For applications that still require a high amount of I/O activity, Table 9 can be used to account for this activity. The value chosen from the table should represent the entire operation time. For example, if 100% I/O activity is performed one half of the time, the 50% column should be used. Activity levels between 0 and 50%, or between 50 and 100%, can be approximated using linear interpolation. The resulting power consumption should directly replace the equivalent row in the C6202 and C6203 power summary table to give a total power consumption.

**Table 9. Power Substitution for Additional I/O Activity on C6202, C6202B, and C6203**

| | C6202 250 MHz | | | C6202B 250 MHz | | | C6203 300 MHz | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 100% Activity | 50% Activity | 0% Activity | 100% Activity | 50% Activity | 0% Activity | 100% Activity | 50% Activity | 0% Activity | Units |
| External Memory I/O | 0.24 | 0.12 | 0.00 | 0.16 | 0.08 | 0.00 | 0.19 | 0.09 | 0.00 | W |
| (1.5 or 1.8 V Supply) | 0.94 | 0.47 | 0.00 | 0.62 | 0.31 | 0.00 | 0.62 | 0.31 | 0.00 | MW/MHz |
| I/O Activity | 0.43 | 0.27 | 0.10 | 0.43 | 0.27 | 0.10 | 0.52 | 0.32 | 0.12 | W |
| (3.3 V Supply) | 1.73 | 1.07 | 0.40 | 1.73 | 1.07 | 0.40 | 1.73 | 1.07 | 0.40 | MW/MHz |

# 4 Power Estimate Examples

The numbers reported in Table 5 through Table 9 can be used to estimate the power consumption for C62x/C67x devices in a given application. To compute the power for a given application, the following steps should be taken:

1. The amount of time spent executing high activity code versus low activity code (or low power modes) must be estimated.
2. Based on the high activity/low activity estimate, a weighted average of the power consumption at these levels is calculated to predict the power consumption of an application.

   Step A) Calculate Core Power:

   Core Power = (%High Activity/% Low Activity) for Core

   Step B) Calculate I/O Power

   I/O Power = (% High Activity/% Low Activity) for I/O

   Step C) Calculate Total Power

   Total Power = Core Power + I/O Power

3. To further refine a power prediction, the individual components can be analyzed according to their own specific activity level to obtain a more accurate result. For the C6202, C6202B, and C6203, the actual level of I/O activity, and power saving resulting from peripherals not in use and are turned off via the peripheral power-down register, must be considered. In addition, if the desired frequency of operation is different than used in the tables, linear interpolation can be used to scale the resulting power consumption to the desired operating frequency.

**Example 1. C6202 Power Estimate**

The following example for the C6202 at 250 MHz assumes that data and code are stored in internal memory. Therefore, the I/O activity is reduced to the 0% high/100% low level. The core activity is maintained at a typical level of 75% high/25% low.

Total Power = Core Power (75% High/25% Low) + I/O Power (0% High/100% Low)

where CPU Frequency = 250 MHz

1. Core High Activity = 75%; Core Low Activity = 25%
   I/O High Activity = 0%; I/O Low Activity = 100%
2. Because the activity levels for this example match the activity profile already provided for the C6202 in Table 6, there is no need to perform linear interpolation to estimate the ’6202 power consumption. However, because a reduced amount of I/O activity is done via the DMA, data from Table 9 must be used to replace the external memory I/O and I/O activity values shown in Table 6.

   Step A) Core power calculation

   $\text{Core Power}_{250\ \text{MHz}}$ = Core Total 75/25 from Table 6 – External Memory I/O from Table 6 + External Memory I/O from Table 9
   = 2.31 W – 0.06 W + 0 W
   = 2.25 W

   Step B) I/O Power calculation

   $\text{I/O Power}_{250\ \text{MHz}}$ = I/O Total 75/25 from Table 6 – I/O Activity from Table 6 + I/O Activity from Table 9
   = 0.29W – 0.19 W + 0.10 W
   = 0.20 W

   Step C) Total power calculation

   Total Power = Core Power + I/O Power
   = 2.25 W + 0.20 W
   = 2.45 W
3. Since the desired operating frequency is 250 MHz, frequency scaling is not performed.

**Example 2. C6201B Power Estimate**

The following example for the C6201B assumes that data and code are stored in internal memory. Therefore, the I/O activity is reduced to the 0% high/100% low level. The core activity is maintained at a typical level of 67% high/33% low.

Total Power = Core Power (67% High/33% Low) + I/O Power (0% High/100% Low)

where CPU Frequency = 188 MHz

1. Core High Activity = 67%; Core Low Activity = 33%
   I/O High Activity = 0%; I/O Low Activity = 100%
2. To predict the power consumption based on these characteristics, linear interpolation can be used to determine the core power consumption at 67% high/33% low activity and the I/O power consumption at 0% high/100% low activity at 200 MHz.

   Step A) Core power calculation

   $\text{Core Power}_{200\ MHz}(67\%\ High) = (P_{75\%\ High} - P_{50\%\ High})/(75\%–50\%)\ x\ (67\% - 75\%) + P_{75\%\ High}$
   $= (1.5\ W - 1.34\ W)/(75\% - 50\%) * (67\% - 75\%) + 1.5\ W$
   $= 1.45\ W$

   Step B) I/O power calculation

   $\text{I/O Power}_{200\ MHz}(0\%\ High) = (P_{75\%\ High} - P_{50\%\ High})/(75\%–50\%)\ x\ (67\% - 75\%) + P_{75\%\ High}$
   $= (0.44\ W - 0.36\ W)/(75\% - 50\%) * (0\% - 75\%) + 0.44\ W$
   $= 0.2\ W$

   Step C) Total power calculation

   $\text{Total Power}_{200\ MHz} = 1.45 + 0.2\ W$
   $= 1.65\ W$
3. The previous calculation used data based on 200-MHz measurements. Next, the result must be derated to predict power consumption at 188 MHz.

   $\text{Power (Application Frequency)} = \text{Power}_{200\ MHz} * \text{Application Frequency} / 200\ MHz$
   $= 1.65\ W * 188\ MHz/200\ MHz$
   $= 1.55\ W$

# 5 Reference

1. *TMS3320C6000 Peripherals Reference Guide* (SPRU190).

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