

Interfacing the TMS320C57S Host Port Interface to 80386EX Host Processor

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Abstract

This document discusses how to connect an Intel 80386EX processor to the Texas Instruments (TI™) TMS320C57S Host Port Interface.

The TI TMS320C57S Host Port Interface (HPI) is an 8-bit parallel port used to interface a host processor to a 16-bit word structure 'C5x DSP. Using this port, the host must always read/write 2 consecutive bytes. The 386EX processor has an input signal BS8_ to indicate that external device is an 8-bit device. A low signal on this line allows 16-bit accesses from an 8-bit processor to be executed as 2 consecutive bytes through data bits D7:D0.

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Design Problem

How to connect an Intel 80386EX processor to the TMS320C57S Host Port Interface?

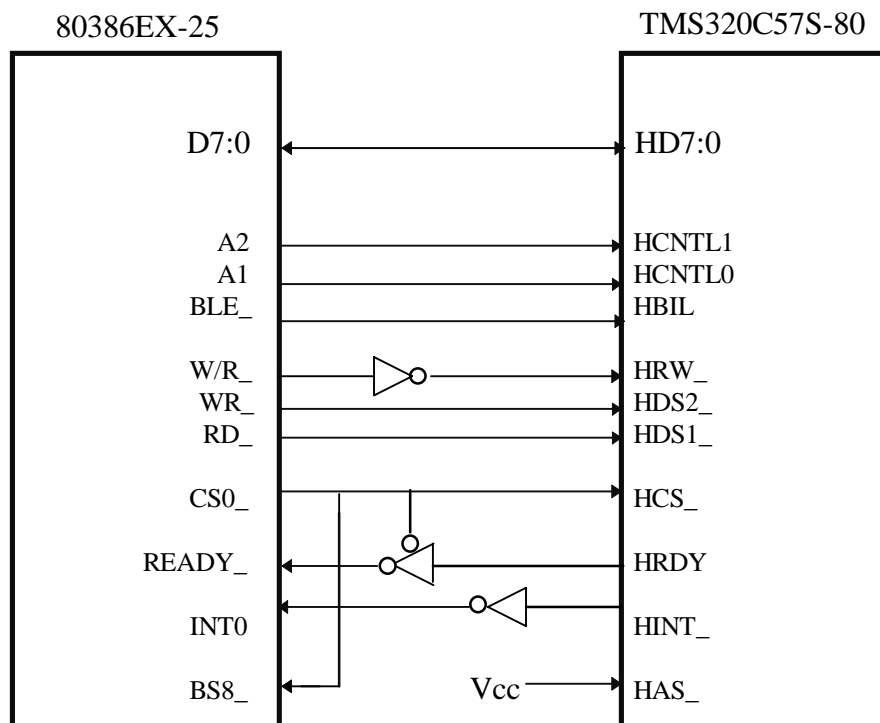
Solution

The Host Port Interface (HPI) is an 8-bit parallel port used to interface a host processor to a 16-bit word structure 'C5x DSP. Using this port, the host must always read/write two consecutive bytes. The 386EX processor has an input signal BS8_ to indicate that external device is an 8-bit device. A low signal on this line allows 16-bit accesses from an 8-bit processor to be executed as 2 consecutive bytes through data bits D7:D0.

From the 386EX address space we need only two lines (A2, A1) to specify where to access in the HPI: Control Register, Address Register, or Data Register (with automatic address modify or not). The 386EX has an internal decoder to place external devices in the address space. Here CS0_ is used for decoded addresses. You can map HPI also to the I/O space of the 386EX. A block diagram of hardware interface is shown in Figure 1.

The external clock for the 386EX is 50MHz (CLK2). This is divided by 2 internally to get 25MHz (40ns) to the CPU. The CPU can make external read/write cycles in 80ns. The speed of the 'C57S HPI in Host Only Mode (HOM) is 2 DSP CPU cycles and 5 DSP CPU cycles in Shared Access Mode (SAM). This means access times are 50ns and 125ns with an 80MHz external clock (40MHz/25ns). For SAM operation, we must use the READY_ line to insert a Wait State to 386EX (one WS means 40ns).

Figure 1. Block Diagram of Hardware Interface





Software Considerations

When the host is accessing the HPI for the first time, it must perform following sequence:

- 1) Write to the HPIC register bit 'BOB' = 1 (upper and lower bytes must be the same)
- 2) Write address to HPIA –registers

After this the host can read and write data registers.

When the DSP is in RESET mode, HPI is automatically in HOM mode. This makes it flexible enough to take control of DSP reset line (RS_) to the host. Also, if you want to save power, the host should take control of DSP clock. (These options are not included in Figure 1). In SAM mode the host must synchronize to the DSP clock. This means a maximum delay of one DSP clock cycle. The Host has priority for memory if DSP is accessing the HPI block in the same cycle.

If you want to boot from HPI, connect the HINT_ pin to INT3_ pin of DSP. The boot-loader program will verify this is done and transfer then program control to start address (8800h in program space).

The Host to DSP interrupt vector address is 0018h. The bit location in the IMR/IFR register is 11. The HPI control register (HPIC) is in address 500h in data memory.

DSP has 2KW HPI memory block in following addresses:

in program space	8800h - 8FFFh	(disabled if RAM=0)
in data space	1000h - 17FFh	(disabled if OVLY=0).

The DSP must take care of the following:

- RAM and OVLY bits must be set to 1 after reset.
- When SMODE bit is written from SAM to HOM, the next instruction must be NOP.
- When SMODE bit is written from HOM to SAM, the next instruction is not allowed to read HPI RAM block

The host processor can get the DSP to execute pre-programmed tasks by remapping the DSP interrupt vector table in program space to HPI memory block (8800h). The host needs to write the task address to address 0019h in the HPI memory before to interrupt the DSP.



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