

Implementing Shared Memory Interface with a TMS320C54x DSP

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Abstract

This document describes how to share memory (SRAM, FIFO, Dual-Port RAM) between a Texas Instruments (TI) TMS320C54x digital signal processor (DSP) and Host or other DSP.

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Design Problem

How to share memory (SRAM, FIFO, Dual-Port RAM) between a C54x DSP and a Host or other DSP?

Design Solution

There are several ways to implement this. The simplest way is to use a C54x with a Host Port Interface, if it is suitable for the design and the 2Kx16 block of memory is large enough. This internal memory area is then available with no glue logic required. If you need the DSP to share external memory with a Host and the DSP can use HOLD mode, this situation is similar to that described in Designer's Notebook 63 (*Shared Memory Interface with a TMS320C5x DSP*). If in HOLD mode, the DSP can continue execution of the program from internal memory by resetting the Hold Mode (HM) bit.

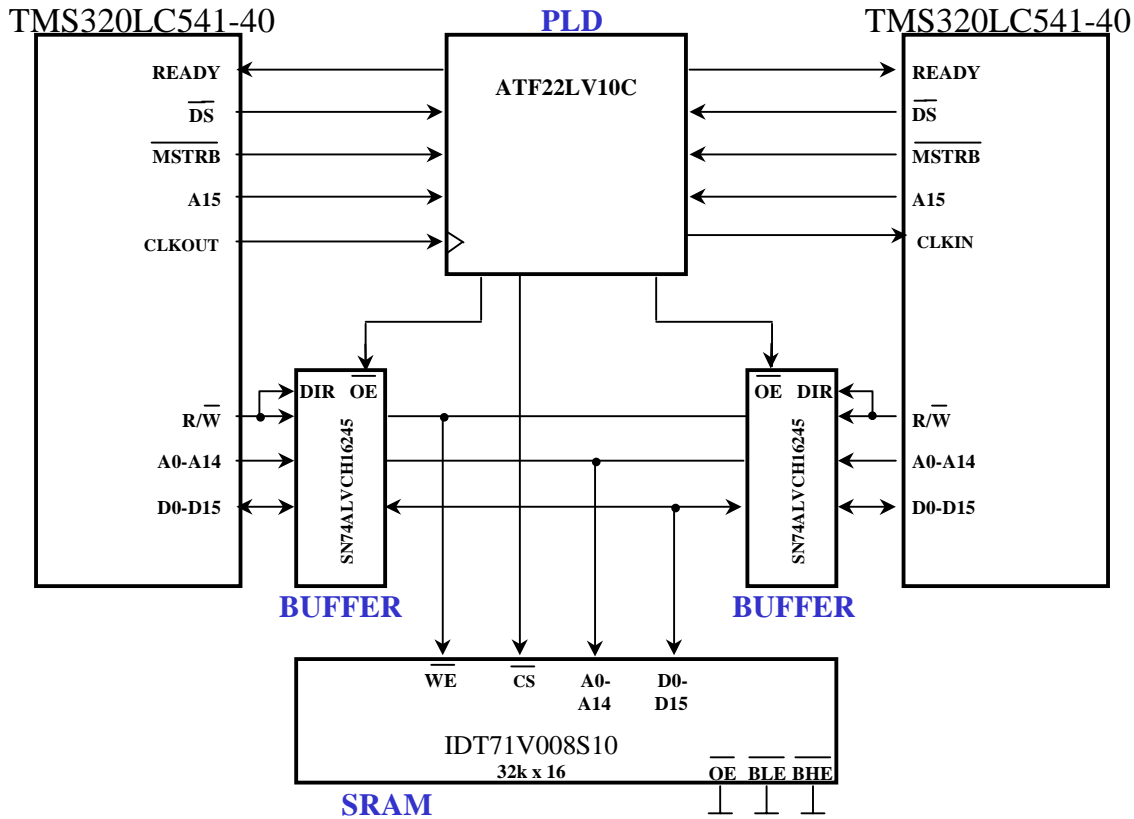
For information on how to use the HPI, see section 8.5 of the Texas Instruments *TMS320C54x User's Guide, Reference Set Volume 1*, 1997. HOLD mode is described in section 10.6 of the same user's guide. See also the data sheet used for this report, *TMS320C54x*, literature number SPRS039A.

The zero wait state access time for a C54x read from external memory is 15ns (using MSTRB). The required setup time for a read is 5ns. For writes the DSP uses two external bus cycles. I/O reads and writes take two cycles (using IOSTRB).

SRAM Used as a Global Memory Area without Using HOLD Mode

When SRAM is shared without HOLD mode, buffers need to be used. Figure 1 shows how two LC54x DSPs share a 32Kx16 memory area.

Figure 1. Two LC54x DSPs Sharing a 32Kx16 Memory Area



The DSPs are synchronized to run with the same clock so the CLKOUT from the left DSP corresponds to the CLKIN from the right DSP. SRAM is located in the upper half of the 64KW Data space (DS). SRAM accesses are arbitrated and synchronized to the clock with a Programmable Logic Device (PLD). Here the DSPs have equal priority to memory. Only one access from a DSP is allowed at a time with the next memory cycle going to the other DSP, if both are asking for the memory within the same arbitration period.

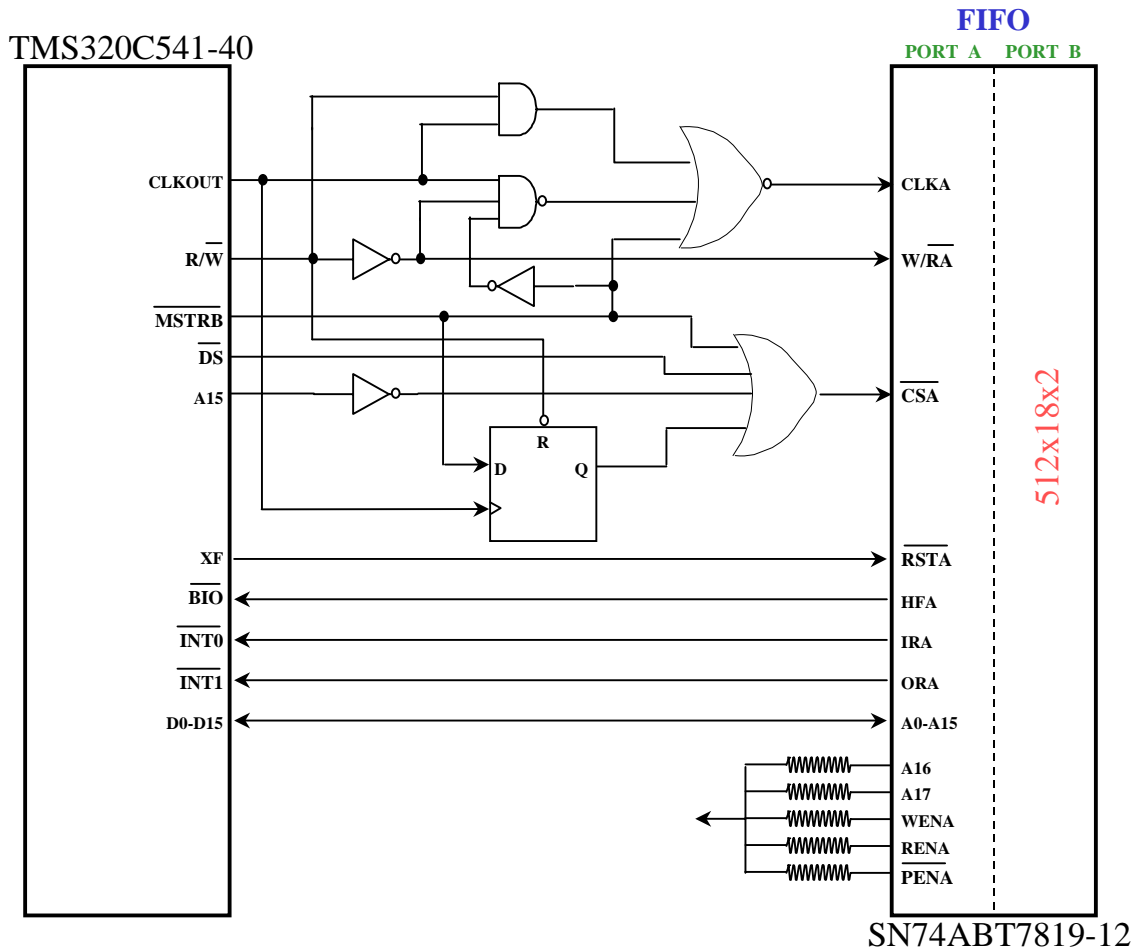
Data Strobe $\overline{\text{DS}}$, Address A15 , and Memory Strobe $\overline{\text{MSTRB}}$ indicate a valid memory request. These signals are decoded to the Chip Select $\overline{\text{CS}}$ line of SRAM. Write timing for the SRAM is $\overline{\text{CS}}$ controlled. The PLD also controls the access from buffers to SRAM with Output Enable $\overline{\text{OE}}$ lines. $\overline{\text{READY}}$ indicates to the DSP that the memory cycle can be served. Note that the DSP will perform ready-detection only if at least two software wait states are programmed into Software Wait State Register (SWWRS) for the upper half of data memory space.

The LC54x Address lines (A0-A14), Data lines (D0-D15), and the $\text{R}/\overline{\text{W}}$ line are all buffered to the SRAM. The $\text{R}/\overline{\text{W}}$ line also controls the direction of the buffer. Using buffers allows both DSPs to also have local external program (64KW) and data memory (32KW on lower half of data space).

FIFO Used as Shared Memory

Figure 2 shows how to use a bidirectional FIFO for communication between a TMS320C54x DSP and a Host.

Figure 2. Using a Bidirectional FIFO to Share Memory between a C54x DSP and Host



The FIFO used is an SN74ABT7819-12, clocked bidirectional FIFO with 512x18x2 organization. The DSP data bus is only 16 bits, so the A16-A17 lines of FIFO are connected to Vcc with resistors. The DSP has control over port A, which means that it writes to FIFOA-B and reads from FIFOB-A. The first read takes two cycles and successive reads take only one cycle.

If there are no interrupts, the buffer will be read as empty. For reads, the first value needs to be discarded because it is not yet valid data. However, after this initial state reads are single cycle. Writing always takes two cycles.



The Almost-Full/Empty flag (AF/AEA) is not used as we indicate Half-Full state of FIFOA-B with HFA line to BIO_ input of the DSP. When FIFOA-B becomes full, Input-Ready port A (IRA) goes low. The DSP is interrupted with the INTO_ line and this disables writes to the FIFO. When FIFOB-A becomes empty, the Output-Ready port A(ORA) goes low. The DSP is interrupted with the INT1_ line to stop reads to the FIFO.

The DSP also controls the FIFOA-B reset line RSTA_ with XF output. The FIFO is located in the upper 32KW half of data space with A15 address line. Valid DSP access to the FIFO is indicated with valid address, Data Strobe DS_, and Memory Strobe MSTRB_.

The critical FIFO timings to consider are the 9ns read access time and 3ns data setup time for write. The FIFO is clocked with the CLKA Low (L) to High (H) transition. Setup time for Chip Select CSA_ is 6ns.

Figure 3 shows the timing for a read cycle and Figure 4 shows the timing for a write cycle. The gate delay is allowed to be a minimum of 3ns and a maximum of 5.5ns. To make handling gate delays easier, you can have for NOR and OR faster gates, e.g., with min/max within the range 1ns - 4ns. The savings of 1.5ns on the maximum value can then be added to the maximum value of the AND and NAND. This gives a delay range of 3.0 -7.0ns to AND and NAND.

Figure 3. Read Cycle Timing Diagram

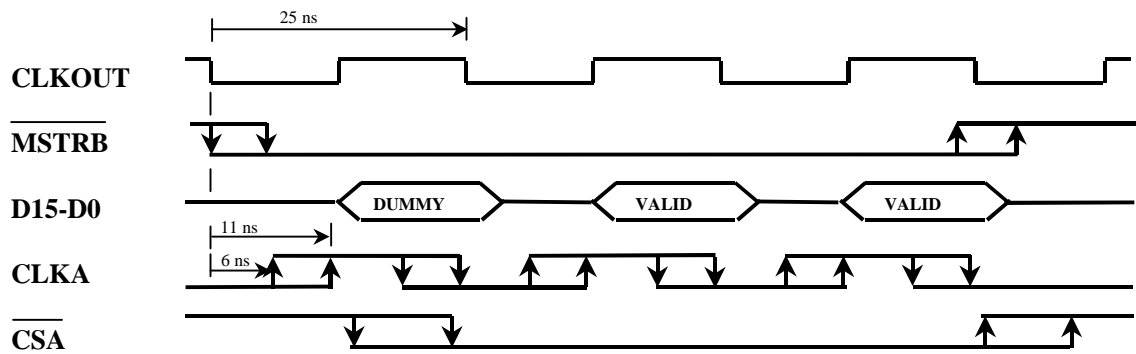
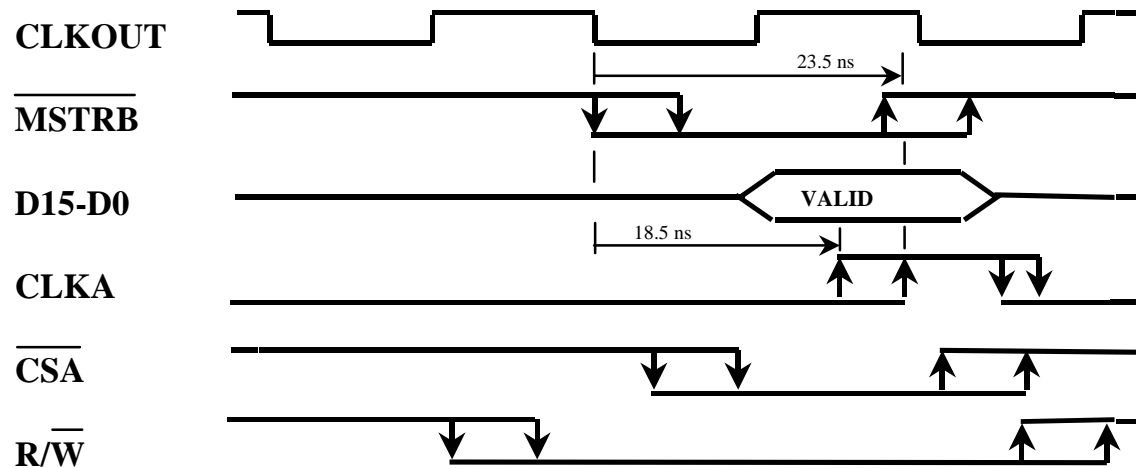


Figure 4. Write Cycle Timing Diagram





The C54x read cycle is activated with MSTRB_ going low, 0-5ns after CLKOUT goes low. MSTRB_ stays active as long as we have successive reads. The most critical timing is with CLKA. The L to H transition may occur earliest 3ns after CLKOUT H to L to eliminate extra clock, after we stop the reading. MSTRB_ L to H timing is -2/+3ns to CLKOUT H to L. The L to H on CLKA may occur latest 11ns after CLKOUT H to L. This enables meeting the maximum access time of 9ns and setup time of 5ns for the C54x data read.

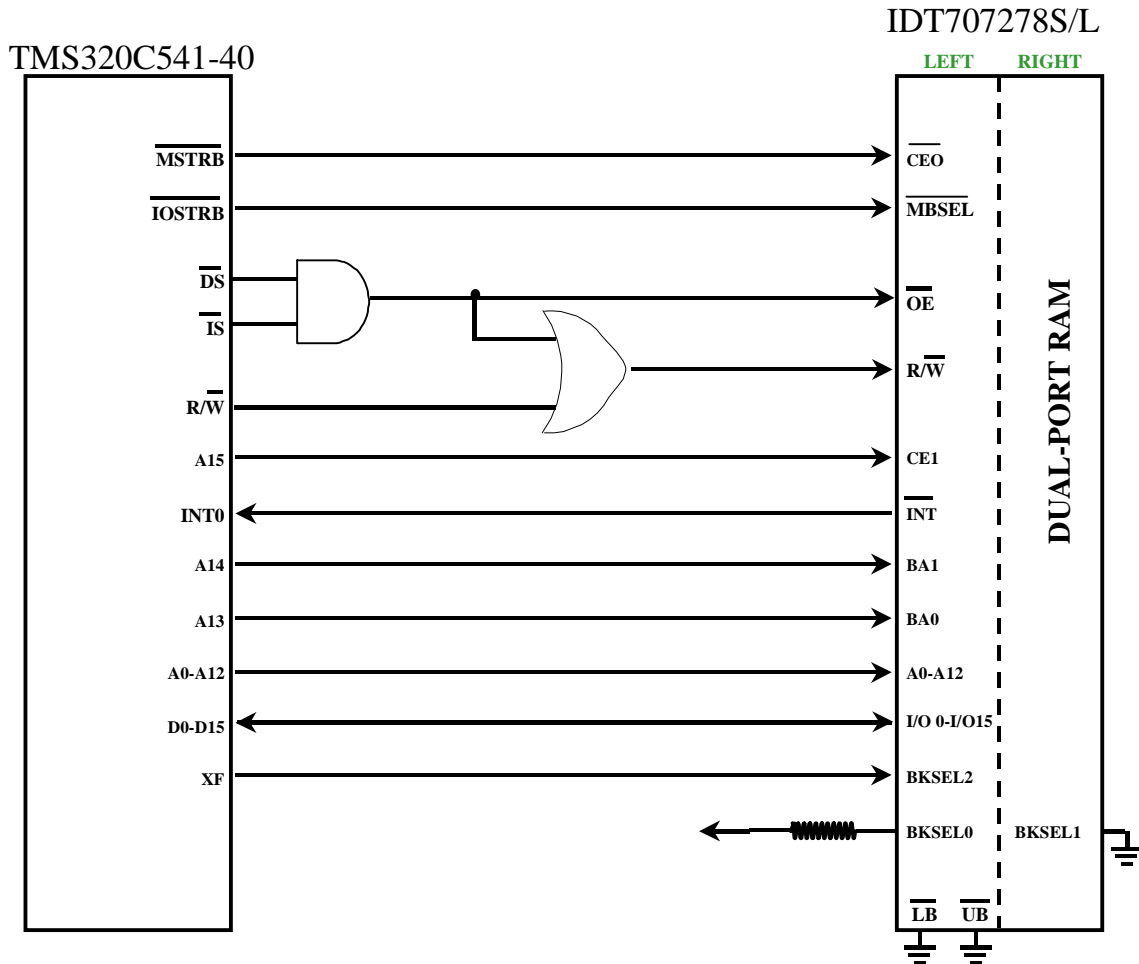
For the C54x write cycle, MSTRB_ goes low and high for every write cycle, which takes two CLKOUT cycles. The extra clock when CSA_ is active needs to be eliminated. This is done by taking the inverted MSTRB_ to the NAND input. Write data is valid after 10ns from second CLKOUT H to L plus 3ns for data setup, so after 13ns. Here CLKA L to H occurs earliest 18.5ns and latest 23.5ns after starting of second CLKOUT cycle.

Local external data memory can exist with the FIFO. If you want to use a smaller area from data space, more address lines need to be decoded.

Dual-Port RAM Used as Shared Memory

This interface uses a 32Kx16 Dual-Port SRAM (DPRAM) with external bank selects from IDT, IDT707278S/L. Figure 5 shows the interface. The DSP is connected to the Left port and the Host sharing the RAM to the Right port. The memory area consists of four 8Kx16 banks, to which multiple devices can connect by using the bank select inputs BKSEL0-3.

Figure 5. Using a DPRam to Share Memory between a C54x DSP and Host



In this design the DSP and Host have their own 8K block to be used as a local memory. BKSEL0 is used for Left port and BKSEL1 for Right port. Two upper 8K blocks are used for exchanging data between the processors. The DSP has control over BKSEL2 with XF line. The Host must be able to control BKSEL3 by toggling it. DPRAM is located in the upper 32KW of data space, so address line A15 works as CE1 Chip Select. Memory Strobe MSTRB_ works as a second Chip Select CE0_. I/O space is used for Mailbox control logic. I/O Strobe IOSTRB_ is connected to MBSEL_ to activate a valid Mailbox access. Address lines A13-A14 are used to choose an 8K bank with Bank Addresses BA0-BA1.

The access time of the DPRAM is 15ns from chip select, so no wait state is needed with 40MIPS DSP. Access time from OE_ signal is 9ns, so we have 6ns for the AND gate to connect data and I/O spaces.



When the mailing (data on BKSEL2 RAM block) to the Right port is ready, the DSP changes XF from H to L to give access to the Right port and sends Mailbox2 interrupt. The Host then changes his BKSEL3 signal L to H to give this RAM area to the Left port and sends Mailbox3 interrupt. The DSP will be interrupted on the INTO_ interrupt line. The DSP will clear Mailbox3 interrupt and read the new data from Host processor. After reading data, the DSP writes new data to BKSEL3 RAM. When this access has completed, the DSP sends the Mailbox3 interrupt. If the Host is quicker than the DSP in reading and writing the data, it will initiate the change of RAM blocks sooner. The response from the DSP should be the same as the Host's response to an interrupt from DSP.

The configuration shown allows you to add external data memory to the lower 32KW of the DSP data space. External program space is also available. Here I/O space is used without decoding. The timing to add a decoder is not critical, with I/O accesses at two cycles.

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