TMS320C6000 Expansion Bus to MC68360 Microprocessor Interface

Zoran Nikolic *DSP Applications*

ABSTRACT

This application report describes how to interface the Motorola MC68360 quad integrated communications controller (QUICC) to the Expansion Bus of the Texas Instruments TMS320C6000™ (C6000™) digital signal processor (DSP). The document contains the following elements:

- A block diagram of the interface and PAL equations.
- Information required to configure the MC68360.
- Timing diagrams illustrating the interface functionality.

Note:
The information presented in this application report has been verified using VHDL simulation.

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1 MC68360 Interface

The expansion bus is configured to operate in the asynchronous host port mode. Note that the internal expansion bus arbiter is disabled. The C6000 requests the expansion bus only if it needs to access a FIFO or asynchronous I/O port (not shown in the block diagram).

Figure 1 shows the interface diagram. The TMS320C6000 DSP is not 5-V tolerant; therefore, voltage translation is needed if a 5-V host is used. A bus switch can be used to convert voltage (for example, the SN74CBTD16211). The bus switch is not shown in the diagram. Table 1 lists the expansion bus connections.

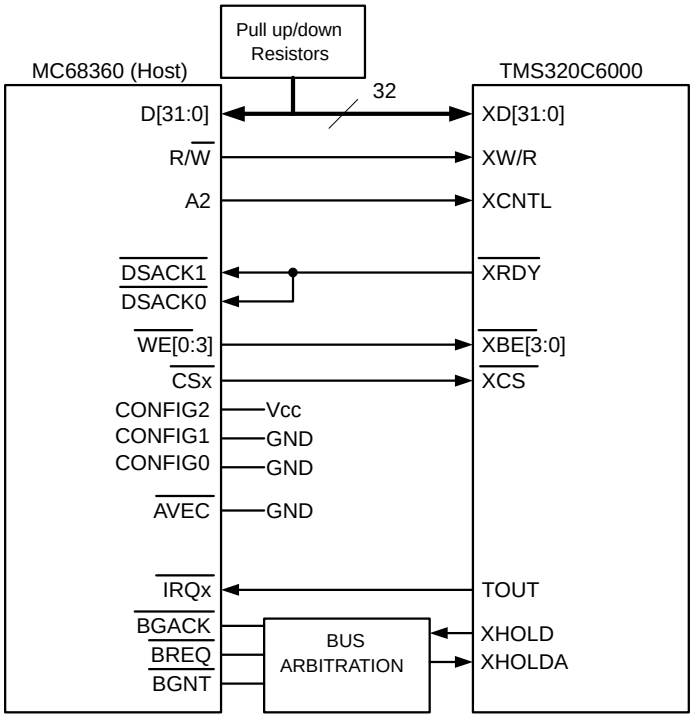


Figure 1. Block Diagram of Interface Between MC68360 (Host) and Expansion Bus

Table 1. MC68360 to TMS320C6000 Expansion Bus Connections

Expansion Bus Signal	MC68360 Pin	Comments
XCNTL	A[2]	Address bit of MC68360 is used as control signal.
X$\overline{W}$/R	R/$\overline{W}$	Indicates a read or write access
XD[31:0]	D[31:0]	Data lines
$\overline{XCS}$	$\overline{CSx}$	Any chip-select of MC68360 can be connected to $\overline{HCS}$ as the chip select signal. This also serves as the data strobe signal in this case (since $\overline{DS}$ of MC68360 is not used as data strobe).
$\overline{XBE}$[3:0]	$\overline{WE}$[0:3]	Byte enables.
$\overline{HRD}$	$\overline{DSACK1}$ $\overline{DSACK2}$	The SPS bits in the MC68360 option registers must be set to indicate that $\overline{DSACK}$ is generated externally by the expansion bus. Refer to the *MC68360 User's Manual* for details.
-	CONFIG[2:0]='100'	The configuration pins are set to CONFIG[2:0]='100'. Therefore the CPU is enabled, global chip select port is 32-bit size, and the MBAR register is at 0x003FF00.
-	AVEC='0'	The Auto Vector input function is selected in normal operation.
XHOLD	Glue is required to connect to $\overline{BR}$, $\overline{BG}$, $\overline{BGACK}$.	Bus arbitration signal. Note that the internal bus arbiter of the C6000 is disabled (please see Figure 1).
XHOLDA	Glue is required to connect to BR, BG, BGAC.	Bus arbitration signal. Note that the internal bus arbiter of the C6000 is disabled (please see Figure 1).
TOUT	$\overline{IRQx}$	User can select interrupt level ($\overline{IRQ1}$ to $\overline{IRQ7}$). Priority level 7 interrupt is a special case. Level 7 interrupts are non-maskable interrupts (NMI). $\overline{IRQ}$7 is a level-sensitive input and must remain low until the second instruction processing module (CPU32+) returns an interrupt acknowledge cycle for interrupt 7. (See the *MC68360 User's Manual* for a detailed description.) Because the expansion bus does not have a dedicated interrupt output pin, a timer pin TOUT is used as a general-purpose output to generate interrupt.

The auto-vector (AVEC) signal is used to terminate interrupt acknowledge cycles, indicating that the QUICC should internally generate a vector (auto-vector) number to locate an interrupt handler routine. AVEC is ignored during all other bus cycles.

The external bus arbiter used in this interface is shown in Figure 2.

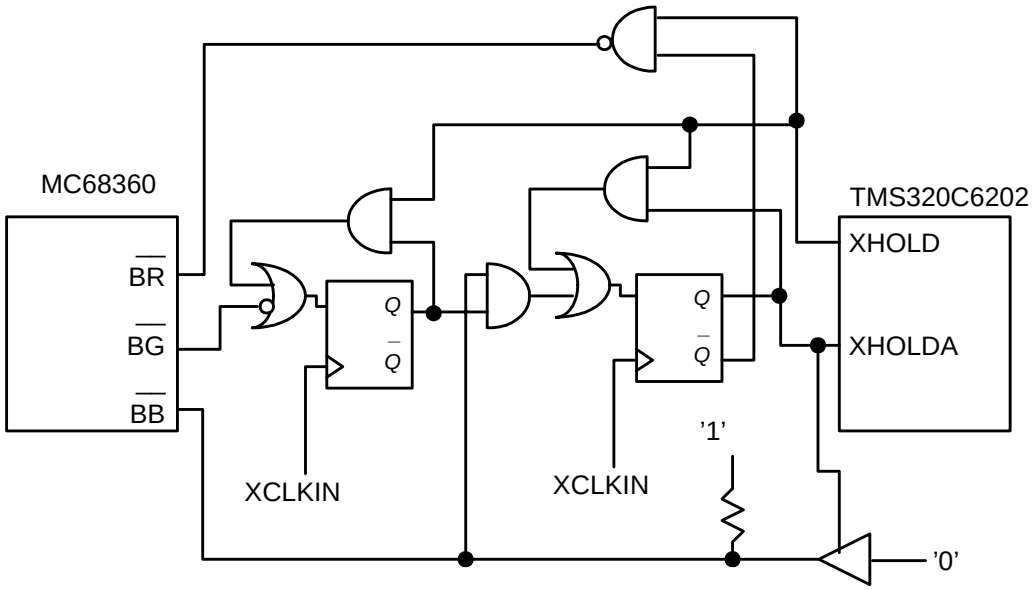


Figure 2. Block Diagram of External Bus Arbiter Used in Interface Between MC68360 (Host) and C6000 Expansion Bus

2 Configuration

The QUICC is comprised of three modules:

- CPU32 + core
- System integration module (SIM60)
- Communication processor module (CPM)

The memory controller is a sub-block of the SIM60 that is responsible for up to eight general-purpose chip-select lines. The general-purpose chip selects are available on lines CS0-CS7. CS0 also functions as the global (boot) chip select for accessing the boot EPROM. The SIM60 supports a glue-less interface to expansion bus.

All internal memory and registers of the MC68360 occupy a single 8-KB memory block that is relocatable along 8-KB boundaries. The location is fixed by writing the desired base address of the 8-KB memory block to the MBAR. The 8-KB block is divided into two 4-KB sections. The RAM occupies the first section; the internal registers occupy the second section. The LSB (least-significant bit) of the MBAR register indicates when the contents of the MBAR are valid (if the bit is equal to one the content is valid).

The MC68360 general-purpose chip-selects are controlled by the global memory register (GMR) and the memory controller status register (MSTAT). There is one GMR and MSTAT in the memory controller. The MSTAT reports write-protect violations and parity errors for all banks. The 32-bit read-write GMR contains selections that are common to the entire memory controller. The GMR is used to control global parameters for memory banks. The DPS bit-field of the GMR register must be set to DPS[1:0]='11' to enable external DSACKx response. The PBEE bit of the GMR register should be set to zero to disable parity-bus error detection.

Each SRAM bank has a base register (BR) and an option register (OR). The MC68360 has eight identical sets of two registers, the BR and OR.

The configuration of the BR0 and OR0 registers is shown in Table 2 and Table 3.

Table 2. Base Register 0 (BR0) Relevant Bits (MC68360)

Bit Field	Description	Value
CSNTQ	CS negate timing This bit is used to determine when CS is negated during an internal QUICC or external QUICC/MC68030-type bus master write cycle.	Set bit to 0 (CS negated normally).
TRLXQ	Timing relax This bit delays the beginning of the internal QUICC or external QUICC/MC68030-type bus master cycle to relax the timing constraints on the user.	Set bit to 0 (do not relax timing).
PAREN	Parity checking enable	0 = Parity checking disabled
V	Valid Bit	1 = Content of BR0 and OR0 pair is valid
BA31-BA11	Base address The base address field, the upper 21 bits of each BR, and the function field are compared to the address on the address bus to determine if a DRAM/SRAM region is being accessed by an internal QUICC master.	Base address of SRAM bank 0 was set to 0x09000000.

The option register is a 32-bit read-write register that can be accessed at any time.

Table 3. Option Register (OR) Relevant Bits (MC68360)

Bit Field	Description	Value
DSSEL	Dynamic RAM select This bit determines if the bank is SRAM or DRAM.	Set bit to 0 (SRAM).
SPS1-SPS0	SRAM port size Because external DSACKx is used, SPS[1:0] = 11.	SPS0 = 1 SPS1 = 1
AM27-AM11	Address mask Mask any of the corresponding bits in the associated BR. By masking the address bits independently, external devices of different address range sizes can be used. Any set bit causes the corresponding address bit to be used in the comparison with the address pins.	All base address and function code bits will be used in the bank-hit comparison (all bits of the AM bit-field are set to one).
TCYC3-TCYC0	Cycle length in clocks	Because external DSACKx is selected with SPS, do not set TCYC to zero. TCYC[3:0] = '1111'

The module configuration register (MCR) that controls the SIM60 configuration can be read or written to at any time. Set the BSTM bit of the MCR register to zero to enable asynchronous timing on the bus signals. Set the ASTM bit of the MCR register to zero to enable asynchronous timing on the arbitration signals.

The Port E pin assignment register (PEPAR) controls the I/O pins associated with port E. Set the CF1MODE bit field of the PEPAR register to CF1MODE[1:0] = '00' (CONFIG1 input pin function is chosen). Set bit 7 of the PEPAR to one (to select the WE0-WE3 output functions). Set bit 0 of the PEPAR register to zero (to select the AVEC input function).

The TMS320C6000 boot configuration is presented in Table 4.

Table 4. TMS320C6000 Boot Configuration via Pull-Up/Pull-Down Resistors on XD[31:0]

Field	Description
RWPOL	Determines polarity of expansion bus read/write signal RWPOL = 1, XR/W_
HMOD	Host mode (status in XB HPIC) HMOD = 0, external host interface is in asynchronous slave mode.
XARB	Expansion bus arbiter (status in XBGC) XARB = 1, internal expansion bus arbiter is disabled.
FMOD	FIFO mode (status in XBGC)
LEND	Little-endian mode LEND = 1, system operates in little-endian mode.
BootMode[4:0]	Dictates the boot mode of the device, including host port boot, ROM boot, memory map selection. For a complete list of boot-modes, see the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

3 Timing Verification

To verify proper operation, two functions have been examined:

- An MC68360 write to the expansion bus.
- An MC68360 read from the expansion bus.

In each instance, timing requirements were compared for each of the devices. The results are shown in Figure 3, Figure 4, Table 5, and Table 6.

The interface was functionally verified using VHDL simulation (Synopsys SmartModel of the MC68360 was used in the test bench). The timing diagrams shown in Figure 3 and Figure 4 illustrate a read and a write initiated by the MC68360.

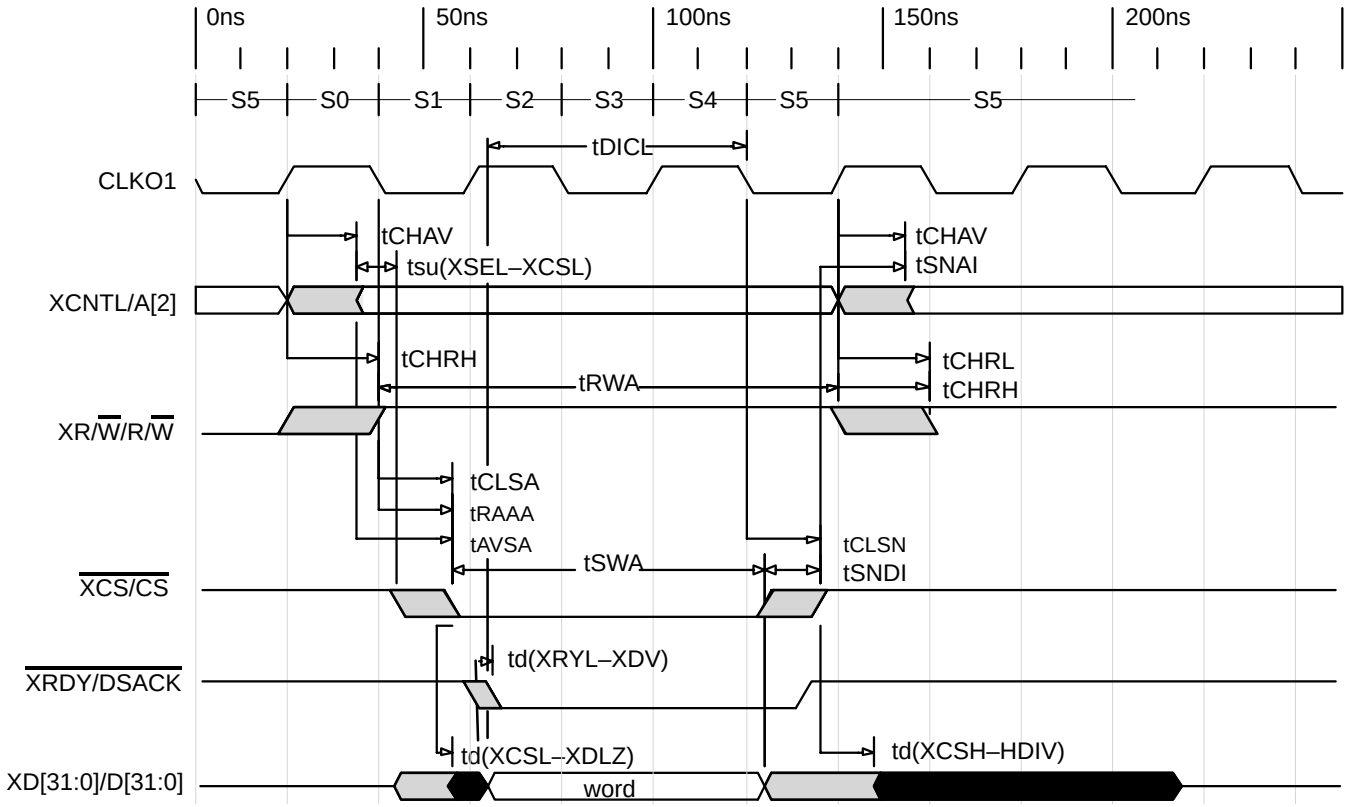


Figure 3. MC68360 (Host) Performs Read from Expansion Bus Asynchronous Host Port Interface

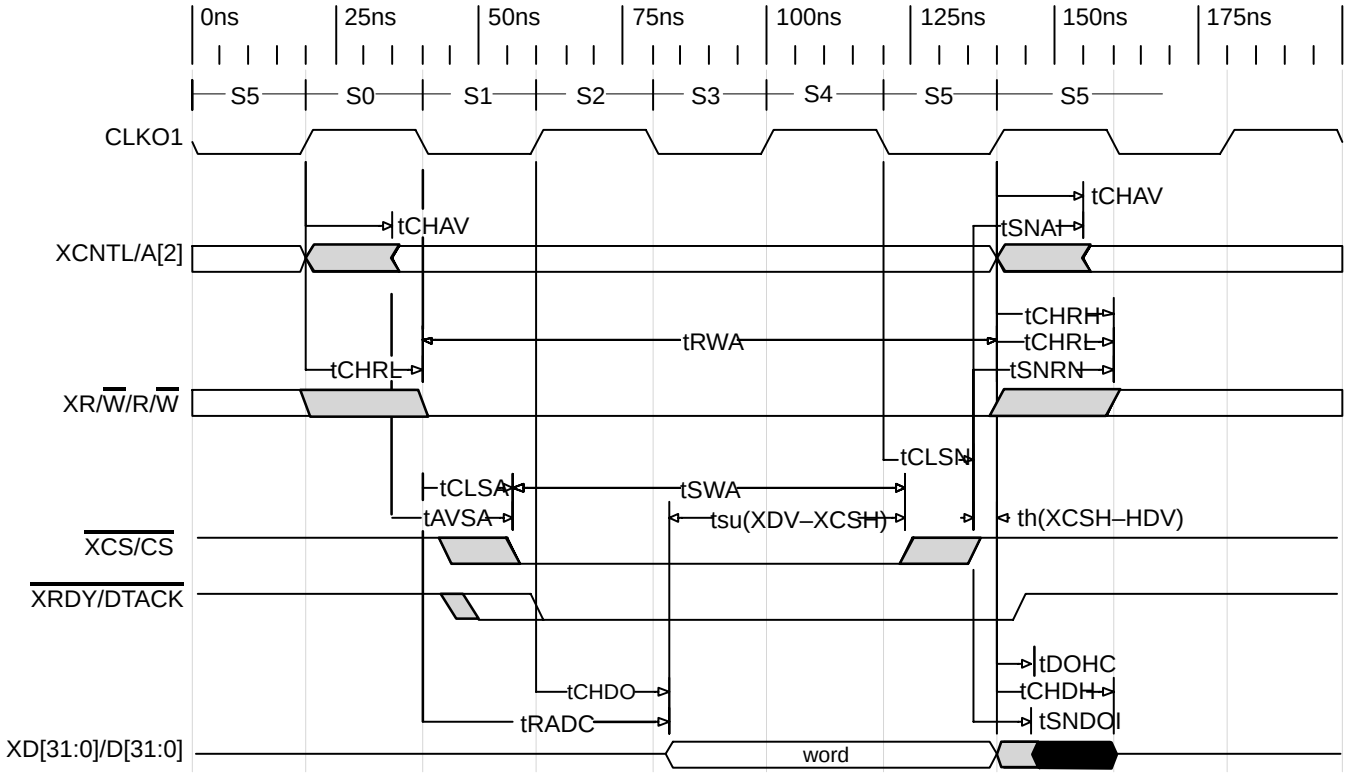


Figure 4. MC68360 (Host) Performs Write to Expansion Bus Interface

Table 5. Timing Requirements for TMS320C6000

C6000 Symbol	MC68360 Symbol	Parameter	C6000‡ Min (ns)	MC68360 Min (ns)
tw(XCSL)	tSWA	Pulse width of $\overline{\text{HCS}}$ low	16	75
tsu(SEL-XCSL)	tAVSA	Setup time, select signals valid before ($\overline{\text{XCS}}$) low	1	10
th(XCSL-SEL)	tSNAI+tSWA	Hold time, select signals valid after ($\overline{\text{XCS}}$) low	3*	85
tsu(XDV-XCSH)	1.5*tcyc@ -tCHDO+tCLSN	Setup time, host data valid before ($\overline{\text{HCS}}$) high (WRITE SETUP TIME)	1	41
th(XCSH-XDV)	tSNDOI	Hold time, host data valid after ($\overline{\text{HCS}}$) high	3	10

tcyc@ denotes one clock cycle time of the MC68360. At 25-MHz operating frequency, tcyc = 40 ns

* th(XCSL-SEL) = 3.4 ns for C6203 processor.

‡ In this case C6000 refers to the C6202(B), C6203, and C6204 devices.

Table 6. Timing Requirements for MC68360

C6000 Symbol	MC68360 Symbol	Parameter	C6000 Min (ns)	MC68360 Min (ns)
td(XCSH-HDIV)	tSNDI	Input data hold time from $\overline{CS}$ negated	0	0
2tcyc@-tCLSA-td(XCSL-HDV)	tDICL	Data-in valid to clock low (READ SETUP TIME)	60	1

tcyc@ denotes one clock cycle time of the MC68360. At 25-MHz operating frequency, tcyc = 40 ns.

In Figure 3 and Figure 4, timing parameters are named in the same way as those in the data-sheets for the TMS320C6000 and MC68360. Actual timing parameter values are listed in Appendix A and Appendix B.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of the MC68360 and TMS320C6000. This interface is based on an MC68360/25-MHz device operating at 3.3 V and a TMS320C6000 device at any frequency.

4 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6202, TMS320C6202B Fixed-Point Digital Signal Processor* (SPRS104).
3. *TMS320C6203 ,TMS320C6203C Fixed-Point Digital Signal Processor* (SPRS086).
4. *TMS320C6204 Fixed-Point Digital Signal Processor* (SPRS152).
5. MC68360 User's Manual*, Motorola, Inc.*

Appendix A MC68360 Timing Requirements

Table A–1. Motorola MC68360 Timing Parameters

Characteristic	Symbol	Min (ns)	Max (ns)
CLKO1 high to address, FC valid [6]	tCHAV	0	15
CLKO1 high to address, FC invalid [8]	tCHAZn	0	
CLKO1 low to $\overline{CS}$ asserted [9]	tCLSA	4	16
AS to DS or $\overline{CS}$ asserted [9A]	tSTSA	-6	6
AS to $\overline{CS}$ asserted [9C]	tSTCA	14	26
Address valid to AS,$\overline{CS}$, OE asserted [11]	tAVSA	10	
CLKO1 low to $\overline{CS}$ negated [12]	tCLSN	4	16
AS,DS,$\overline{CS}$,OE,WE negated to address, FC invalid (address hold) [13]	tSNAI	10	
AS,$\overline{CS}$,OE and DS (read) width asserted [14]	tSWA	75	
AS,DS,$\overline{CS}$,OE width negated [15]	tSN	35	
CLKO1 high to AS,DS,R/$\overline{W}$ high impedance [16]	tCHSZ		40
AS,DS,$\overline{CS}$,WE negated to R/W high [17]	tSNRN	10	
CLKO1 high to R/W high [18]	tCHRH	0	20
CLKO1 high to R/W low [20]	tCHRL	0	20
R/W high to AS,$\overline{CS}$, OE asserted [21]	tRAAA	10	
R/$\overline{W}$– low to $\overline{DS}$ asserted (Write) [22]	tRASA	47	
CLKO1 high to Data-Out valid [23]	tCHDO		23
DS,$\overline{CS}$,WE negated to Data-Out invalid (Data-Out hold) [25]	tSNDOI	10	
Data Out valid to DS asserted (write) [26]	tDVSA	10	
Data In to CLKO1 low (Data setup) [27]	tDICL	1	
AS,DS, negated to $\overline{DSACK}$ negated [28]	tSNDN	0	50
DS,$\overline{CS}$,OE negated to Data In invalid (Data In hold) [29]	tSNDI	0	
DS,$\overline{CS}$,OE negated to Data In high Z [29A]	tSHDI		40
$\overline{DSACK}$ asserted to $\overline{DSACK}$ valid (Skew) [31A]	tDADV		10
R/$\overline{W}$ width asserted (write or read) [46]	tRWA	100	
Async input setup time [47A]	tAIST	5	
Async input hold time [47B]	tAIHT	10	
Data Out from CLKO1 high [53]	tDOHC	0	
CLKO1 high to Data-Out high Z [54]	tCHDH		20
R/W asserted to data bus impedance change [55]	tRADC	25	

The timing requirements in Table A–1 are provided for quick reference only. For detailed description, notes, and restrictions, please see the *MC68360 User's Manual*.

Appendix B TMS320C6000 Timing Parameters

Table B–1. TMS320C6000 Timing Parameters (Asynchronous Host Port)

Characteristic	Symbol	Min (ns)	Max (ns)
Pulse duration, XCS low	Tw(XCSL)	4P†	
Pulse duration, XCS high	Tw(XCSH)	4P†	
Setup time, expansion bus select signals valid before XCS low	Tsu(XSEL-XCSL)	1	
Hold time, expansion bus select signals valid after XCS low	Th(XCSL-XSEL)	3*	
Hold time, XCS low after XRDY low	Th(XRYL-XCSL)	1.5+P†	
Setup time, XBE[3:0]/XA[5:2] valid before XCS high	Tsu(XBEV-XCSH)	1	
Hold time, XBE[3:0]/XA[5:2] valid after XCS high	Th(XCSH-XBEV)	3	
Setup time, XDx valid before XCS high	Tsu(XDV-XCSH)	1	
Hold time, XDx valid after XCS high	Th(XCSH-XDV)	3	
Delay time, XCS low to XDx low impedance	Td(XCSL-XDLZ)	0	
Delay time, XCS high to XDx invalid	Td(XCSH-XDIV)	0	12
Delay time, XCS high to XDx high impedance	Td(XCSH-XDHZ)		4P†
Delay time, XRDY low to XDx valid	Td(XRYL-XDV)	-4	1
Delay time, XCS high to XRDY high	Td(XCSH-XRYH)	0	12

† P is a clock period of the TMS320C6000 core.
* Th(XRYL–XCSL) = 3.4 ns for the TMS320C6203 processor.

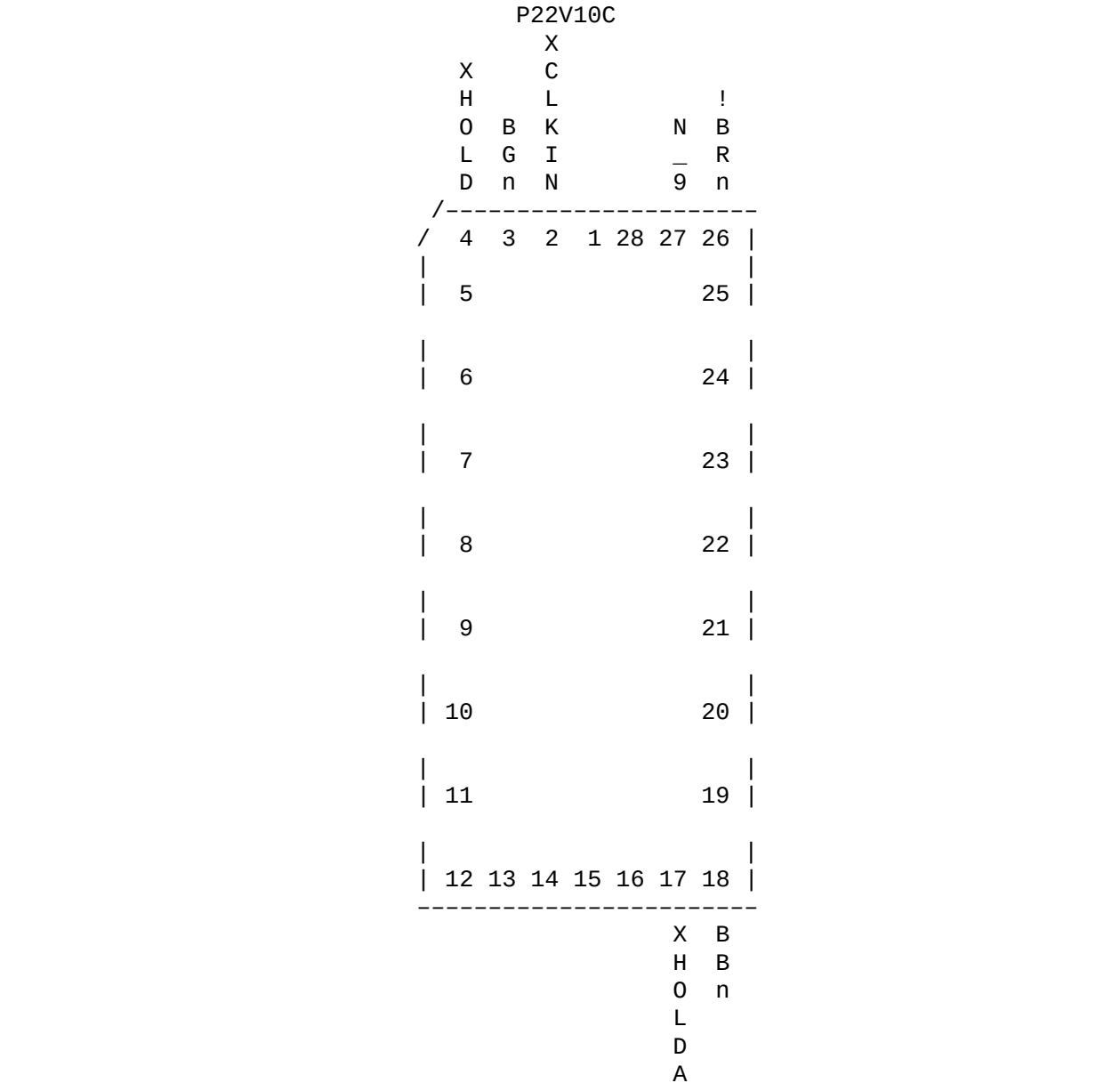
The timing requirements in Table B–1 are provided for quick reference only. For detailed description, notes, and restrictions please see the corresponding Fixed-Point Digital Signal Processor data sheet.

Appendix C External Bus Arbiter PAL Equations

```
Synario 3.10  –  Device Utilization Chart         Thu Apr 01 14:13:34 1999
bus_arb.bls
------------------------------------------------------------------------------
--
Module                   : 'bus_arb'
------------------------------------------------------------------------------
--
Input files:
    ABEL PLA file        : bus_arb.tt3
    Device library       : P22V10C.dev
Output files:
    Report file          : bus_arb.rep
    Programmer load file : bus_arb.jed
------------------------------------------------------------------------------
--
```

```
                                                                        Page 2
Synario 3.10  –  Device Utilization Chart         Thu Apr 01 14:13:34 1999
bus_arb.bls
P22V10C Programmed Logic:
--------------------------------------------------------------------------------
--
BBn     = (0);
BBn.OE  = (  XHOLDA.Q );
BRn     = !(  !XHOLDA.Q & XHOLD );
XHOLDA.D   = (  N_9.Q & XCLKIN
             #   XHOLDA.Q & XHOLD ); ” ISTYPE ’BUFFER’
XHOLDA.C   = (  XCLKIN );
N_9.D   = (  !BGn
           #   N_9.Q & XHOLD ); ” ISTYPE ’BUFFER’
N_9.C   = (  XCLKIN );
```

Synario 3.10 – Device Utilization Chart Thu Apr 01 14:13:34 1999
bus_arb.bls
P22V10C Chip Diagram:



```
                                                                        Page 4
Synario 3.10  –  Device Utilization Chart         Thu Apr 01 14:13:34 1999
bus_arb.bls
P22V10C Resource Allocations:
--------------------------------------------------------------------------------
        Device         | Resource  |   Design    |
       Resources       | Available | Requirement | Unused
=======================|===========|=============|==============
                       |           |             |
Input Pins:            |           |             |
                       |           |             |
          Input:       |     12    |      3      |    9 ( 75 %)
                       |           |             |
Output Pins:           |           |             |
                       |           |             |
          In/Out:      |     10    |      4      |    6 ( 60 %)
          Output:      |      –    |      –      |    –
                       |           |             |
Buried Nodes:          |           |             |
                       |           |             |
          Input Reg:   |      –    |      –      |    –
          Pin Reg:     |     10    |      2      |    8 ( 80 %)
          Buried Reg:  |      –    |      –      |    –
```

Synario 3.10 – Device Utilization Chart Thu Apr 01 14:13:35 1999
bus_arb.bls
P22V10C Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
BBn	18	0	10	10
BRn	26	1	10	9
XHOLDA.D	17	2	8	6
N_9.D	27	2	8	6

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
XCLKIN	2	CLK/IN
BGn	3	INPUT
XHOLD	4	INPUT

Page 6
Synario 3.10 – Device Utilization Chart Thu Apr 01 14:13:35 1999
bus_arb.bls
P22V10C Unused Resources:

Pin Number	Pin Type	Product Terms	Flip–flop Type
5	INPUT	–	–
6	INPUT	–	–
7	INPUT	–	–
9	INPUT	–	–
10	INPUT	–	–
11	INPUT	–	–
12	INPUT	–	–
13	INPUT	–	–
16	INPUT	–	–
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D

```
                                                                                Page 7
Synario 3.10  –  Device Utilization Chart         Thu Apr 01 14:13:35 1999
bus_arb.bls
P22V10C Fuse Map:
--------------------------------------------------------------------------------
--
       0          10         20         30         40
   44: ---------- ---------- ---------- ---------- ----
   88: -----X---- ---------- ---------- ---------- ----
  132: ---X----X- ---------- ---------- ---------- ----
  440: ---------- ---------- ---------- ---------- ----
  484: --------X- ---------- ---------- --------X- ----
 4884: ---------- ---------- ---------- ---------X ----
 5368: ---------- ---------- ---------- ---------- ----
 5412: X--X------ ---------- ---------- ---------- ----
 5456: --------X- ---------- ---------- ---------X ----
       0          10
 5808: –XX–XXXXXX XXXXXX---X
```

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