Application Report
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Using Boundary Scan on the TMS320VC5420

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ABSTRACT

The Texas Instruments (TI™) TMS320VC5420 DSP implements limited boundary scan capability with respect to standard IEEE 1149.1 boundary scan devices. This application report contains a description of the 'VC5420 boundary scan implementation and information about how to use it with other boundary scan tools and devices.

The material covered in this application report assumes the reader is familiar with the boundary scan concepts defined by IEEE Standard 1149.1. An overview of these concepts is presented in the IEEE Standard 1149.1 (JTAG) Testability Primer (literature number SSYA002C). For detailed information on the operation and requirement for boundary scan, refer to the IEEE standard itself. Copies of the standard are available from IEEE at 1-800-678-IEEE.

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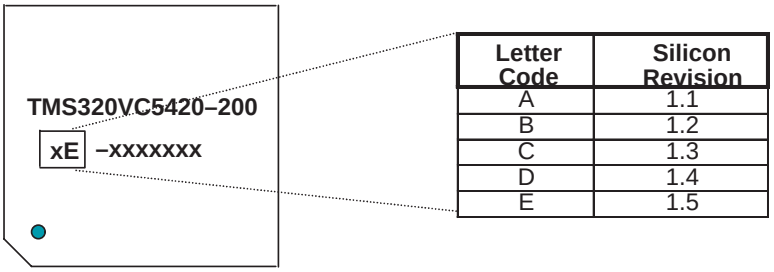
1.1 TMS320VC5420 Silicon Revision Requirements

In the ’VC5420 revisions 1.1 through 1.4, the boundary scan capability does not operate properly. On these device revisions boundary scan tests cannot be performed. If these device revisions are operated in EXTEST or SAMPLE/PRELOAD, the scan chain is broken and the board test will fail.

The ’VC5420 boundary scan implementation described in this document applies to silicon revisions 1.5 and higher. The device silicon revision is identified by a code number printed on the package as shown in Figure 1:



Letter Code	Silicon Revision
A	1.1
B	1.2
C	1.3
D	1.4
E	1.5

Figure 1. Determining the Silicon Revision from the Package Symbolization

The BYPASS function of the scan chain operates correctly on all revisions, so revisions 1.1-1.5 can be included in the scan chain if the boundary scan ATPG tool is configured to always keep these devices in BYPASS mode. Consider that according to the IEEE standard 1149.1, when a device is in BYPASS mode, its pins operate in their normal (non-test) function.

CAUTION:

Although the ’VC5420 pins are described as inputs in the BSDL files (see the following section), pins that have output or input/output capability in their functional mode may be driven when the boundary scan test is in BYPASS mode. Extreme care must be taken to prevent drive contention on these pins, or damage to the device may occur.

1.2 Observe-only Boundary Register

The ’VC5420 implements “observe-only” boundary scan cells on the device pins. These cells are capable of observing (reading) the state of a pin driven by another source but are not capable of controlling (writing) the state of the pin. Devices that are fully compliant with IEEE 1149.1 implement boundary scan cells that match the operational states of the pins. If the device pin is only an input, observe capability is present. If the pin is only an output, control capability is present. If the pin can be either an input or an output, both observe and control capability are present. Since all pins on the ’VC5420 have observe-only capability, some limitation is implied on testability depending on the configuration of the board connections.

Table 1 and Figure 2 show the extent of testability between the ’VC5420 and another fully compliant boundary scan device in a board or system. Since the ’VC5420 has observe-only boundary scan cells on each pin, the ability to test a net (a connection between 2 or more pins) is determined by the nature of the boundary scan cell on the other side of the net since the ’VC5420 cannot drive the net through boundary scan. As long as there is a boundary scan cell connected to the net that is capable of driving the net (as indicated by the arrows in Figure 2), the net will be testable. Table 1 shows the combinations of boundary scan cells that could be present on a net and the corresponding ability to test that net. Although all of the combinations of pin types are shown, the rows in gray are connections that are not valid from a functional standpoint.

Table 1. Testability of Boundary Scan Nets Connected to the ’VC5420 Based on Boundary Scan Cell (BSC) Types

’VC5420 Functional pin type	’VC5420 BSC type	Other Device(s) Functional Pin type	Other Device(s) BSC type	Testability
Input	Observe	Input	Observe	
Input	Observe	Output	Control	Testable
Input	Observe	I/O	Observe/Control	Testable
Output	Observe	Input	Observe	Not testable
Output	Observe	Output	Control	
Output	Observe	I/O	Observe/Control	Testable
I/O	Observe	Input	Observe	Not testable
I/O	Observe	Output	Control	Testable
I/O	Observe	I/O	Observe/Control	Testable

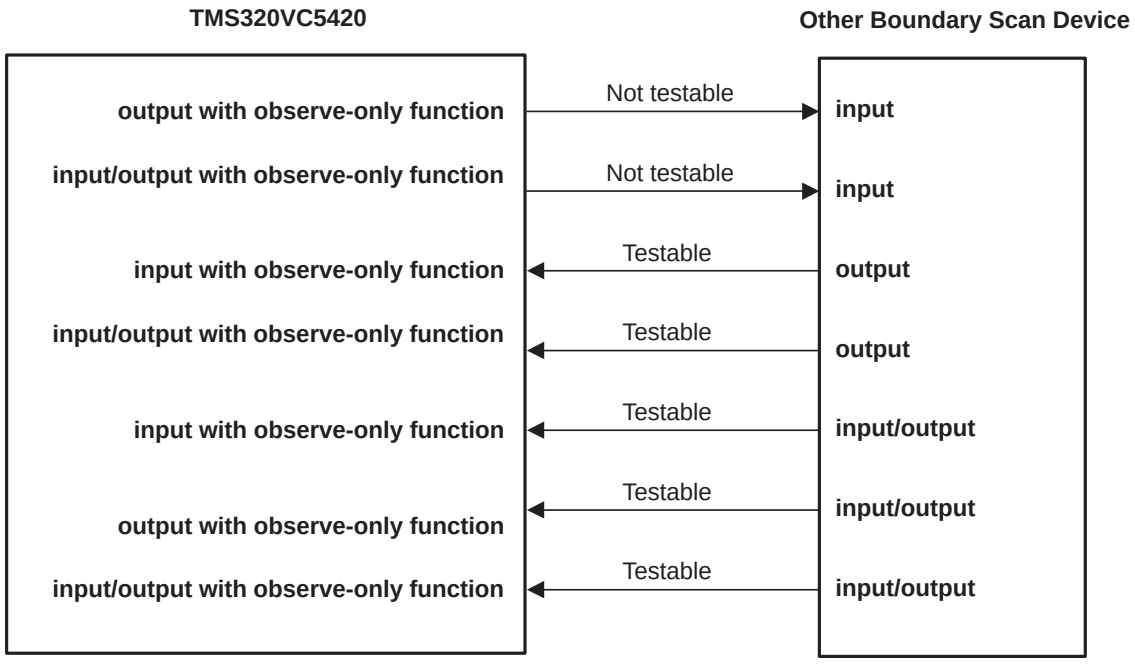


Figure 2. Testability of Boundary Scan Nets Connected to the ’VC5420

In the ’VC5420 Boundary Scan Description Language (BSDL) files, the description of the observe-only capability is implemented by describing all device pins as inputs in the logical port declaration and in the boundary register description. Describing the pins as inputs conveys to boundary scan automatic test pattern generation (ATPG) tools that control capability on these pins is not available. The ATPG tools will then look for other boundary scan cells to control the testable nets.

1.3 Techniques to Increase Board Testability

Some of the limitations of the observe-only capability on the ’VC5420 pins can be overcome with considerations in the board design. Two techniques that can be used to increase the board test coverage are the use of boundary scan buffers/transceivers and the addition of test points.

If the board design requires buffers or transceivers between the ’VC5420 and other devices in the system, the choice of boundary scan tranceivers can increase test coverage. The connection shown in Figure 3 between a ’VC5420 output pin and an input pin on another boundary scan device would normally not be testable. With the addition of a bidirectional boundary scan transceiver between the two devices, each of the pins can now be driven by the boundary scan cells on the transceiver. Many ATPG tools will recognize the ability to use the bidirectional boundary scan cells on the transceiver as drivers for the other pins to which they are connected. This structure provides increased test coverage in a boundary scan only environment where no tester resources are available.

For information on boundary scan logic products, refer to:
http://www.ti.com/sc/docs/jtag/jtaghome.htm

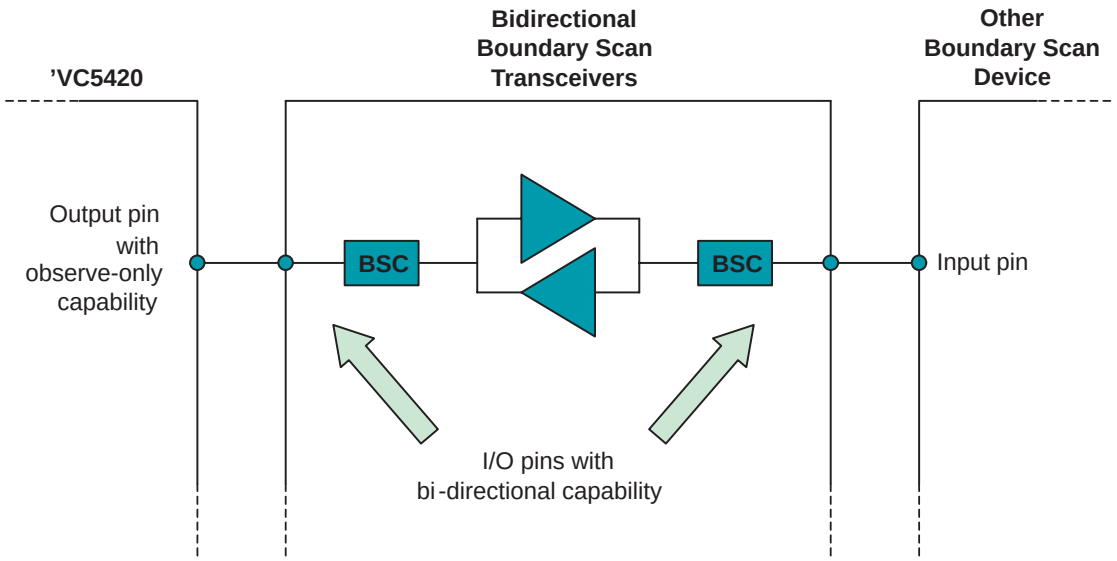


Figure 3. Increasing Test Coverage Through the Use of Boundary Scan Transceivers

If tester resources are available, test points can be placed on nets with limited test coverage to provide the ability to drive the net, as shown in Figure 4. Many ATPG tools provide analysis of a board netlist indicating which nets will only have partial or no boundary scan testability available. This analysis can be used to determine which nets will require test points.

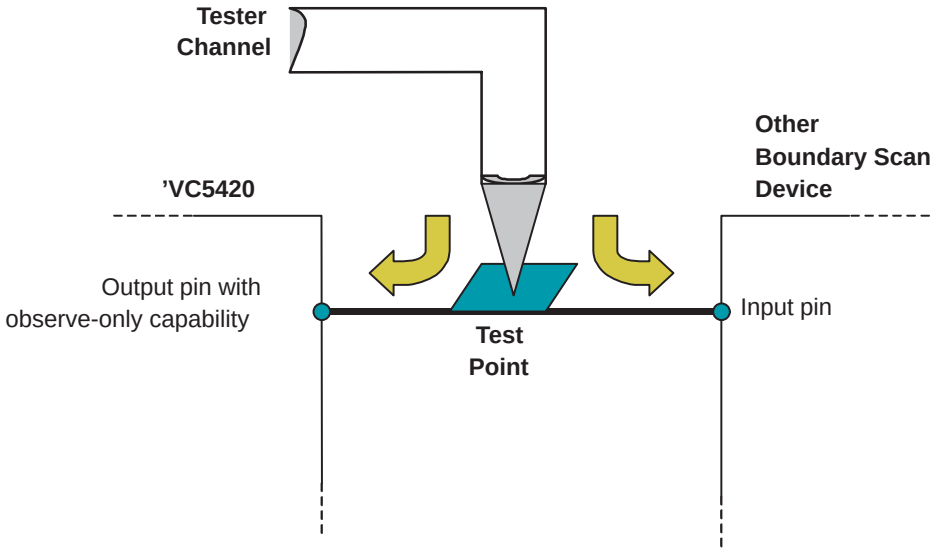


Figure 4. Increasing Test Coverage by Adding Test Points

1.4 TMS320VC5420 Hardware Requirements for Boundary Scan Test

Boundary scan test requires control of the five test access port signals (TMS, TCK, TDI, TDO and TRST) as described in IEEE standard 1149.1. Two additional signals, EMU0 and EMU1/OFF, are used by TI DSPs to provide emulation debug capability through the JTAG test access port. These signals are also used by TI for scan-based factory tests.

During boundary scan tests, EMU0 and EMU1/OFF must be held high while TRST is transitioned from low to high. This operation sets the correct internal test mode for boundary scan test to be performed. EMU0 and EMU1/OFF should be pulled high through 4.7k ohm pull-up resistors on each pin. The pull-up resistors are connected to the DVdd power supply for the ’VC5420.

Boundary scan ATPG tools should be configured to cycle TRST before beginning boundary scan tests to ensure that the device is in the proper test mode. See Figure 5.

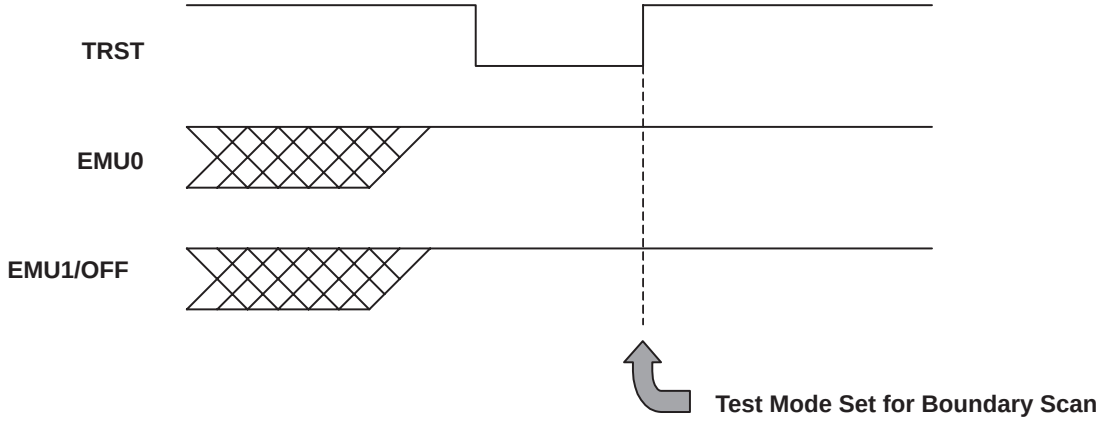


Figure 5. Initialization for Boundary Scan Test Mode using TRST, EMU0 and EMU1/OFF.

1.5 TMS320VC5420 Boundary Scan Pin Coverage

All digital pins (100 pins) on the ’VC5420 have boundary scan cells for test with the following exceptions. The device pins not testable through boundary scan are shown below in Table 2.

Table 2. Device Pins Not Testable Through Boundary Scan

Pin	Pin Function
DVdd, CVdd, Vss, AVdd, Vssa	Power supply pins
VCO, TEST	Factory test pins
TMS, TCK, TDI, TDO, TRST	JTAG test access pins
EMU0, EMU1/OFF	Emulation test pins

1.6 TMS320VC5420 Boundary Scan Description Language (BSDL) Implementation

A representation of the internal structure of the ’VC5420 with respect to boundary scan is shown in Figure 6. The ’VC5420 is composed of two internal processors called subsystems. Each subsystem has its own independent TAP controller to provide boundary scan test and emulation capability. The device signals TMS, TCK and TRST are connected to each subsystem in parallel. The device TDI is connected to subsystem A. The internal equivalent of TDO for subsystem A is connected to the internal TDI for subsystem B. The output of the chain from subsystem B is connected to the device TDO. To a boundary scan test system, this structure is equivalent to treating the subsystems as independent devices.

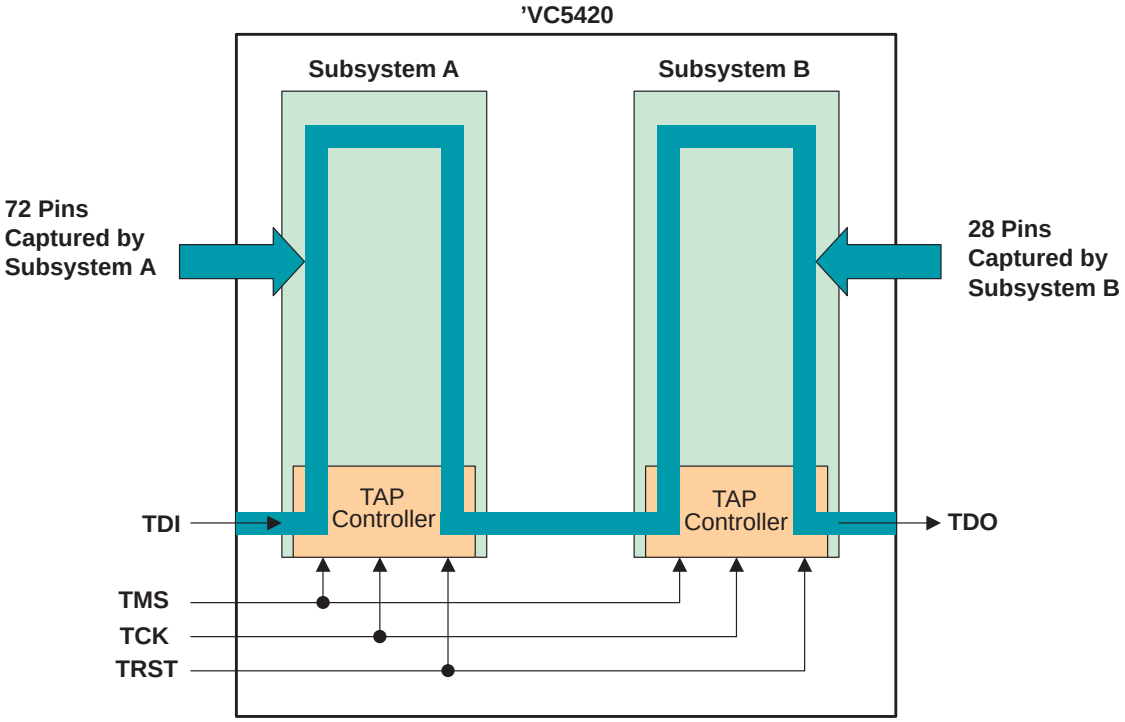


Figure 6. Boundary Scan Structure of the ’VC5420

The two subsystems have the ability to capture unique groups of pins on the device. Subsystem A captures 72 pins which include the pins associated uniquely with subsystem A and the device pins that are common to both subsystems. Subsystem B captures only the device pins associated with subsystem B. The pins captured by each subsystem are listed in Table 3.

Table 3. Pins Captured by Each ’VC5420 Subsystem During Boundary Scan Test

Subsystem	Pins			Description
A	A_BCLKR [0:2] A_BCLKX [0:2]	A_BDR [0:2] A_BDX [0:2]	A_FSR [0:2] A_FSX [0:2]	McBSP signals
	A_CLKOUT	CLKIN		Clock signals
	A_GPIO[0:3]	A_XF		General purpose I/O signals
	A_INT[0:1]	A_NMI	A_RS	Interrupt signals
	XIO	SELA/B		Mode control signals
	HCS HMODE HR/W	HDS1 HPIRS	HDS2 HRDY	HPI-16 signals
	(H)A[0:17]			Address bus
	(H)D[0:15]			Data bus
B	B_BCLKR [0:2] B_BCLKX [0:2]	B_BDR [0:2] B_BDX [0:2]	B_FSR [0:2] B_FSX [0:2]	McBSP signals
	B_CLKOUT			Clock signals
	B_GPIO[0:3]	B_XF		General purpose I/O signals
	B_INT[0:1]	B_NMI	B_RS	Interrupt signals

Although ATPG tools vary in how they describe system level structure, all tools provide a method to describe the order of the devices in the scan chain. The BSDL description of the ’VC5420 is implemented as 2 BSDL files, one for each subsystem. These two boundary scan objects must always be paired and described to the ATPG tools in the proper order. Subsystem B must be described as the subsystem closer to TDO. If the order is reversed, tests generated by the ATPG tools will be incorrect.

Since the connection between the scan chains of the two subsystems is internal to the device, some ATPG tools may issue a warning or error indicating that the TDO-TDI connection between the two subsystem objects is not present. In this case, the device can be modeled as a multichip module using the hierarchical capabilities of the ATPG tool. Many boundary scan systems have hierarchical scan chain descriptions where, for example, a plug-in module may be described as a sub-chain to the main boundary scan chain. The model for the sub-chain is generated separately, and then referenced in the description of the main boundary scan chain. The same approach can be used to model the ’VC5420 as a single object if necessary. The device can be modeled as a sub-chain composed of subsystem A and subsystem B, shown in Figure 7. Then, the ’VC5420 can be referenced in the main description of the scan chain as a single device “module”. Since the methods to describe hierarchical and modular systems are tool dependent, a single method cannot be described here. It will be necessary to contact the ATPG tool vendor regarding how this procedure is done on their tool. Given the BSDL files for each subsystem and the information in this document, a model can be generated.

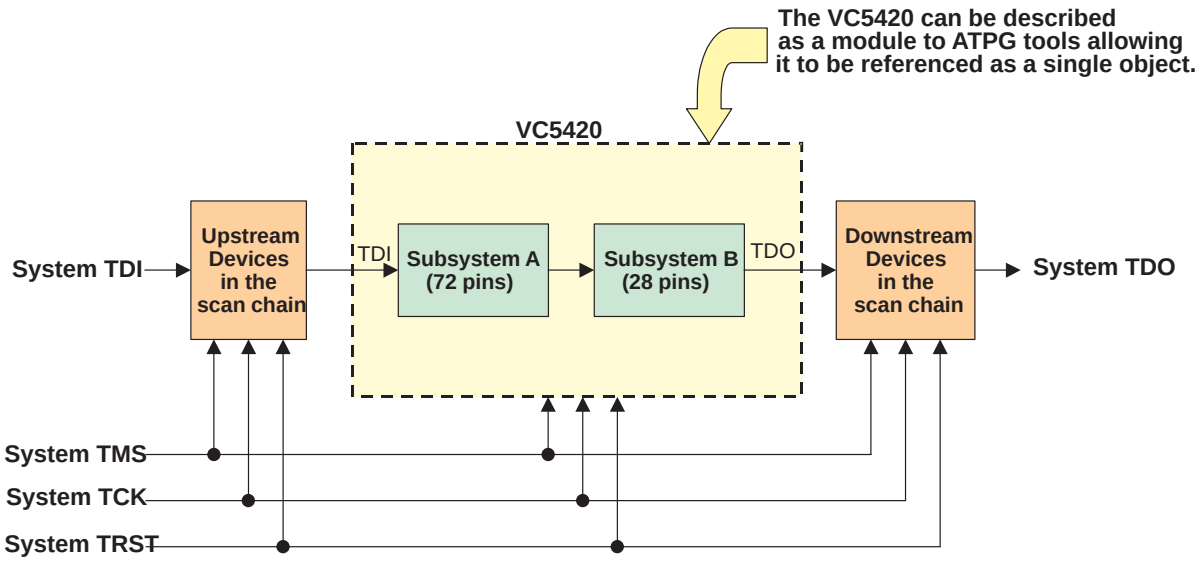


Figure 7. The ’VC5420 Subsystems Modeled as a “Module” in the Scan Chain

The BSDL files used for the ’VC5420 should be revision 3.0 or later. The BSDL file revision is listed in the information in the beginning of the file. File revisions prior to 3.0 reflect the architecture of silicon prior to silicon revision 1.5 and should not be used.

Current ’VC5420 BSDL files and information are available on the web at:

http://www.ti.com/sc/docs/tools/dsp/ftp/c54x.htm

1.7 TMS320VC5420 Boundary Scan Instruction Implementation

The ’VC5420 implements the three required instructions for boundary scan:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS

IEEE standard 1149.1 specifies that the SAMPLE/PRELOAD instruction samples inputs and preloads but does not drive outputs. During the SAMPLE/PRELOAD instruction, the device pins maintain their normal functional behavior. Since the ’VC5420 has no output (control) boundary scan cells to preload, the operation of this instruction is identical to fully compliant devices.

IEEE standard 1149.1 specifies that the EXTEST instruction samples inputs, and loads and drives outputs. During the EXTEST instruction, all device pins function as boundary scan inputs. Since the ’VC5420 has no output (control) boundary scan cells to load/drive, this instruction can be used only to sample the states of the device pins and consequently deviates from compliance with IEEE standard 1149.1.

IEEE standard 1149.1 specifies that the BYPASS instruction maps a one-bit bypass register between TDI and TDO (to minimize the chain length when a device is not being tested) and the device pins operate in their normal functional (non-test) mode. The observe-only capability on the ’VC5420 has no impact on the BYPASS instruction. During the BYPASS instruction, the device pins maintain their normal functional behavior. The operation of the BYPASS instruction is identical to fully compliant devices. Note that the ’VC5420 has one bypass bit for each subsystem (since there is a TAP controller for each subsystem) for a total of two bits between the device TDI and TDO. This behavior is accounted for (and maintains compliance with IEEE standard 1149.1) through the use of separate BSDL files for each subsystem.

None of the other boundary scan instructions specified as optional in IEEE standard 1149.1 are implemented on the ’VC5420.

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