Application Report
SPRA621 - December 1999

TMS320VC5420 to TMS320VC5421 DSP Migration

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5420 to the TMS320VC5421. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets, the TMS320C54x DSP CPU and Peripherals, Reference set Volume 1 (SPRU131), and the TMS320C54x DSP Enhanced Peripherals, Reference set Volume 5 (SPRU302).

Migration issues from the ’VC5420 to ’VC5421 are indicated with the following symbols:

[S] means software modification is required

[H] means hardware modification is required

[D] means the ’VC5420 and ’VC5421 are different (usually due to added features on the ’VC5421), but no modification is necessary for migration (that is, the devices are different but compatible).

These symbols are included at the beginning of each section.

Unless otherwise noted, the information contained in this document should be considered ADVANCE INFORMATION on new products in the sampling or pre-production phase of development. Information and specifications in this document are subject to change without notice.

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1 Introduction

One goal of the ’VC5421 program was to make it as easy as possible to migrate existing ’VC5420 designs to the new architecture. However, within a few areas compromises were made. Most of the differences should require software-only changes to the user’s system. This document is only intended to highlight those differences, not to provide a detailed technical reference. For more information, please see the ’VC5421 device datasheet (SPRS098), the TMS320C54x Enhanced Peripherals, Reference Set Volume 5 (SPRU302), the TMS320VC5421 Bootloader Specification, or the TMS320C5000 DSP Family Functional Overview (SPRS039).

2 Memory Structure [S]

The memory structure of the ’VC5421 is the most significant change that was made from the ’VC5420. The ’VC5421 contains a total of 256K words of RAM. This is an addition of 56K words over the ’VC5420. Each of the two subsystems on the device contains 32K words of local DARAM (Program/Data) and 32K words of local SARAM (Data only). The remaining 128K words of DARAM (Program only) are shared between the two subsystems. The shared memory scheme was implemented to more efficiently use memory in systems that are running the same code on both cores. In addition, the ’VC5421 includes 2K words of local ROM in each subsystem for use in bootloading the device. For reference, please see the block diagrams of both devices located in Appendix A.

3 Memory Maps [S]

3.1 CPU Map

The CPU memory maps of the ’VC5420 and the ’VC5421 are very similar in terms of the address location of the memories (see memory maps in Appendix B). The ’VC5421 adds its additional memory at addresses that were designated as external on the ’VC5420. Although all of the shared memory is shown on the ’VC5421’s CPU memory map, the CPU only has read access to those blocks. The HPI or DMA must be used to perform all writes to the shared memory. The CPU was not given write access to the shared memory to protect the user from inadvertently overwriting program code

3.2 DMA and HPI Maps

There was a significant change made to the organization of both the DMA and HPI memory maps with respect to the ’VC5420. The address range of the DMA on the ’VC5421 has been extended to include access to all external memory. This feature was not available on the ’VC5420. (Although only the DMA is mentioned, all of the following comments apply to both the DMA and the HPI). In addition, each DMA on the ’VC5421 has access to all of the on-chip memory of the device. For example, Core A’s DMA is able to access all of Core B’s local memory. In order to make this feature possible, the memory maps are organized differently from those of the ’VC5420. Also, certain blocks of memory appear at different addresses depending on the type of access: CPU, DMA, or HPI. For example, the ’VC5421’s CPU map shows a 32K word block called “Shared 0” at program address 00 8000, while the DMA map shows the same block at program address 01 0000.

4 McBSPs [D]

4.1 Sample Rate Generator

The McBSPs of the ’VC5421 have been enhanced to provide more flexibility in the choice of the sample rate generator input clock source. On previous C5000 devices, the McBSP Sample Rate Generator (SRG) input clock could be driven from one of two possible choices: the internal CPU clock, or the external CLKS pin. However, most C5000 devices have only the internal CPU clock as a possible source because the CLKS pin is not present on most device packages.

To accommodate applications that require an external reference clock for SRG, the ’VC5421 McBSPs allow the receive clock (BCLKR) or the transmit clock (BCLKX) to be configured as the input clock to the SRG. This enhancement is enabled through two register bits: Pin Control Register (PCR) bit 7 – enhanced sample clock mode (SCLKME), and SRG Register 2 (SRGR2) bit 13 – McBSP SRG Clock Mode (CLKSM). SCLKME is an addition to the PCR contained in ’VC5420 and other previous C5000 devices. The new bit layout of the PCR register is shown in the figure below.

15 14	13	12	11	10	9	8
Reserved	XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM

7	6	5	4	3	2	1	0
SCLKME	CLKS STAT	DX STAT	DR STAT	FSXP	FSRP	CLKXP	CLKRP

Figure 1. ’VC5421 Pin Control Register (PCR)

The selection of the SRG clock input source is made by the combination of the CLKSM and SCLKME bit values as shown in the table below.

Table 1. ’VC5421 Sample Rate Input Clock Selection

SCLKME	CLKSM	SRG Clock Source
0	0	CLKS pin (not available as a pin on ’VC5421)
0	1	CPU clock
1	0	BCLKR pin
1	1	BCLKX pin

When either of the bi-directional pins BCLKX or BCLKR is configured as the clock input, its output buffer is automatically disabled.

4.2 128 Channel Enable

Another enhancement to the ’VC5421’s McBSPs is the addition of the 128 channel selection capability. The ’VC5421 McBSPs now have two working modes that are selected by setting the RMCME and XMCME bits in the Multichannel Control Registers (MCR1x and MCR2x). A description of these modes follows:

- In the first mode, when RMCME = 0 and XMCME = 0, there are two partitions (A and B), with each containing 16 channels. This is compatible with the mode used in the ’VC5420, where only 32-channel selection is available.
- In the second mode, with RMCME = 1 and XMCME=1, the McBSPs have 128 channel selection capability. Twelve new sub-addressed registers (RCERCx – RCERHx and XCERCx – XCERHx: x=0,1,2) are used to enable the 128 channel selection. The subaddresses of the new registers are given in the ’VC5421 datasheet (SPRS098). The new registers are functionally equivalent to the RCERAx-RCERBx and XCERAx-XCERBx registers in the ’VC5420. These are used to enable/disable the transmit and receive of additional channel partitions (C, D, E, F, G, and H) in the 128 channel stream. For example, XCERH1 is the transmit channel enable for channel partition H (channels 112 to 127) of McBSP1 for each DSP subsystem. See the following figures and tables for bit layout of the control, receive, and transmit registers.

15 – 10	9	8 – 7	6 – 5	4 – 2	1 – 0
Reserved	XMCME	XPBBLK	XPABLK	XCBLK	XMCM

NOTE: x = MCBSP 0, 1, or 2

Figure 2. Multichannel Control Register 2x (MCR2x) Bit Layout

15 – 10	9	8 – 7	6 – 5	4 – 2	1 – 0
Reserved	RMCME	RPBBLK	RPABLK	RCBLK	RMCM

NOTE: x = MCBSP 0, 1, or 2

Figure 3. Multichannel Control Register 1x (MCR1x) Bit Layout

15	14	13	12	11	10	9	8
RCERyz15	RCERyz14	RCERyz13	RCERyz12	RCERyz11	RCERyz10	RCERyz9	RCERyz8
7	6	5	4	3	2	1	0
RCERyz7	RCERyz6	RCERyz5	RCERyz4	RCERyz3	RCERyz2	RCERyz1	RCERyz0

NOTE: y = Partition A, B, C, D, E, F, G, or H; z = McBSP 0,1, or 2

Figure 4. Receive Channel Enable Registers Bit Layout (RCERyz)

Table 2. Receive Channel Enable Registers for Partitions A to H

Bit	Name	Function
15–0	RCERyz(15:0)	Receive Channel Enable Register: RCERyz n=0 Disables reception of nth channel in partition y RCERyz n=1 Enables reception of nth channel in partition y

NOTE: y = Partition A, B, C, D, E, F, G, or H; z = McBSP 0,1, or 2; n = bit 15–0

15	14	13	12	11	10	9	8
XCERyz15	XCERyz14	XCERyz13	XCERyz12	XCERyz11	XCERyz10	XCERyz9	XCERyz8
7	6	5	4	3	2	1	0
XCERyz7	XCERyz6	XCERyz5	XCERyz4	XCERyz3	XCERyz2	XCERyz1	XCERyz0

NOTE: y = Partition A, B, C, D, E, F, G, or H; z = McBSP 0, 1, or 2

Figure 5. Transmit Channel Enable Registers Bit Layout (XCERyz)

Table 3. Transmit Channel Enable Registers for Partitions A to H

Bit	Name	Function
15–0	XCERyz(15:0)	Transmit Channel Enable Register: XCERyz n=0 Disables transmit of nth channel in partition y XCERyz n=1 Enables transmit of nth channel in partition y

NOTE: y = Partition A, B, C, D, E, F, G, or H; z = McBSP 0,1, or 2; n = bit 15–0

5 Bootloading [D]

The ’VC5420 does not contain an on-chip bootloader program. Therefore, a host processor must load the device’s memory through the HPI. In addition, for stand-alone operation, the end user can write a bootloader program to perform this function. The end user’s bootloader program can be placed along with the code to be booted into a non-volatile external memory. Furthermore, similar to the ’VC5420, the ’VC5421 supports bootloading through the HPI. In addition, the ’VC5421 has the capability to load its internal memory through the use of the bootloader program contained in on-chip ROM.

The ’VC5421 bootloader is a program contained in the on-chip ROM that can be used to initialize the system memory after reset. Several options or boot modes are available to support various methods of initialization. The following boot modes are included in the ’VC5421 boot loader:

- Parallel-16 Boot Mode: loads code via 16-bit wide asynchronous memory device using the external memory interface.
- Parallel-8 Boot Mode: loads code via 8-bit wide asynchronous memory device using the external memory interface.
- Serial EEPROM Boot Mode: loads code via an external master device such as 8-bit wide serial EEPROMs using McBSP 2.

The bootloader allows multiple memory sections to be loaded into different destination addresses within the system RAM. These sections can be either program or data. However, the bootloader cannot directly boot into data space. If specific sections must be placed in data memory space, these particular sections can initially be stored in program space, and then copied over by the main program at run time. Another way of initializing sections in data space is by using the on-chip DARAM, which can be mapped into both program space and data space. Otherwise, sections to be stored in data memory must follow the sections to be stored in program memory and these sections will be booted last.

After reset, if the on-chip ROM is enabled (XIO=1 and ROMEN/GPIO0=1), the ’VC5421 automatically begins execution of the boot loader. After the initialization is performed, the boot loader loads the system RAM according to the boot mode selected and then causes the ’VC5421 to begin execution of the loaded code. At this point, the boot load process is complete, and the ’VC5421 performs the intended system function.

For additional information about the bootloader and boot modes, please refer to the TMS320VC5421 Bootloader Specification and the device datasheets.

6 HOLD/HOLDA Pins [H]

HOLD and HOLDA pins have been added to the ’VC5421. HOLDA takes the place of the ’VC5420’s VCO pin, and HOLD was placed in a previously unused pin on the ’VC5420. These pins are used to request access to the external buses on the device. ’VC5420 designs moving to the ’VC5421 should be evaluated to determine if the VCO pin was being used.

Descriptions of the HOLD/HOLDA pins are shown below:

HOLD – Input – HOLD is asserted to request control of the address, data, and control lines. When acknowledged, these lines go into the high-impedance state.

HOLDA – Output – Hold acknowledge. HOLDA indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing them to be available to the external circuitry.

7 SELA/B/PPA18 Pin [H]

On the ’VC5420, this pin was always an input. On the ’VC5421, this pin is also an input when in HPI mode (XIO=0). However, this pin becomes address bit output PPA18 on the ’VC5421 when in XIO mode (XIO=1). Existing designs may need to be modified to accommodate the bi-directionality of this pin on ’VC5421.

8 Chip Subsystem ID Register [D]

The Chip subsystem ID Register (CSIDR) is a new feature contained only on the ’VC5421. CSIDR is a read-only memory mapped register located at address 0x003E in each DSP subsystem. This register contains three elements for electrically readable device identification. The ChipID bits identify the type of ’54xx device (0x21 for ’VC5421). The ChipRev bits contain the revision number of the device. The SubSysID contains a unique subsystem identifier (A=0h, B=1h).

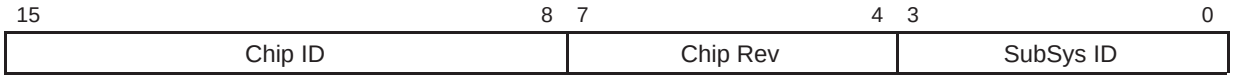

Figure 6. Chip Subsystem ID Register Bit Layout

9 DMA/XIO Arbitration [S]

The DMA on the ’VC5420 does not support any external accesses. Conversely, the ’VC5421 DMA supports external accesses to extended program, extended data, and extended I/O memory. In addition, the ’VC5421 DMA has extended data memory overlay pages that are only visible to the DMA controller. These pages are not directly accessible by the CPU. It supports single 16-bit word transfers when writing or reading from external memory. A maximum of two DMA channels (one for reads, one for writes) can be used for external memory accesses per subsystem. These accesses require 9 cycles (minimum) for external writes and 13 cycles (minimum) for external reads.

The two subsystems share the external bus. The control of the bus is arbitrated between the two CPUs and the two DMAs. While one (DMA or CPU) is in control of the external bus, the other three components will be held off (via wait-states) until the current external transfer is complete. The DMA takes precedence over XIO requests. The HOLD/HOLDA feature of the ’VC5421 affects external CPU transfers, as well as external DMA transfers. When an external processor asserts the HOLD pin to gain control of the memory interface, the HOLDA signal is not asserted until all pending DMA transfers are completed. To prevent a DMA from blocking out the CPUs or HOLD/HOLDA feature from accessing the external bus, burst transfers are not supported by the DMAs. Subsequently, CPU and DMA arbitration is performed for each external bus cycle, regardless of the bus activity. With the completion of each block, the highest priority owner (i.e. DMA) of the external bus will be swapped with the next highest priority requestor (i.e. XIO or other DMA).

For arbitration at the DSP subsystem level, the DMA requests (DMA_REQ_A or DMA_REQ_B) from either DMA will be sent to both CPUs as shown in the block diagram in Appendix A. Regardless of which CPU controls the external pin interface (XIO), both CPUs must send a grant (GRANT_A, GRANT_B) for control of the bus to be released to the DMAs.

Arbitration between CPUs is done using a request/grant scheme. Prior to accessing XIO of one of the CPUs, software is responsible for asserting a request for access to the device pins and polls grant status until the pins are granted to the requestor. If both CPUs request the bus simultaneously, subsystem A is granted priority. For details on memory mapped register bits pertaining to CPU XIO arbitration, see the General Purpose I/O Control Register bits 6:4 (CORE SEL, XIO GRANT, and XIO REQ) in the ’VC5421 datasheet (SPRS098).

At reset, the default is that subsystem A has access to the device pins. Accesses without a grant will be allowed, but do not show up on the device pins.

Appendix A Block Diagrams

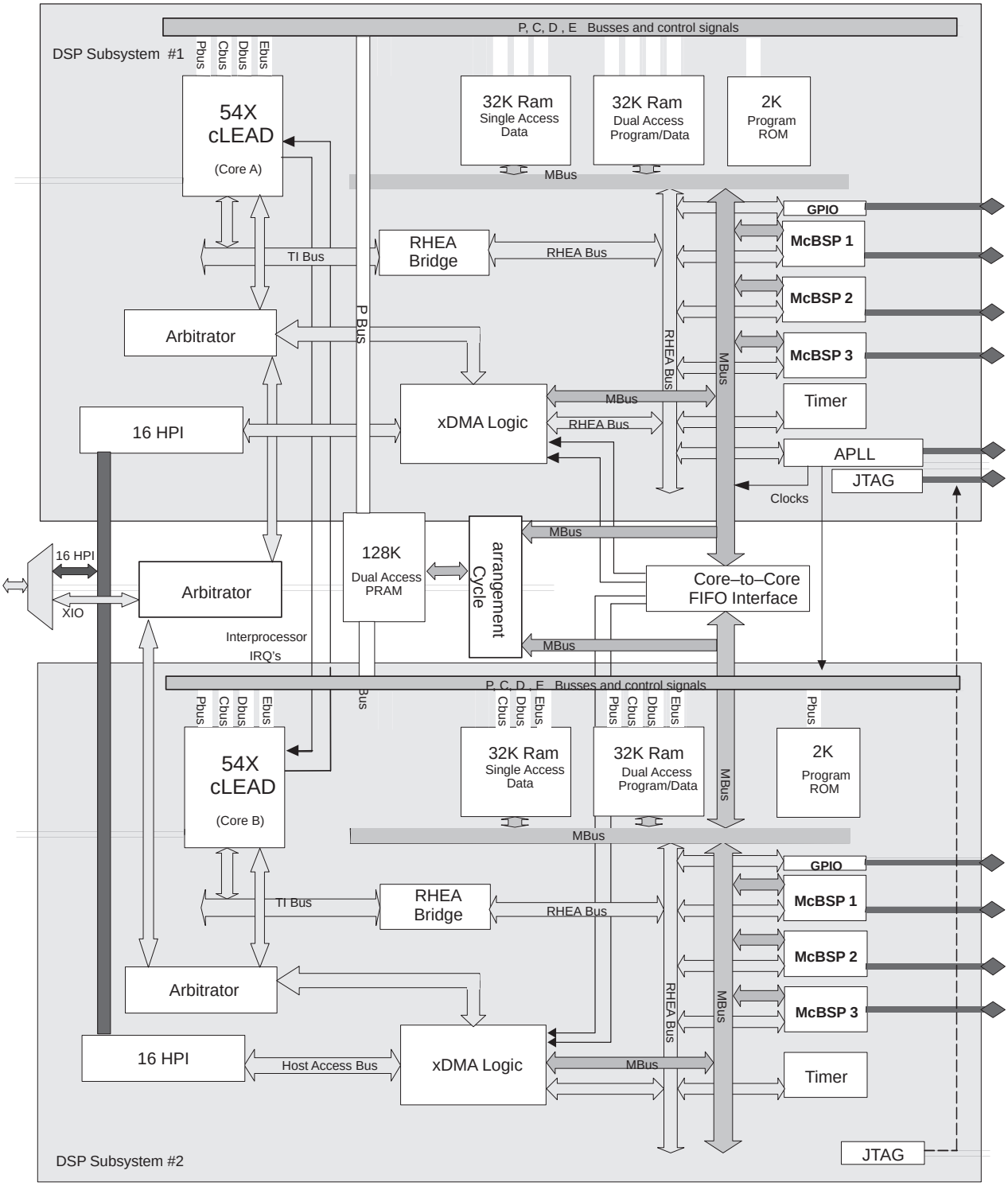

Figure A–1. 'VC5421 Block Diagram

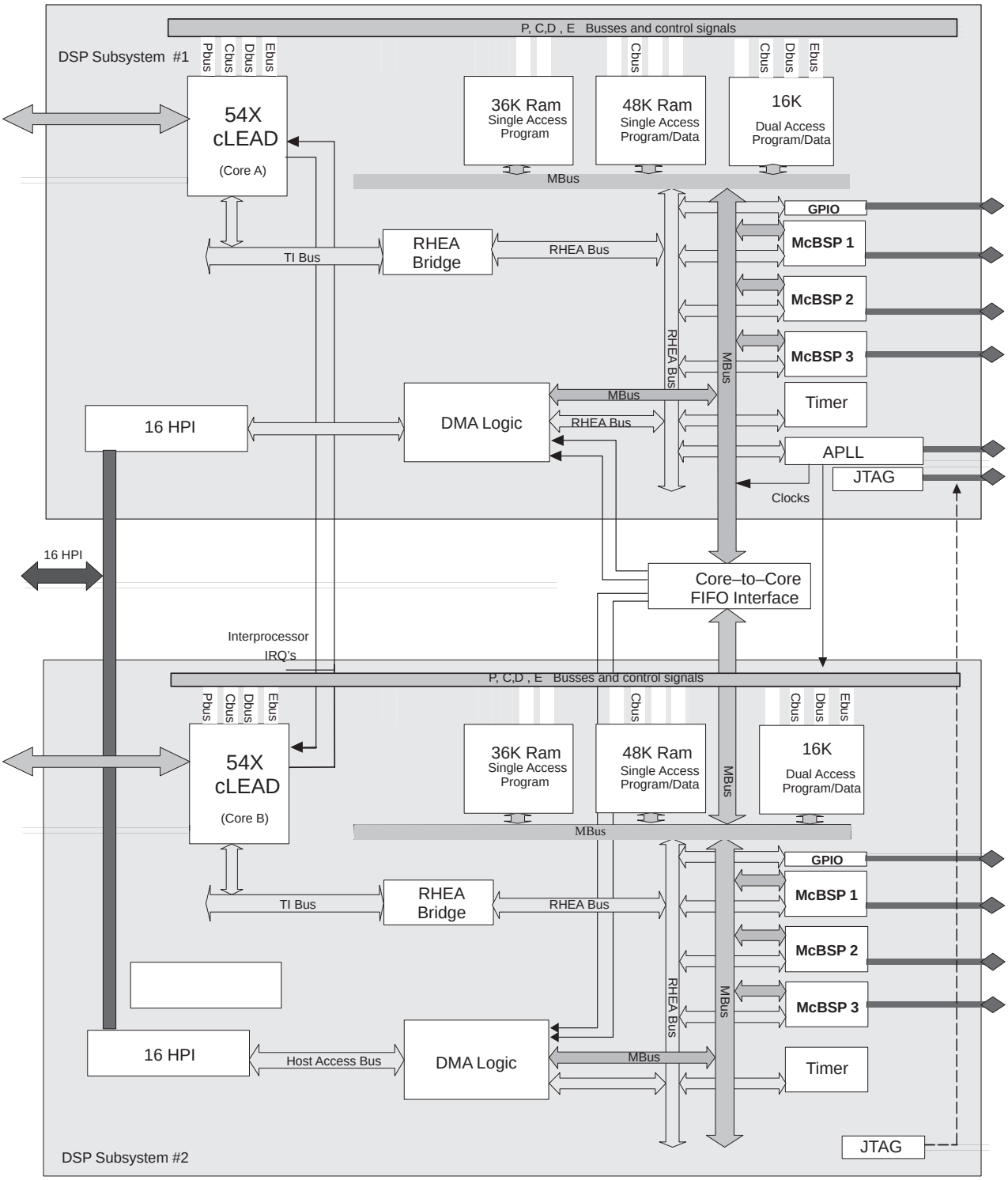

Figure A–2. ’VC5420 Block Diagram

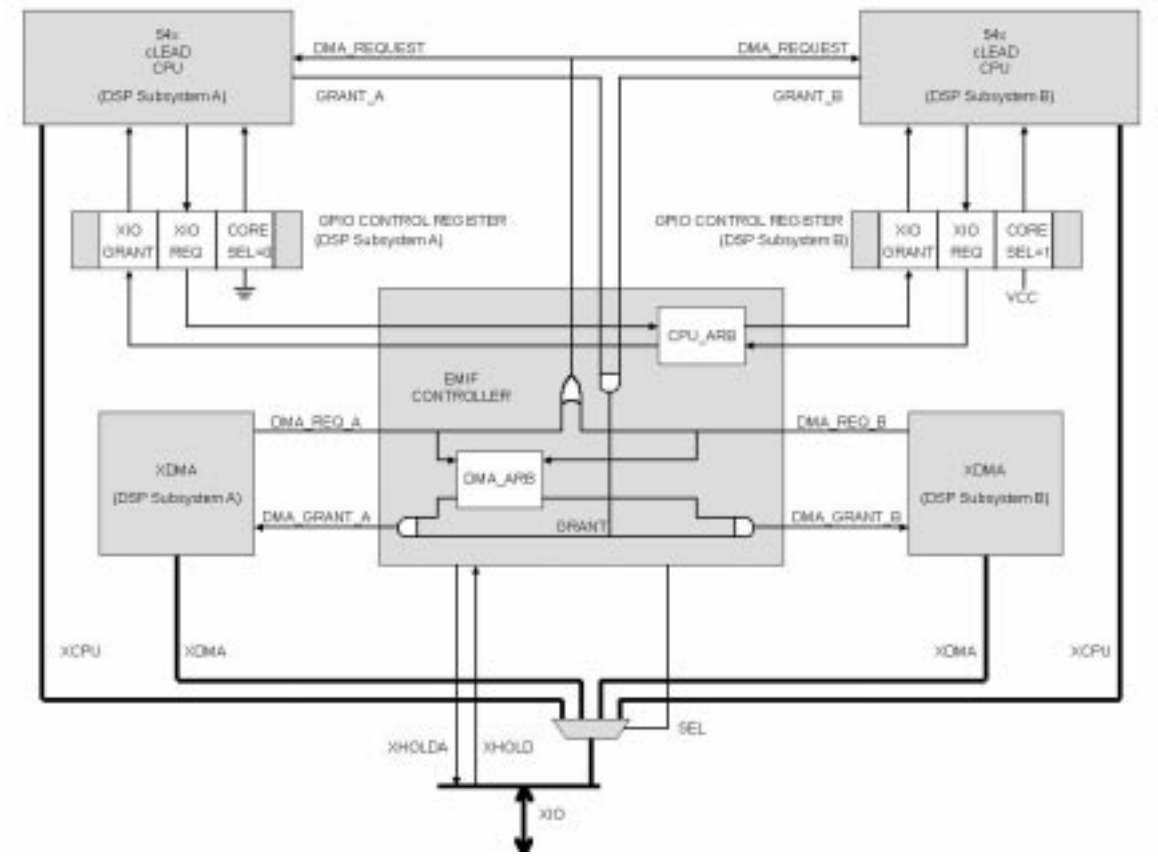

Figure A–3. ’VC5421 DMA/XIO Arbitration

Appendix B Memory Maps

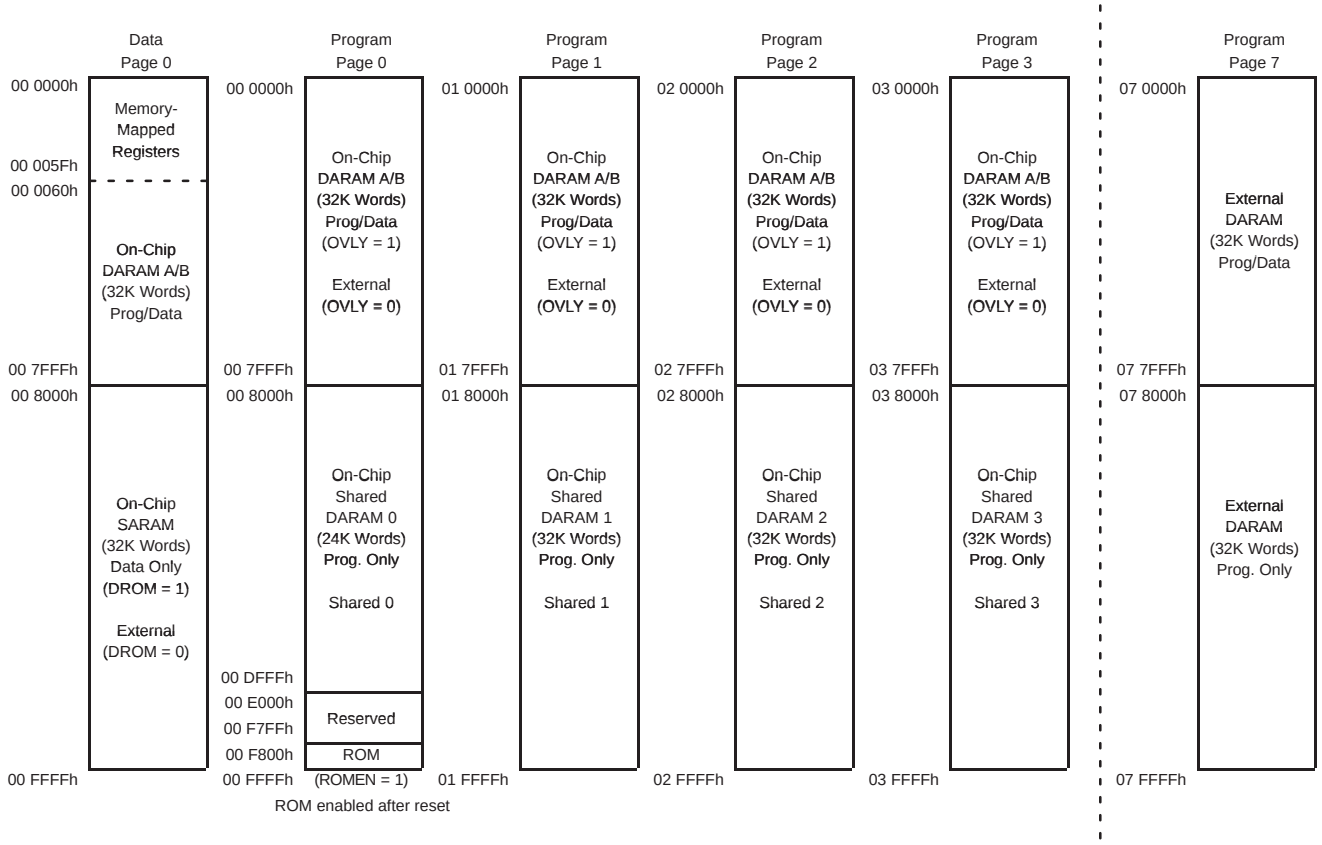

Figure B–1. ’VC5421 CPU Memory Map

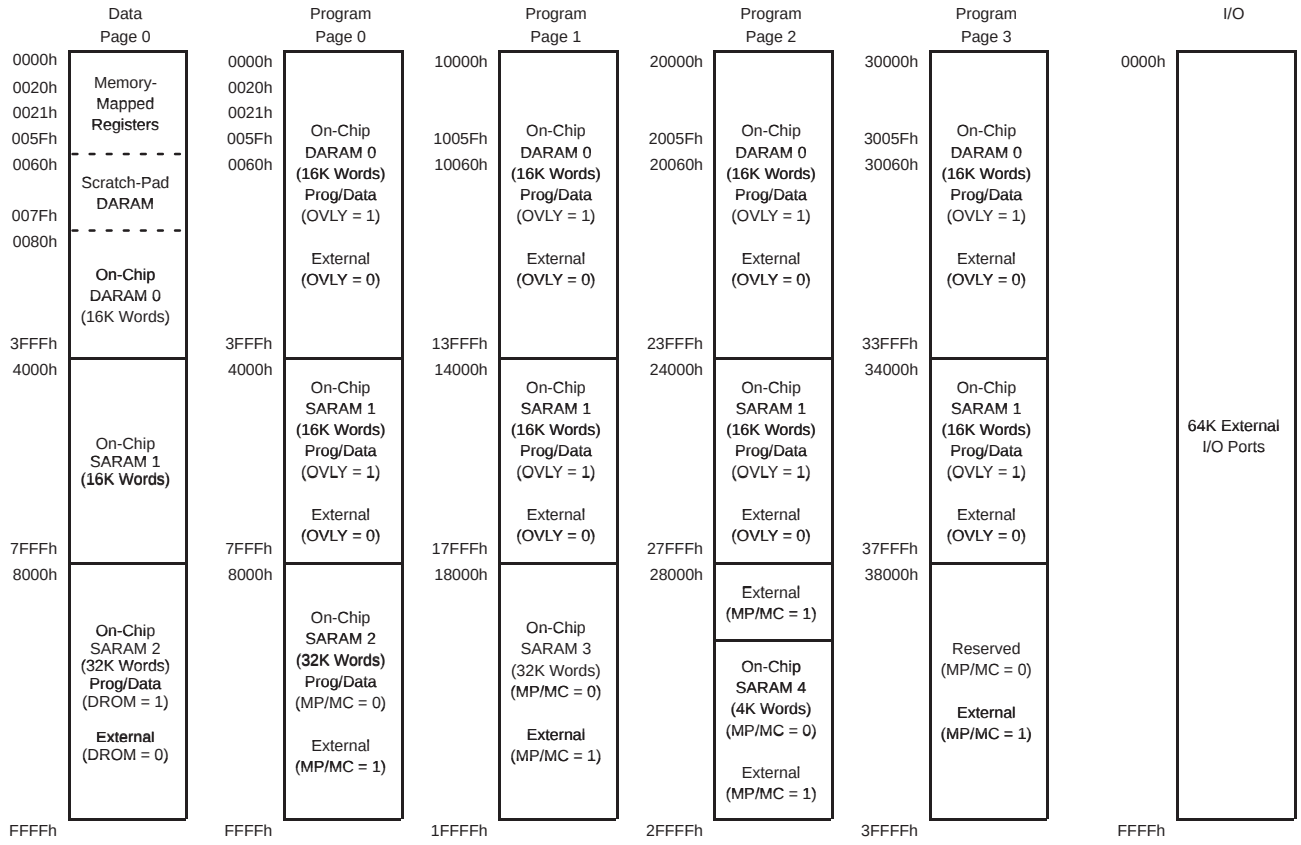

Figure B–2. ’VC5420 CPU Memory Map

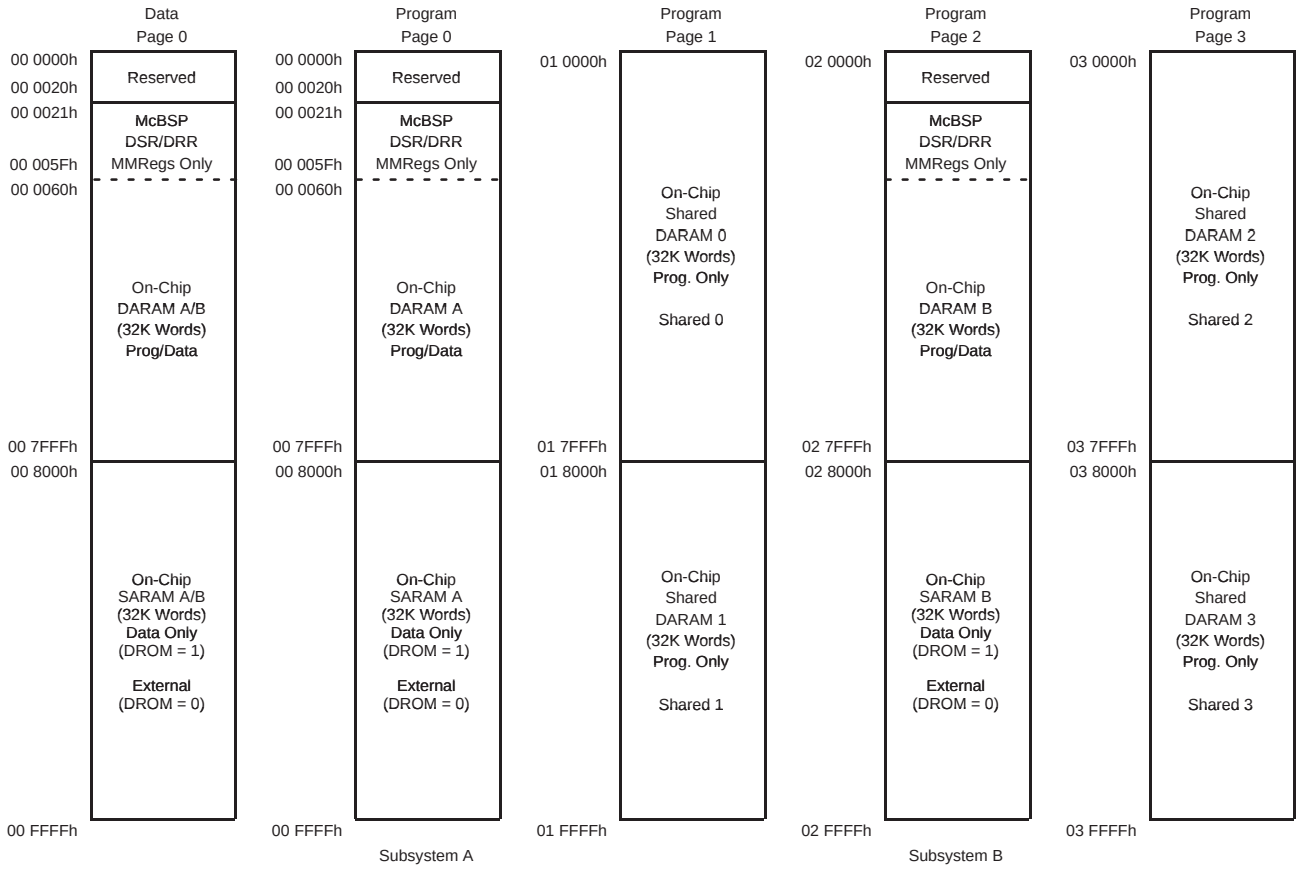

Figure B–3. ’VC5421 DMA Internal Memory Map

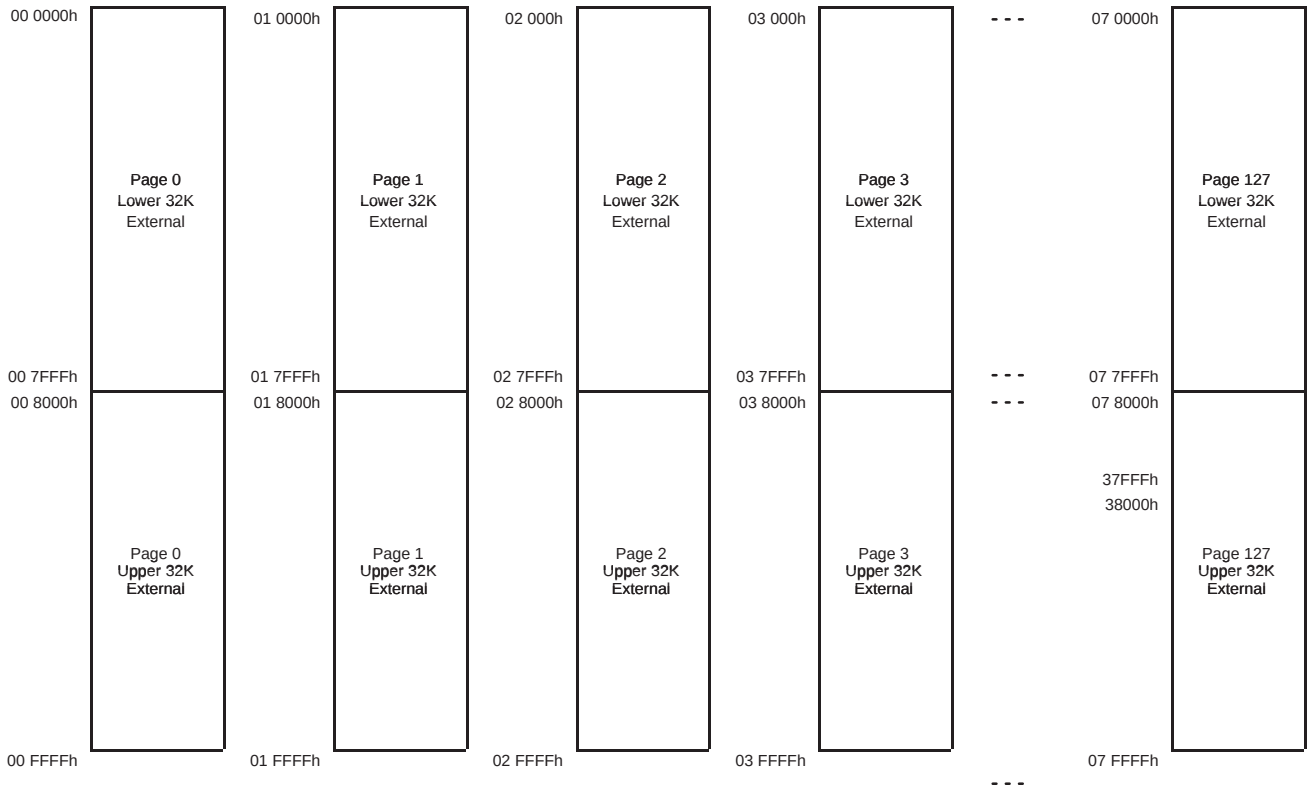

Figure B–4. ’VC5421 DMA External Data Memory Map

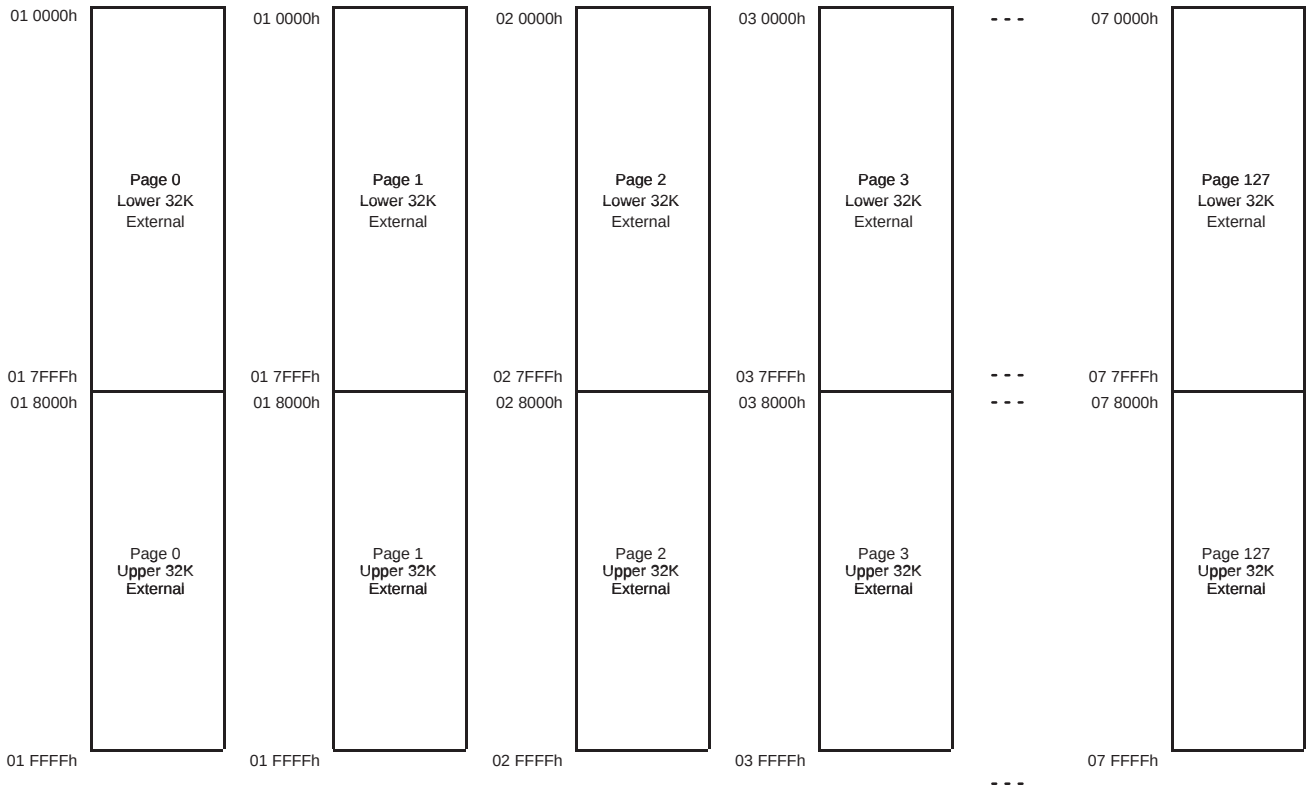

Figure B–5. ’VC5421 DMA External Program Memory Map

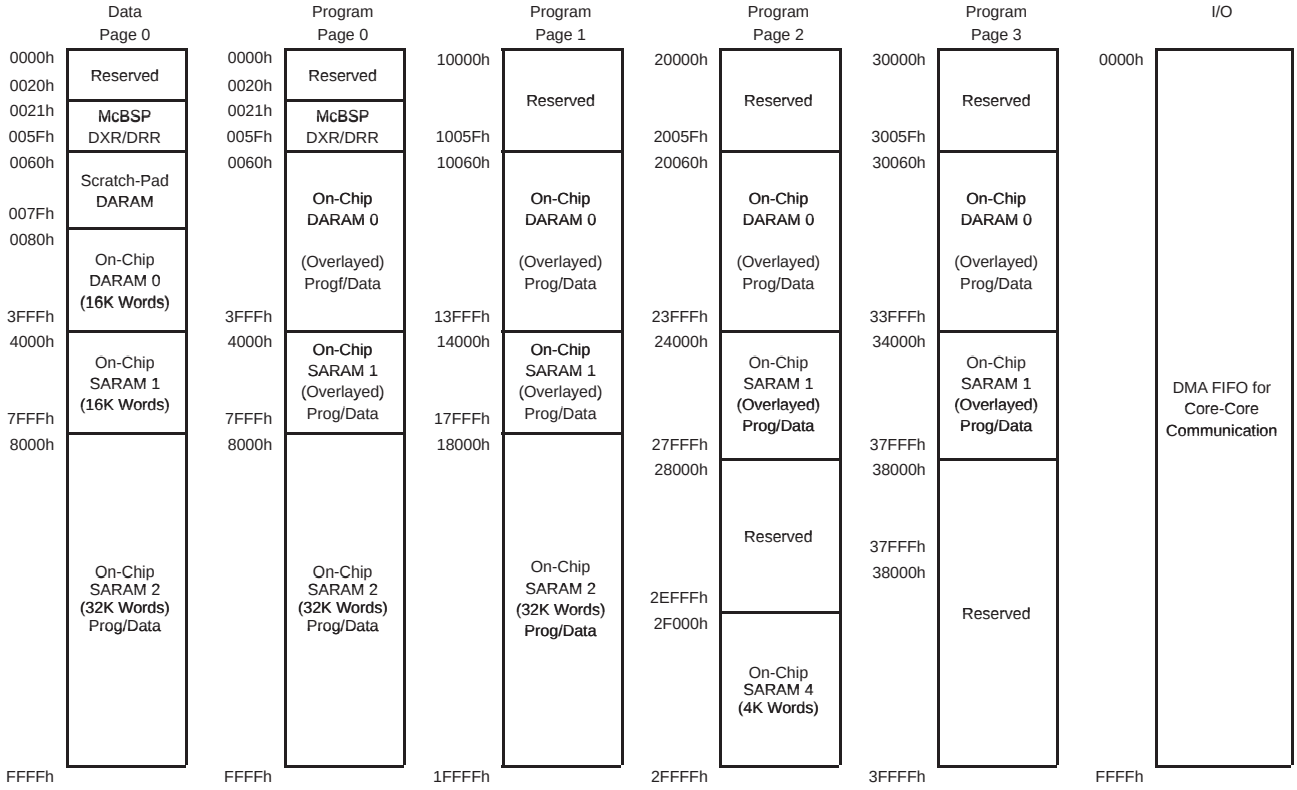

Figure B–6. ’VC5420 DMA Memory Map

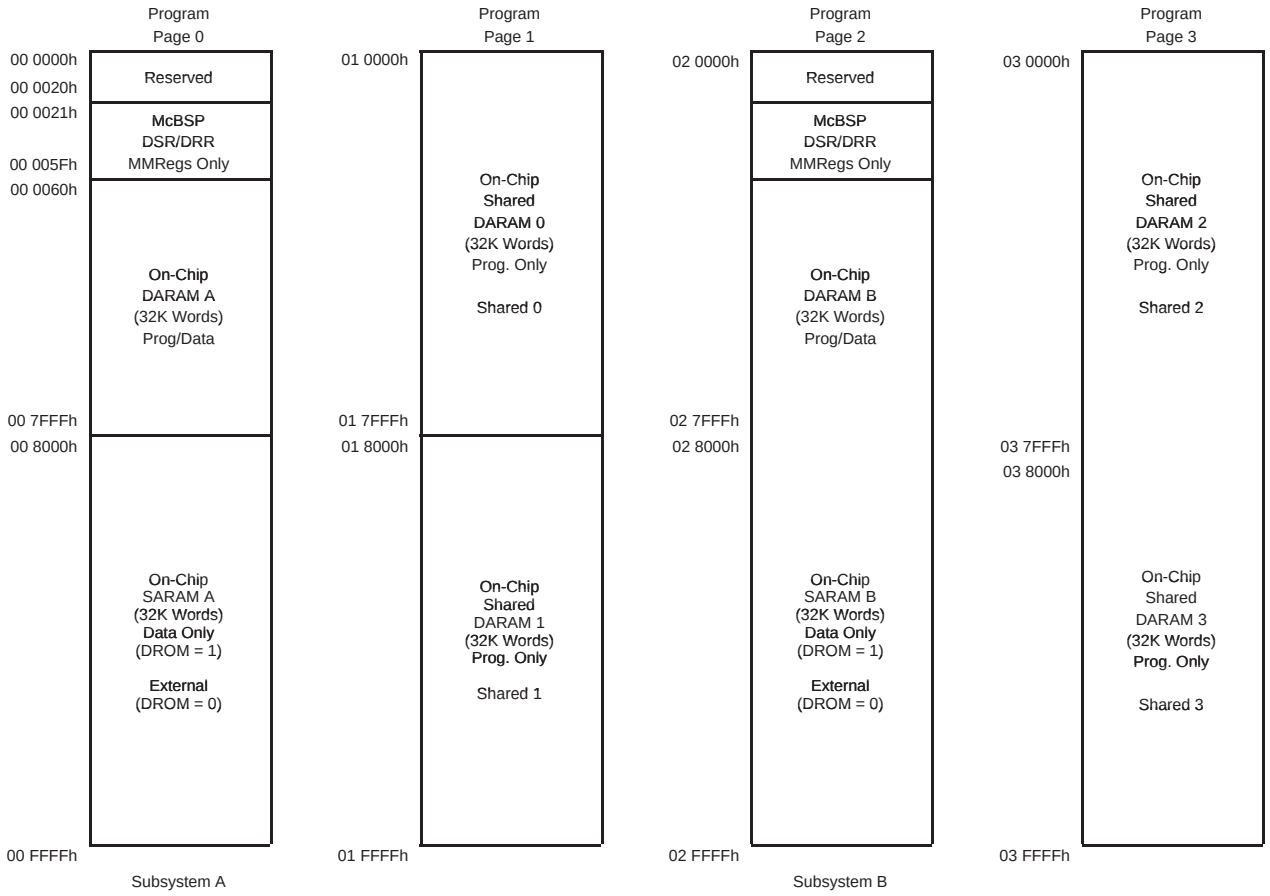

Figure B–7. ’VC5421 HPI Memory Map

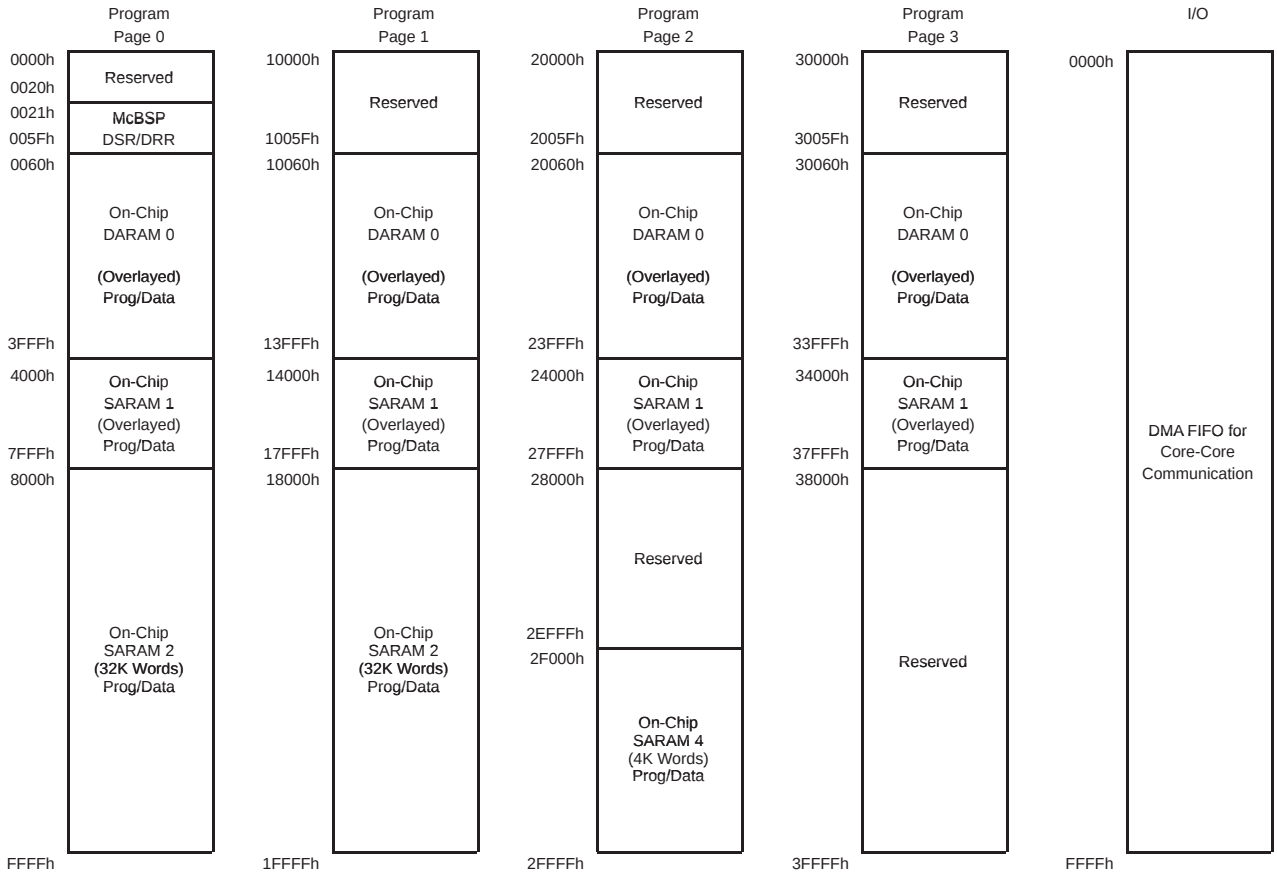

Figure B–8. ’VC5420 HPI Memory Map

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