Application Report
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TMS320 Cross-Platform Daughtercard Specification Revision 1.0

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ABSTRACT

A standard has been established for daughtercards made to function with TMS320C6000™ and TMS320C5000™ systems. The daughtercard specification is based on the interfaces provided with several existing DSP motherboards: the TMS320C6201 EVM, TMS320C6201 McEVM, TMS320C6701 EVM, TMS320C6211 DSK, TMS320C6711 DSK, TMS320C5402 DSK, and TMS320C6202 EVM. The document is divided into two primary sections: existing interfaces and future interfaces. The focus of the first section is to clearly document what is present on the motherboards that exist today as well as how to design a daughtercard that is compatible with all or some of these motherboards. The second section sets guidelines for how to move forward with designing new DSP motherboards aiming to provide a compatible interface. This specification is necessary to allow daughtercards to be designed to function with as many systems as possible. This includes systems based on different DSPs as well as systems from different vendors. The layout of a daughtercard is specified such that a card may reside within a PC chassis when attached to a PCI motherboard, though the interface is not restricted to PCI platforms. Signals are brought to the daughtercard through two 80-pin headers, with one header primarily for peripheral signals and the other primarily for the external memory interface. The daughtercard interface on the DSP motherboard has several set requirements concerning signal drive, timing delay, and voltage tolerance. Daughtercards designed with knowledge of the possible different interfaces available can be guaranteed to work on any C6000™ or C5000™ system designed to this specification. However, it is important for the engineer building the daughtercard to design logic, perform timing analysis, and develop software drivers considering the differences between the DSP interfaces and development boards (Evaluation Modules (EVMs) and DSP Starter Kits (DSKs)).

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1 Introduction

The basis for the common TMS320 daughtercard interface was the interface implemented on the Texas Instruments TMS320C6201 EVM. This EVM provided daughtercard connectors with signals for the asynchronous memory interface of the EMIF and most on-chip peripheral signals, allowing developers to design interfaces without designing an actual DSP board. This interface provides a cost-effective way to prototype a system.

Since this time, several DSP products have been created with similar interfaces. As other C6000 development platforms are being brought to market, along with similar platforms for the C5000 DSPs, commonalties in the daughtercard connectors allow daughtercards designed for one motherboard to be used on the others.

This application report documents details on how to design a daughtercard to work with all or some existing DSP development boards, as well as how to design DSP boards with compatible interfaces.

The TMS320 daughtercard standard applies to all of the C6000 and C5000 devices. The daughtercard interface allows communication to asynchronous memory or I/O peripherals, serial port interfaces, timers, multiple interrupts, and general-purpose I/O. This specification describes the several existing interfaces that provide slightly different capabilities, as well as details on how to design a daughtercard to connect to all of them. A recommended signal placement is also presented for future development boards, along with details on signal characteristics and power requirements.

2 Existing Daughtercard Interfaces

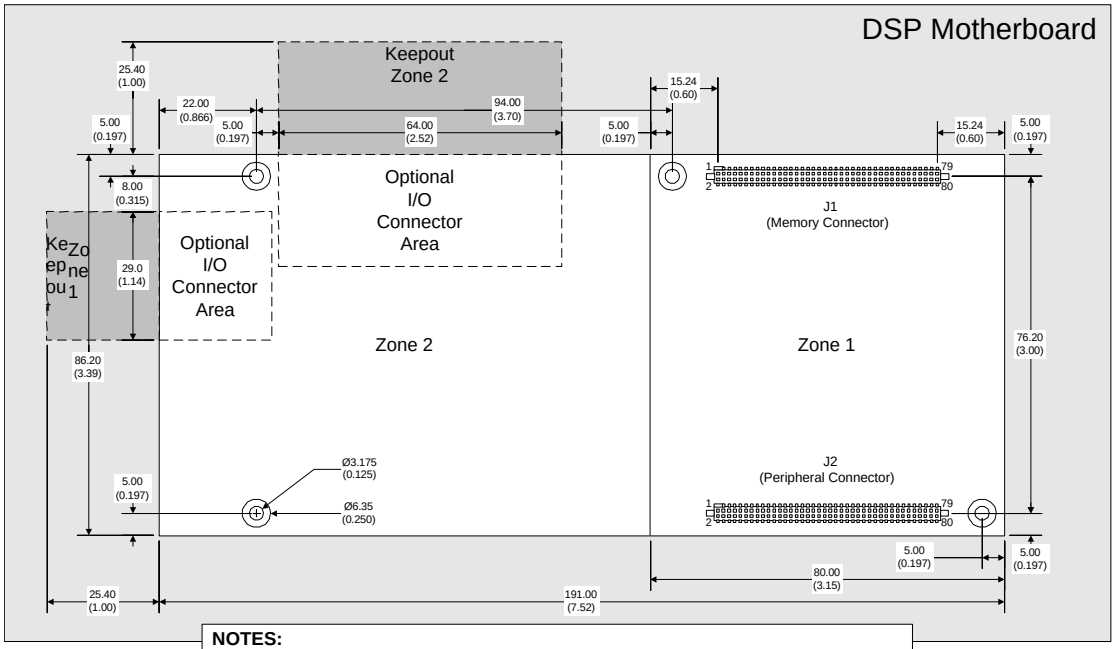
The daughtercard interfaces on all existing DSP motherboards consist of two 80-pin headers. One header contains the memory interface signals, while the other contains peripheral signals. The dimensions of the daughtercard layout area are designed to facilitate being incorporated on a PCI card within a PC chassis. The interface is not intended to be restricted to such platforms, however. Any DSP board can be equipped with a compliant daughtercard interface provided that the signal pinout and physical requirements are met.

2.1 Physical Layout

The layout of the daughtercard interface on a DSP motherboard is shown in Figure 1. Note that the layout shows the top of the DSP board and *not* the daughtercard[1]. The diagram shows the physical dimensions of the daughtercard area and the placement of the daughtercard connectors. The daughtercard interface on the DSP motherboard consists of two 80-pin connectors from Samtec. The part number for the connectors is SFM-140-L2-S-D-LC. Details on the required mating connectors on the daughtercard are provided in the daughtercard section. The DSP motherboards all support daughtercards that have dimensions up to 191 x 86.2mm (7.52 x 3.39in). This in no way affects the size requirement of the motherboard itself. It is possible that the motherboard only be large enough to accommodate the daughtercard connectors, so long as the mounted components meet the height restrictions.

The diagram shows two keepout zones on the motherboard, which are intended to allow access to I/O connectors on the daughtercard. The keepout zones are not to be physically occupied by any daughtercard component. For existing motherboards, Keepout Zone 1 on the short edge (left edge on the diagram) is only available on the C6201 EVM, C6201 McEVM, and C6701 EVM. The Keepout Zone 2 on the long edge is available on all existing C6000 motherboards. The restriction placed on the motherboard within these keepout zones is that the component height within the keepout zone is within the maximum component height for Zone 1, defined in the mating section of this document.

[1] See Figure 2 for a layout drawing of a daughtercard.



NOTES:

1. All dimensions are shown in millimeters. Inch dimensions are shown in parentheses.
2. Drawing shows component side of DSP board.
3. Full-size daughtercard area is 191 x 86.2 mm (7.52 x 3.39 in).
4. Daughtercard interface connectors are Samtec SFM-140-L2-S-D-LC.

Figure 1. Daughtercard Interface Layout on DSP Motherboard

2.2 Existing Interfaces

Several DSP motherboards are currently in production, each with common (but not identical) interfaces. Most of the differences between the interfaces stem from the fact that different DSPs have different signals available. It is possible, however, to design a variety of useful daughtercards to work with some or all of these development boards, even across DSP platforms.

TMS320C6201 EVM, C6201 McEVM, C6701 EVM

The C6201 EVM, C6201 McEVM, and C6701 EVM[2] were the first boards designed with the daughtercard interface in this specification. The interfaces on these cards provide a 32-bit asynchronous memory interface, two serial ports, two timers, and interrupt, and various status and control signals. All signals present are documented in the C6201 datasheet except for DC_CNTL[1:0] and DC_STAT[1:0], which are general-purpose inputs and outputs, respectively.

The EVM daughtercard interface pinout is provided in Table 1 and Table 2.

[2] The daughtercard interfaces on the C6201 EVM, C6201 McEVM, and C6701 EVM are all identical. Throughout this document, any reference to the C6201 EVM also applies to both the C6201 McEVM and C6701 EVM.

Table 1. TMS320C6201 EVM Peripheral Connector (J2) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	N/C	-	No connect
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX1	I/O	McBSP1 transmit clock	34	N/C	-	No connect
35	FSX1	I/O	McBSP1 transmit frame sync	36	DX1	O	McBSP1 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR1	I/O	McBSP1 receive clock	40	N/C	-	No connect
41	FSR1	I/O	McBSP1 receive frame sync	42	DR1	I	McBSP1 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	N/C	-	No connect	48	N/C	-	No connect
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT7	I	External interrupt 7	54	IACK	O	Interrupt acknowledge
55	INUM3	O	Interrupt number bit 3	56	INUM2	O	Interrupt number bit 2
57	INUM1	O	Interrupt number bit 1	58	INUM0	O	Interrupt number bit 0
59	RESET	O	System reset	60	PD	O	Power down status
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	N/C	-	No connect	68	N/C	-	No connect
69	CE2#	O	Chip enable 2	70	CE3#		Chip enable 3
71	DMAC3	O	DMA condition for channel 3	72	DMAC2	O	DMA condition for channel 2
73	DMAC1	O	DMA condition for channel 1	74	DMAC0	O	DMA condition for channel 0
75	GND	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	CLKOUT2	O	CPU clock / 2
79	GND	Vss	System ground	80	GND	Vss	System ground

Table 2. TMS320C6201 EVM Memory Connector (J1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	EA21	O	EMIF address pin 21	4	EA20	O	EMIF address pin 20
5	EA19	O	EMIF address pin 19	6	EA18	O	EMIF address pin 18
7	EA17	O	EMIF address pin 17	8	EA16	O	EMIF address pin 16
9	EA15	O	EMIF address pin 15	10	EA14	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	EA13	O	EMIF address pin 13	14	EA12	O	EMIF address pin 12
15	EA11	O	EMIF address pin 11	16	EA10	O	EMIF address pin 10
17	EA9	O	EMIF address pin 9	18	EA8	O	EMIF address pin 8
19	EA7	O	EMIF address pin 7	20	EA6	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	EA5	O	EMIF address pin 5	24	EA4	O	EMIF address pin 4
25	EA3	O	EMIF address pin 3	26	EA2	O	EMIF address pin 2
27	BE3#	O	EMIF byte enable 3	28	BE2#	O	EMIF byte enable 2
29	BE1#	O	EMIF byte enable 1	30	BE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	ED31	I/O	EMIF data pin 31	34	ED30	I/O	EMIF data pin 30
35	ED29	I/O	EMIF data pin 29	36	ED28	I/O	EMIF data pin 28
37	ED27	I/O	EMIF data pin 27	38	ED26	I/O	EMIF data pin 26
39	ED25	I/O	EMIF data pin 25	40	ED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	ED23	I/O	EMIF data pin 23	44	ED22	I/O	EMIF data pin 22
45	ED21	I/O	EMIF data pin 21	46	ED20	I/O	EMIF data pin 20
47	ED19	I/O	EMIF data pin 19	48	ED18	I/O	EMIF data pin 18
49	ED17	I/O	EMIF data pin 17	50	ED16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	ED15	I/O	EMIF data pin 15	54	ED14	I/O	EMIF data pin 14
55	ED13	I/O	EMIF data pin 13	56	ED12	I/O	EMIF data pin 12
57	ED11	I/O	EMIF data pin 11	58	ED10	I/O	EMIF data pin 10
59	ED9	I/O	EMIF data pin 9	60	ED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	ED7	I/O	EMIF data pin 7	64	ED6	I/O	EMIF data pin 6
65	ED5	I/O	EMIF data pin 5	66	ED4	I/O	EMIF data pin 4
67	ED3	I/O	EMIF data pin 3	68	ED2	I/O	EMIF data pin 2
69	ED1	I/O	EMIF data pin 1	70	ED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	ARE#	O	EMIF async read enable	74	AWE#	O	EMIF async write enable
75	AOE#	O	EMIF async output enable	76	ARDY	I	EMIF asynchronous ready
77	N/C	-	No connect	78	CE1#	O	Chip enable 1
79	GND	Vss	System ground	80	GND	Vss	System ground

TMS320C6211 DSK

The interface of the TMS320C6211 DSK was designed using most of the same signals as the EVM. The main differences between the C6211 DSK and the C6201 EVM interfaces are that signals not physically present on the C6211 were removed, there is only one McBSP available, an additional external memory chip enables is available, and all of the DSP interrupts are available. The connectors also include the hold interface signals, though the board does not facilitate a daughtercard mastering the memory on the DSK. These signals can only be used to control daughtercard memory. The daughtercard connectors for the C6211 DSK are shown in Table 3 and Table 4.

Table 3. TMS320C6211 DSK Peripheral Connector (J2) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	HOLD#	I	EMIF hold request
13	N/C	-	No connect	14	HOLDA#	O	EMIF hold acknowledge
15	N/C	-	No connect	16	BUSREQ	O	EMIF bus request
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	N/C	-	No connect	22	N/C	-	No connect
23	N/C	-	No connect	24	N/C	-	No connect
25	GND	Vss	System ground	26	GND	Vss	System ground
27	N/C	-	No connect	28	N/C	-	No connect
29	N/C	-	No connect	30	N/C	-	No connect
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX1	I/O	McBSP1 transmit clock	34	N/C	-	No connect
35	FSX1	I/O	McBSP1 transmit frame sync	36	DX1	O	McBSP1 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR1	I/O	McBSP1 receive clock	40	N/C	-	No connect
41	FSR1	I/O	McBSP1 receive frame sync	42	DR1	I	McBSP1 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	NMI	I	Non-maskable interrupt	48	EXT_INT5	I	External interrupt 5
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT4	I	External interrupt 4	54	N/C	-	No connect
55	N/C	-	No connect	56	N/C	-	No connect
57	N/C	-	No connect	58	N/C	-	No connect
59	RESET	O	System reset	60	N/C	-	No connect
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	EXT_INT6	I	External interrupt 6	68	EXT_INT7	I	External interrupt 7
69	CE3#	O	Chip enable 3	70	N/C	-	No connect
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	GND	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	ECLKOUT	O	EMIF clock
79	GND	Vss	System ground	80	GND	Vss	System ground

Table 4. TMS320C6211 DSK Memory Connector (J1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	EA21	O	EMIF address pin 21	4	EA20	O	EMIF address pin 20
5	EA19	O	EMIF address pin 19	6	EA18	O	EMIF address pin 18
7	EA17	O	EMIF address pin 17	8	EA16	O	EMIF address pin 16
9	EA15	O	EMIF address pin 15	10	EA14	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	EA13	O	EMIF address pin 13	14	EA12	O	EMIF address pin 12
15	EA11	O	EMIF address pin 11	16	EA10	O	EMIF address pin 10
17	EA9	O	EMIF address pin 9	18	EA8	O	EMIF address pin 8
19	EA7	O	EMIF address pin 7	20	EA6	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	EA5	O	EMIF address pin 5	24	EA4	O	EMIF address pin 4
25	EA3	O	EMIF address pin 3	26	EA2	O	EMIF address pin 2
27	BE3#	O	EMIF byte enable 3	28	BE2#	O	EMIF byte enable 2
29	BE1#	O	EMIF byte enable 1	30	BE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	ED31	I/O	EMIF data pin 31	34	ED30	I/O	EMIF data pin 30
35	ED29	I/O	EMIF data pin 29	36	ED28	I/O	EMIF data pin 28
37	ED27	I/O	EMIF data pin 27	38	ED26	I/O	EMIF data pin 26
39	ED25	I/O	EMIF data pin 25	40	ED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	ED23	I/O	EMIF data pin 23	44	ED22	I/O	EMIF data pin 22
45	ED21	I/O	EMIF data pin 21	46	ED20	I/O	EMIF data pin 20
47	ED19	I/O	EMIF data pin 19	48	ED18	I/O	EMIF data pin 18
49	ED17	I/O	EMIF data pin 17	50	ED16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	ED15	I/O	EMIF data pin 15	54	ED14	I/O	EMIF data pin 14
55	ED13	I/O	EMIF data pin 13	56	ED12	I/O	EMIF data pin 12
57	ED11	I/O	EMIF data pin 11	58	ED10	I/O	EMIF data pin 10
59	ED9	I/O	EMIF data pin 9	60	ED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
63	ED7	I/O	EMIF data pin 7	64	ED6	I/O	EMIF data pin 6
65	ED5	I/O	EMIF data pin 5	66	ED4	I/O	EMIF data pin 4
67	ED3	I/O	EMIF data pin 3	68	ED2	I/O	EMIF data pin 2
69	ED1	I/O	EMIF data pin 1	70	ED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	ARE#	O	EMIF async read enable	74	AWE#	O	EMIF async write enable
75	AOE#	O	EMIF async output enable	76	ARDY	I	EMIF asynchronous ready
77	N/C	-	No connect	78	CE2#	O	Chip enable 2
79	GND	Vss	System ground	80	GND	Vss	System ground

TMS320C6711 DSK

The interface on the TMS320C6711 DSK is identical to that of the C6211 DSK with the second McBSP added and the hold interface signals removed. The other minor differences include CE3 moving and NMI being removed.

The C6711 DSK daughtercard connectors are shown in Table 5 and Table 6.

Table 5. TMS320C6711 DSK Peripheral Connector (J2) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	N/C	-	No connect
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX1	I/O	McBSP1 transmit clock	34	N/C	-	No connect
35	FSX1	I/O	McBSP1 transmit frame sync	36	DX1	O	McBSP1 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR1	I/O	McBSP1 receive clock	40	N/C	-	No connect
41	FSR1	I/O	McBSP1 receive frame sync	42	DR1	I	McBSP1 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	N/C	-	No connect	48	EXT_INT5	I	External interrupt 5
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT4	I	External interrupt 4	54	N/C	-	No connect
55	N/C	-	No connect	56	N/C	-	No connect
57	N/C	-	No connect	58	N/C	-	No connect
59	RESET	O	System reset	60	N/C	-	No connect
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	EXT_INT6	I	External interrupt 6	68	EXT_INT7	I	External interrupt 7
69	N/C	-	No connect	70	N/C	-	No connect
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	GND	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	ECLKOUT	O	EMIF clock
79	GND	Vss	System ground	80	GND	Vss	System ground

Table 6. TMS320C6711 DSK Memory Connector (J1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	EA21	O	EMIF address pin 21	4	EA20	O	EMIF address pin 20
5	EA19	O	EMIF address pin 19	6	EA18	O	EMIF address pin 18
7	EA17	O	EMIF address pin 17	8	EA16	O	EMIF address pin 16
9	EA15	O	EMIF address pin 15	10	EA14	O	EMIF address pin 14
11	GND	Vss	System ground	12	GND	Vss	System ground
13	EA13	O	EMIF address pin 13	14	EA12	O	EMIF address pin 12
15	EA11	O	EMIF address pin 11	16	EA10	O	EMIF address pin 10
17	EA9	O	EMIF address pin 9	18	EA8	O	EMIF address pin 8
19	EA7	O	EMIF address pin 7	20	EA6	O	EMIF address pin 6
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	EA5	O	EMIF address pin 5	24	EA4	O	EMIF address pin 4
25	EA3	O	EMIF address pin 3	26	EA2	O	EMIF address pin 2
27	BE3#	O	EMIF byte enable 3	28	BE2#	O	EMIF byte enable 2
29	BE1#	O	EMIF byte enable 1	30	BE0#	O	EMIF byte enable 0
31	GND	Vss	System ground	32	GND	Vss	System ground
33	ED31	I/O	EMIF data pin 31	34	ED30	I/O	EMIF data pin 30
35	ED29	I/O	EMIF data pin 29	36	ED28	I/O	EMIF data pin 28
37	ED27	I/O	EMIF data pin 27	38	ED26	I/O	EMIF data pin 26
39	ED25	I/O	EMIF data pin 25	40	ED24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	ED23	I/O	EMIF data pin 23	44	ED22	I/O	EMIF data pin 22
45	ED21	I/O	EMIF data pin 21	46	ED20	I/O	EMIF data pin 20
47	ED19	I/O	EMIF data pin 19	48	ED18	I/O	EMIF data pin 18
49	ED17	I/O	EMIF data pin 17	50	ED16	I/O	EMIF data pin 16

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
51	GND	Vss	System ground	52	GND	Vss	System ground
53	ED15	I/O	EMIF data pin 15	54	ED14	I/O	EMIF data pin 14
55	ED13	I/O	EMIF data pin 13	56	ED12	I/O	EMIF data pin 12
57	ED11	I/O	EMIF data pin 11	58	ED10	I/O	EMIF data pin 10
59	ED9	I/O	EMIF data pin 9	60	ED8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	ED7	I/O	EMIF data pin 7	64	ED6	I/O	EMIF data pin 6
65	ED5	I/O	EMIF data pin 5	66	ED4	I/O	EMIF data pin 4
67	ED3	I/O	EMIF data pin 3	68	ED2	I/O	EMIF data pin 2
69	ED1	I/O	EMIF data pin 1	70	ED0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	ARE#	O	EMIF async read enable	74	AWE#	O	EMIF async write enable
75	AOE#	O	EMIF async output enable	76	ARDY	I	EMIF asynchronous ready
77	CE3#	O	Chip enable 3	78	CE2#	O	Chip enable 2
79	GND	Vss	System ground	80	GND	Vss	System ground

TMS320C6202 EVM (Blue Wave Systems)

The C6202 EVM (PCI/C6202-EVM™) by Blue Wave Systems also includes a daughtercard interface, which is based on the C6201 EVM interface but uses the expansion bus for the asynchronous parallel memory interface. The remaining signals are the same as on the C6201 EVM with the addition of more chip selects, more interrupts, and no general-purpose I/O signals. The daughtercard connectors include all expansion bus signals, which provide the host interface to the daughtercard. Documentation describing the use of the daughtercard on the PCI/C6202-EVM is available from Blue Wave Systems.

The daughtercard connectors for the PCI/C6202-EVM are shown in Table 7 and Table 8.

Table 7. PCI/C6202-EVM Peripheral Connector (J2) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	XHOLD#	I	XBUS hold request
13	N/C	-	No connect	14	XHOLDA#	O	XBUS hold acknowledge
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	N/C	-	No connect
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX1	I/O	McBSP1 transmit clock	34	N/C	-	No connect
35	FSX1	I/O	McBSP1 transmit frame sync	36	DX1	O	McBSP1 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR1	I/O	McBSP1 receive clock	40	N/C	-	No connect
41	FSR1	I/O	McBSP1 receive frame sync	42	DR1	I	McBSP1 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT0	O	Timer 0 output	46	TINP0	I	Timer 0 input
47	NMI	I	Non-maskable interrupt	48	EXT_INT6	I	External interrupt 6
49	TOUT1	O	Timer 1 output	50	TINP1	I	Timer 1 input
51	GND	Vss	System ground	52	GND	Vss	System ground
53	EXT_INT7	I	External interrupt 7	54	IACK	O	Interrupt acknowledge
55	INUM3	O	Interrupt number bit 3	56	INUM2	O	Interrupt number bit 2
57	INUM1	O	Interrupt number bit 1	58	INUM0	O	Interrupt number bit 0
59	RESET	O	System reset	60	PD	O	Power down status
61	GND	Vss	System ground	62	GND	Vss	System ground
63	N/C	-	No connect	64	N/C	-	No connect
65	N/C	-	No connect	66	N/C	-	No connect
67	EXT_INT5	I	External interrupt 5	68	EXT_INT4	I	External interrupt 4
69	XCE2#	O	XBUS Chip enable 2	70	XCE3#		XBUS Chip enable 3
71	DMAC3	O	DMA condition for channel 3	72	DMAC2	O	DMA condition for channel 2
73	DMAC1	O	DMA condition for channel 1	74	DMAC0	O	DMA condition for channel 0
75	GND	Vss	System ground	76	GND	Vss	System ground
77	GND	Vss	System ground	78	CLKOUT2	O	CPU clock / 2
79	GND	Vss	System ground	80	GND	Vss	System ground

Table 8. PCI/C6202-EVM Memory Connector (J1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	N/C	-	No connect	4	N/C	-	No connect
5	XFCLK	O	XBUS FIFO clock	6	XCLKIN	I	XBUS input clock
7	XCE2#	O	XBUS chip enable 2	8	XCE3#	O	XBUS chip enable 3
9	N/C	-	No connect	10	N/C	-	No connect
11	GND	Vss	System ground	12	GND	Vss	System ground
13	XW/R	I	XBUS read/write strobe	14	XCNTL	I	XBUS control
15	XAS#	I/O	XBUS address strobe	16	XCS#	I	XBUS host chip select
17	XHOLDA	I/O	XBUS hold acknowledge	18	XHOLD	I/O	XBUS hold request
19	XBOFF	I	XBUS back off	20	XBLAST	I/O	XBUS last-in-burst
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	XA5	I/O	XBUS address pin 5	24	XA4	I/O	XBUS address pin 4
25	XA3	I/O	XBUS address pin 3	26	XA2	I/O	XBUS address pin 2
27	XBE3#	I/O	XBUS byte enable 3	28	XBE2#	I/O	XBUS byte enable 2
29	XBE1#	I/O	XBUS byte enable 1	30	XBE0#	I/O	XBUS byte enable 0

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
31	GND	Vss	System ground	32	GND	Vss	System ground
33	XD31	I/O	XBUS data pin 31	34	XD30	I/O	XBUS data pin 30
35	XD29	I/O	XBUS data pin 29	36	XD28	I/O	XBUS data pin 28
37	XD27	I/O	XBUS data pin 27	38	XD26	I/O	XBUS data pin 26
39	XD25	I/O	XBUS data pin 25	40	XD24	I/O	XBUS data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	XD23	I/O	XBUS data pin 23	44	XD22	I/O	XBUS data pin 22
45	XD21	I/O	XBUS data pin 21	46	XD20	I/O	XBUS data pin 20
47	XD19	I/O	XBUS data pin 19	48	XD18	I/O	XBUS data pin 18
49	XD17	I/O	XBUS data pin 17	50	XD16	I/O	XBUS data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	XD15	I/O	XBUS data pin 15	54	XD14	I/O	XBUS data pin 14
55	XD13	I/O	XBUS data pin 13	56	XD12	I/O	XBUS data pin 12
57	XD11	I/O	XBUS data pin 11	58	XD10	I/O	XBUS data pin 10
59	XD9	I/O	XBUS data pin 9	60	XD8	I/O	XBUS data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	XD7	I/O	XBUS data pin 7	64	XD6	I/O	XBUS data pin 6
65	XD5	I/O	XBUS data pin 5	66	XD4	I/O	XBUS data pin 4
67	XD3	I/O	XBUS data pin 3	68	XD2	I/O	XBUS data pin 2
69	XD1	I/O	XBUS data pin 1	70	XD0	I/O	XBUS data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	XRE#	O	XBUS async read enable	74	XWE#	O	XBUS async write enable
75	XOE#	O	XBUS async output enable	76	XRDY	I/O	XBUS asynchronous ready
77	XCE1#	O	XBUS chip enable 1	78	XCE0#	O	XBUS chip enable 0
79	GND	Vss	System ground	80	GND	Vss	System ground

TMS320C5402 DSK

The C5402 DSK is the first C5000 DSP board to include a compatible daughtercard interface. This board has an interface based on that of the C6201 EVM, as well. There are several differences based on the fact that the C54x has a different memory interface than the C6000 DSPs, and the functionality of the peripherals differ slightly. The interface still provides a 32-bit data bus, though accesses are optimized for the default width of 16 bits. There are a number of different signals available that are not present on the C6201 interface due to the differences between the DSPs. All signals that are not on the C6201 EVM interface are documented in the C5402 datasheet except for DCINT, which is a system-to-daughtercard interrupt generated in hardware.

The daughtercard interface on the C5402 DSK also contains the signal DC_DET#, which is used to detect the presence of a daughtercard. This pin must be either physically connected to ground (recommended, as it is a ground pin on most interfaces) or pulled low in order for the C5402 DSK to provide the daughtercard with power. If the C5402 DSK does not detect a ‘low’ on this pin, then no voltage is provided to the daughtercard.

The daughtercard connectors for the C5402 DSK are shown in Table 9 and Table 10.

Table 9. TMS320C5402 DSK Peripheral Connector (J2) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	12V	Vcc	12V voltage supply pin	2	-12V	Vcc	-12V voltage supply pin
3	GND	Vss	System ground	4	GND	Vss	System ground
5	5V	Vcc	5V voltage supply pin	6	5V	Vcc	5V voltage supply pin
7	GND	Vss	System ground	8	GND	Vss	System ground
9	5V	Vcc	5V voltage supply pin	10	5V	Vcc	5V voltage supply pin
11	N/C	-	No connect	12	N/C	-	No connect
13	N/C	-	No connect	14	N/C	-	No connect
15	N/C	-	No connect	16	N/C	-	No connect
17	N/C	-	No connect	18	N/C	-	No connect
19	3.3V	Vcc	3.3V voltage supply pin	20	3.3V	Vcc	3.3V voltage supply pin
21	CLKX0	I/O	McBSP0 transmit clock	22	N/C	-	No connect
23	FSX0	I/O	McBSP0 transmit frame sync	24	DX0	O	McBSP0 transmit
25	GND	Vss	System ground	26	GND	Vss	System ground
27	CLKR0	I/O	McBSP0 receive clock	28	N/C	-	No connect
29	FSR0	I/O	McBSP0 receive frame sync	30	DR0	I	McBSP0 receive data
31	GND	Vss	System ground	32	GND	Vss	System ground
33	CLKX1	I/O	McBSP1 transmit clock	34	N/C	-	No connect
35	FSX1	I/O	McBSP1 transmit frame sync	36	DX1	O	McBSP1 transmit data
37	GND	Vss	System ground	38	GND	Vss	System ground
39	CLKR1	I/O	McBSP1 receive clock	40	N/C	-	No connect
41	FSR1	I/O	McBSP1 receive frame sync	42	DR1	I	McBSP1 receive data
43	GND	Vss	System ground	44	GND	Vss	System ground
45	TOUT	O	Timer output	46	N/C	-	No connect
47	N/C	-	No connect	48	INT1#	I	Interrupt 1
49	XF	O	External flag	50	BIO#	I	Branch control
51	GND	Vss	System ground	52	GND	Vss	System ground
53	INT0#	I	Interrupt 0	54	IACK	O	Interrupt acknowledge
55	N/C	-	No connect	56	IOSTRB#	O	I/O strobe
57	MSC#	O	Microstate complete	58	IAQ#	O	Instruction acquisition
59	RESET	O	System reset	60	DCINT#	O	Daughtercard interrupt
61	GND	Vss	System ground	62	GND	Vss	System ground
63	CNTL1	O	Daughtercard control 1	64	CNTL0	O	Daughtercard control
65	STAT1	I	Daughtercard status 1	66	STAT0	I	Daughtercard status
67	INT2#	I	Interrupt 2	68	INT3#	I	Interrupt 3
69	PS#	O	Program memory select	70	IS#	O	I/O memory select
71	N/C	-	No connect	72	N/C	-	No connect
73	N/C	-	No connect	74	N/C	-	No connect
75	DC_DET#	I	Daughtercard detect	76	GND	Vss	System ground
77	GND	Vss	System ground	78	CLKOUT	O	Output clock
79	GND	Vss	System ground	80	GND	Vss	System ground

Table 10. TMS320C5402 DSK Memory Connector (J1) Pinout

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	5V	Vcc	5V voltage supply pin	2	5V	Vcc	5V voltage supply pin
3	A19	O	EMIF address pin 19	4	A18	O	EMIF address pin 18
5	A17	O	EMIF address pin 17	6	A16	O	EMIF address pin 16
7	A15	O	EMIF address pin 15	8	A14	O	EMIF address pin 14
9	A13	O	EMIF address pin 13	10	A12	O	EMIF address pin 12
11	GND	Vss	System ground	12	GND	Vss	System ground
13	A11	O	EMIF address pin 11	14	A10	O	EMIF address pin 10
15	A9	O	EMIF address pin 9	16	A8	O	EMIF address pin 8
17	A7	O	EMIF address pin 7	18	A6	O	EMIF address pin 6
19	A5	O	EMIF address pin 5	20	A4	O	EMIF address pin 4
21	5V	Vcc	5V voltage supply pin	22	5V	Vcc	5V voltage supply pin
23	A3	O	EMIF address pin 3	24	A2	O	EMIF address pin 2
25	A1	O	EMIF address pin 1	26	A0	O	EMIF address pin 0
27	A21	O	EMIF address pin 21	28	A20	O	EMIF address pin 20
29	GND	Vss	System ground	30	GND	Vss	System ground
31	GND	Vss	System ground	32	GND	Vss	System ground
33	D31	I/O	EMIF data pin 31	34	D30	I/O	EMIF data pin 30
35	D29	I/O	EMIF data pin 29	36	D28	I/O	EMIF data pin 28
37	D27	I/O	EMIF data pin 27	38	D26	I/O	EMIF data pin 26
39	D25	I/O	EMIF data pin 25	40	D24	I/O	EMIF data pin 24
41	3.3V	Vcc	3.3V voltage supply pin	42	3.3V	Vcc	3.3V voltage supply pin
43	D23	I/O	EMIF data pin 23	44	D22	I/O	EMIF data pin 22
45	D21	I/O	EMIF data pin 21	46	D20	I/O	EMIF data pin 20
47	D19	I/O	EMIF data pin 19	48	D18	I/O	EMIF data pin 18
49	D17	I/O	EMIF data pin 17	50	D16	I/O	EMIF data pin 16
51	GND	Vss	System ground	52	GND	Vss	System ground
53	D15	I/O	EMIF data pin 15	54	D14	I/O	EMIF data pin 14
55	D13	I/O	EMIF data pin 13	56	D12	I/O	EMIF data pin 12
57	D11	I/O	EMIF data pin 11	58	D10	I/O	EMIF data pin 10
59	D9	I/O	EMIF data pin 9	60	D8	I/O	EMIF data pin 8
61	GND	Vss	System ground	62	GND	Vss	System ground
63	D7	I/O	EMIF data pin 7	64	D6	I/O	EMIF data pin 6
65	D5	I/O	EMIF data pin 5	66	D4	I/O	EMIF data pin 4
67	D3	I/O	EMIF data pin 3	68	D2	I/O	EMIF data pin 2
69	D1	I/O	EMIF data pin 1	70	D0	I/O	EMIF data pin 0
71	GND	Vss	System ground	72	GND	Vss	System ground
73	RE#	O	EMIF async read enable	74	WE#	O	EMIF async write enable
75	OE#	O	EMIF async output enable	76	RDY	I	EMIF asynchronous ready
77	MSTRB#	O	Memory strobe	78	DS#	O	Data memory select
79	GND	Vss	System ground	80	GND	Vss	System ground

2.3 Existing Interface Summary

The features of each of the existing daughtercard interfaces are provided in Table 11. The text following the table describes the differences in detail. Address ranges are provided per memory space, and represent the range of contiguous memory available to the daughtercard. Note that the address ranges are provided in bytes, regardless of the addressing capabilities of the interfaces. Details on the addressable memory of each card are outlined following the table.

Table 11. Existing Daughtercard Interface Features

		C6201 EVM	C6211 DSK	C6711 DSK	C5402 DSK	C6202 EVM
Memory interface	**Width**	8/16/32[3]	8/16/32	8/16/32	16/32	32
	Addressing	Byte	Byte	Byte	16-bit	Byte
	Accesses	Byte	Byte	Byte	16-bit word	32-bit word
		16-bit word	16-bit word	16-bit word	32-bit word	
		32-bit word	32-bit word	32-bit word		
	Chip selects	1-3	2	2	3	4
	Memory types	Async	Async	Async	Async	Async/ Sync FIFO
	Addressable Memory	CE1: 3MB	CE2: 4MB	CE2: 4MB	DS: 2MB	XCE0: 64B
		CE2: 4MB	CE3: 4MB	CE3: 4MB	PS: 1MB	XCE1: 64B
		CE3: 4MB			IS: 2MB	XCE2: 64B
						XCE3: 64B
Serial Ports		2 McBSPs	1 McBSP	2 McBSPs	2 McBSPs	2 McBSPs
Timers		2 TINP	2 TINP	2 TINP	1 TOUT	2 TINP
		2 TOUT	2 TOUT	2 TOUT		2 TOUT
Interrupts	**DC to DSP**	1	5	4	4	5
	DSP to DC	0	0	0	1	0
DSP/System status		IACK, INUM, DMAC, RESET, PD	RESET	RESET	IACK, IAQ, XF, BIO, MSC, RESET	IACK, INUM, DMAC, RESET, PD
GPIO		2 input	2 input	2 input	2 input	None
		2 output	2 output	2 output	2 output	
Host I/F		None	None	None	None	32-bit

2.4 Memory Interface

The memory interfaces currently available with the existing daughtercard interfaces vary between boards due to architectural differences between the DSPs. These differences are:

- **C6201 EVM:** The EVM provides an asynchronous memory interface capable of communicating with 32-bit memory. There is one primary chip select, with up to two more optionally available (selectable between system and daughtercard memory). The interface is byte addressable, with 20 address lines and individual byte enables. The memory is controlled with separate output, read, and write enables. A ready input to the DSP is

[3] All RAM is 32-bit only. 8- and 16-bit modes are supported for ROM only

available to indicate a memory is not ready. 8-bit and 16-bit ROM is also supported. For these modes the memory is always aligned with the lowest-numbered data lines.

The addressable memory is not identical between the three memory areas. The primary memory space (CE1#) has 3MB of addressable memory available for use. This 3MB comprises the daughtercard addresses of DC_EA[21:2] = 0x00000 – 0xEFFFF (byte address range = 0x000000 – 0x1FFFFF). The second and third memory spaces (CE2# and CE3#, respectively), which are optionally available to the daughtercard, allow the use of the full daughtercard address range of 4MB: DC_EA[21:2] = 0x000000 – 0xFFFFF (byte address range = 0x000000 – 0x3FFFFF).

- **C6211 DSK, C6711 DSK:** The C6211 DSK and C6711 DSK provide an asynchronous memory interface capable of communicating with 8-, 16-, or 32-bit memory. There are two chip selects. The interface is byte addressable, with 20 address lines and individual byte enables. The memory is controlled with separate output, read, and write enables. A ready input to the DSP is available to indicate a memory is not ready. When using 8-bit or 16-bit memory the physical connection of the memory depends on the endianness of the DSP. For little endian mode of operation, the memory is attached to the low-numbered data lines. For big endian mode, the memory is attached to the high-numbered data lines.

  The addressable memory for both memory spaces are identical, offering the full 4MB of memory to the daughtercards: DC_EA[21:2] = 0x000000 – 0xFFFFF (byte address range = 0x000000 – 0x3FFFFF).

- **C5402 DSK:** The C5402 has a 16-bit memory interface, which is available to the daughtercard. This includes three memory areas (data, program, and I/O), 20 address lines (16-bit word addressing), and strobes for control. There are two types of strobes present. One is the read, write, and output enables as in the C6201 EVM. Additionally there is an I/O strobe and a memory strobe. The C5402 DSK also supports 32-bit wide memory. The additional data lines are present on the connectors and on-board logic controls accessing 32-bit words rather than 16-bit words. This is included to support cards initially designed for use with the C6201 EVM.

  The addressable memory is not identical between the three memory areas. The data memory space (DS#) offers the full address range to the daughtercard: DC_A[19:0] = 0x00000 – 0xFFFFF. Data memory on the daughtercard can be accessed either as 16-bit or 32-bit words, which results in 1M x 16 or 1M x 32 bits of addressable memory. The two upper address bits DC_A[21:20] are used for 32-bit data accesses only, and are generated by hardware on the motherboard.

  The I/O memory space (IS#) also offers the full address range to the daughtercard: DC_A[19:0] = 0x00000 – 0xFFFFF. This memory can only be accessed as 16-bit words, resulting in 1M x 16 bits of addressable memory.

  The program memory space (PS#) has a reduced address range available to the daughtercard due to the program memory located on the motherboard. Half of the external program memory space is available: DC_A[19:0] = 0x80000 – 0xFFFFF. The memory can only be accessed as 16-bit words, resulting in 512k x 16 bits of addressable memory.

- **C6202 EVM:** The C6202 EVM uses the expansion bus as the parallel interface, which has several differences from the external memory interface. It supports 32-bit data only, is word

addressable, and has a limited address range of 16 words. The asynchronous memory control is identical to that of the C6201 EVM. Additionally, synchronous FIFOs are supported by the memory interface.

The addressable memory of the expansion bus is limited to 16 x 32-bit words per chip enable. This constitutes a daughtercard address range of DC_EA[21:2] = 0x00000 – 0x0000F for each of the four chip enables.

Serial Ports

All of the interfaces documented provide a serial interface to the daughtercard. There are some architectural differences in the DSPs that cause the functionality present to vary slightly, as described in the following list:

- **C6201 EVM, C6202 EVM, C6711 DSK:** The C6201 EVM, C6202 EVM, and C6711 DSK provide two 7-signal serial ports to the daughtercard. This includes clock, frame, and data signals for both the transmit and receive data streams, as well as a clock input to operate the serial port asynchronously to the DSP. Of the two serial interfaces present, one is dedicated to the daughtercard and one is selectable between the daughtercard and system hardware. The serial port signals may optionally be used as general-purpose I/O.

- **C6211 DSK:** The C6211 DSK provides one instance of the 7-signal serial port described above. This serial port is dedicated to the daughtercard.

- **C5402 DSK:** The C5402 DSK provides two 6-signal serial ports to the daughtercard. The serial ports are identical to those listed above, minus the external clock source input. If the clocks and or frame signals are to be generated internally by the DSP, they must be based on the internal clock.

Timers

The on-chip timers are made available to the daughtercard as well. The architectural differences between the timers of the DSPs are:

- **C6201 EVM, C6211 DSK, C6711 DSK, C6202 EVM:** Each of the two timers available consist of an input signal and an output signal. The input can be used as either a general-purpose input or as an event to be counted internally. Likewise the output signal can either be a general-purpose output, a periodic pulse, or a clock output.

- **C5402 DSK:** The C5402 DSK provides only one timer signal, TOUT0. This signal can provide a periodic pulse every time the counter for timer 0 underflows.

Interrupts

There are various levels of interrupt resources present on the different daughtercard interfaces.

- **C6201 EVM:** The C6201 EVM provides a single interrupt for the daughtercard to provide events to the DSP.

- **C6211 DSK:** The C6211 DSK provides five interrupts for the daughtercard to signal events. This includes the four maskable interrupts plus the non-maskable (system) interrupt.

- **C6711 DSK:** The C6711 DSK provides four external interrupts for the daughtercard. It does not provide the non-maskable interrupt.

- **C5402 DSK:** The C5402 DSK provides four external interrupts for the daughtercard to generate events to the DSP. Additionally there is an interrupt to the daughtercard for the DSP or system to provide events to the daughtercard.

- **C6202 EVM:** The C6202 EVM provides four maskable interrupts as well as the non-maskable interrupt for the daughtercard.

Status and Control Signals

The interfaces have several degrees of status signals, as follows:

- **C6201 EVM, C6202 EVM:** The C6201 EVM provides all the status signals present on the DSP. There is an interrupt acknowledge and interrupt number signals to indicate interrupts being serviced by the CPU. The DMA action complete signals are also provided to notify the daughtercard of DMA status and conditions. The DMA signals can also be use as general-purpose outputs. The system reset is provided to the daughtercard to synchronize with system resets. The powerdown signal is provided to inform the daughtercard when the DSP enters a low power mode (PD2 or PD3).

- **C6211 DSK, C6711 DSK:** The C6211 and C6711 DSKs do not have the status indicators that are present on the C6201. The DSKs provide only the reset signal to the daughtercard.

- **C5402 DSK:** The C5402 DSK provides several signals to the daughtercard for status and control. There are the interrupt acknowledge, instruction acquisition, branch control input, external flag output, microstate complete, and reset signals.

General-Purpose I/O

Several of the interfaces have general-purpose signals present to communicate between the DSP (or system) and the daughtercard.

- **C6201 EVM, C6211 DSK, C6711 DSK, C5402 DSK:** These EVMs and DSKs have two general-purpose inputs and two outputs for communication. These are referred to as status and control signals, respectively.

- **C6202 EVM:** The C6202 EVM does not have any general-purpose I/O. For this functionality it is necessary to use a peripheral signal in GPIO mode.

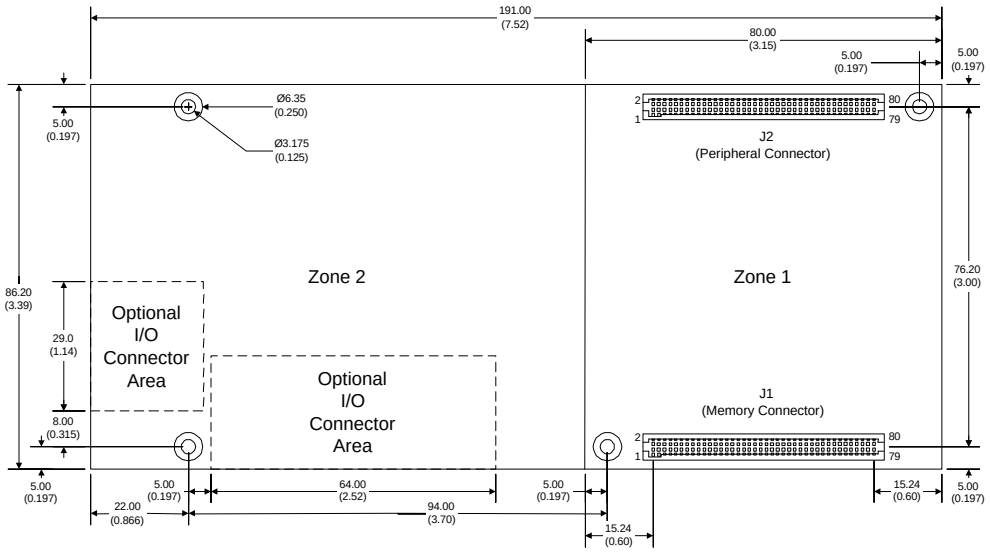
Host Interface

The C6202 EVM is currently has the only daughtercard interface that includes a host port. The expansion bus used for the parallel memory interface portion of the daughtercard interface is dual-purpose. It allows the DSP to access external asynchronous memory or synchronous FIFOs, and it also acts as a host port. The expansion bus can be used as a 32-bit asynchronous host port interface or a 32-bit synchronous host interface.

2.5 Physical Daughtercard Layout

Daughtercards designed to attach to a DSP motherboard must conform to the requirements documented in this section. The daughtercard interface consists of two signal connectors that present both an external memory interface as well as numerous peripheral signals. The physical dimensions of the daughtercard allow mounting the card on a PCI DSP motherboard while allowing the attached motherboard and daughtercard to fit within a single PCI slot of a PC. While the specification is not restricted to PCI applications, the physical dimensions of the daughtercard must fit within the maximum dimensions outlined below to be compliant.

A daughtercard may be designed to use some or all of the signals presented by the daughtercard interfaces on the DSP motherboards. Likewise, a daughtercard may be physically any size that fits within the maximum dimension of 191 x 86.2mm. Mounting holes are provided on both the daughtercard and the DSP board to allow stability. The daughtercard layout is shown in Figure 2. Note that the diagram shows the component side of the daughtercard.



NOTES:
1. All dimensions are shown in millimeters. Inch dimensions are shown in parentheses.
2. Drawing shows component side of daughtercard.
3. Full-size daughtercard area is 191 x 86.2 mm (7.52 x 3.39 in).
4. Daughtercard connectors are Samtec TFM-140-32-S-D-LC (or TFM-140-31-D-LC).

Figure 2. Daughtercard Layout

2.6 Daughtercard Connectors and Component Height

The interface on the daughtercard consists of two of any 80-pin TFM series connectors from Samtec. It is highly recommended that the largest connectors be used, as they allow the most height for components on the daughtercard. The recommended part numbers are shown in Table 12. The connectors listed for the daughtercard offer a sufficient mating height to meet the PCI's maximum component height of 14.48mm (0.57in). This mating height allows for passive components on the back side of the daughtercard that is to be attached to a PCI motherboard. Details on height restrictions of components in the daughtercard area are provided later in the document.

Table 12. Daughtercard Interface Connector Part Numbers

Location	Part Number	Mating Height
DSP Motherboard	SFM-140-L2-S-D-LC	--
Daughtercard	TFM-140-32-S-D-LC (surface mount)	11.81mm (0.465in)
	TFM-140-31-S-D-LC (through-hole)	11.43mm (0.450in)

Figure 3 depicts a mounted daughtercard designed to attach to a PCI DSP board and fit within a single PCI slot. It is assumed that a minimum of 1.27mm (0.050in)[4] clearance is maintained between components. The component heights for the pair are provided in Table 13.

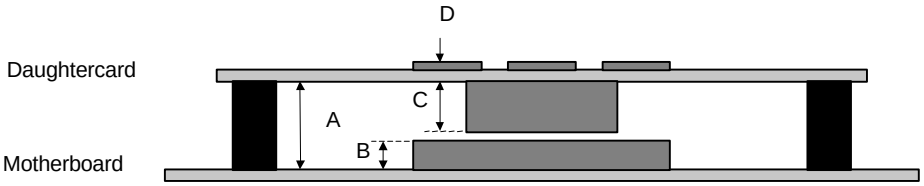


Figure 3. PCI Motherboard and Daughtercard Illustration

Table 13. PCI Motherboard and Daughtercard Component Height

Label	Description	Dimension (Zone 1)	Dimension (Zone 2)
A	Mated Height	11.81mm (0.465in)	11.81mm (0.465in)
B	Maximum motherboard Component Height	3.81mm (0.150in)	4.78mm (0.180in)
C	Maximum Daughtercard Component Height	6.73mm (0.265in)	5.97mm (0.235in)
D	Maximum "bottom-side" daughtercard component height	1.00mm (0.039in)	1.00mm (0.039in)

If a daughtercard is designed that is not required to fit within a single PCI slot, then there is more flexibility with the 'D' dimension shown. In this case, components on the back side of the board can be any height, allowing any size component or connector to be present on the daughtercard.

[4] This distance assumes the use of the TFM-40-32-S-D-LC. The distance between motherboard and daughtercard components is a minimum of 0.89mm (0.485in) if the TFM-40-31-S-D-LC is used with the height numbers in the table.

2.7 Stackable Daughtercards

Daughtercards that do not require all of the available resource presented by the DSP motherboard(s) can be designed to be “stackable”. That is to include a daughtercard interface (two SFM connector pair) to which another daughtercard can be attached. An example diagram of this is shown in Figure 4, with component heights outlined in Table 14. One suggested component placement for a stackable daughtercard is to follow the ‘D’ height requirement as defined above for a single-PCI slot card while still having pads for SFM connectors on the back side. This would allow the connectors to be added later to facilitate stacking while conforming to the stricter component requirements of the default situation.

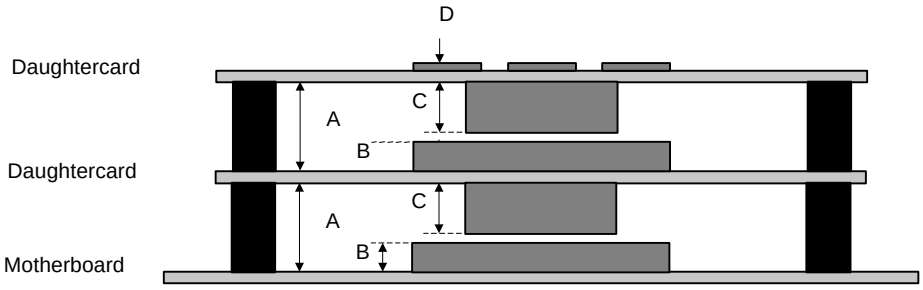


Figure 4. Stacked Daughtercard Illustration

Table 14. Stacked Daughtercard Component Height

Label	Description	Dimension (Zone 1)	Dimension (Zone 2)
A	Mated Height	11.81mm (0.465in)	11.81mm (0.465in)
B	Maximum motherboard Component Height	3.81mm (0.150in)	4.78mm (0.180in)[5]
C	Maximum Daughtercard Component Height	6.73mm (0.265in)	5.97mm (0.235in)
D	Maximum “bottom-side” daughtercard component height	None	None

Stackable daughtercards are by definition not designed to fit within a single PCI slot and do not have the same height restrictions. They can use other means to increase dimensions ‘A’ and ‘B’. It is required, however, to allow an additional daughtercard a minimum height of C’ for mounted components.

2.8 Daughtercard Design for Existing Motherboards

Due to the variations in pinout and functionality of the existing daughtercard interfaces, there are several considerations that must be taken into account when designing a daughtercard that will be used on multiple platforms. The most obvious (and simplest) solution is to only use the signals shared by all interfaces. This will guarantee that the daughtercard will always connect to available signals. A schematic showing the “least common denominator” of signals that are shared on all existing interfaces is shown in Figure 5.

[5] Note that the middle daughtercard has both the daughtercard and the motherboard component height requirements.

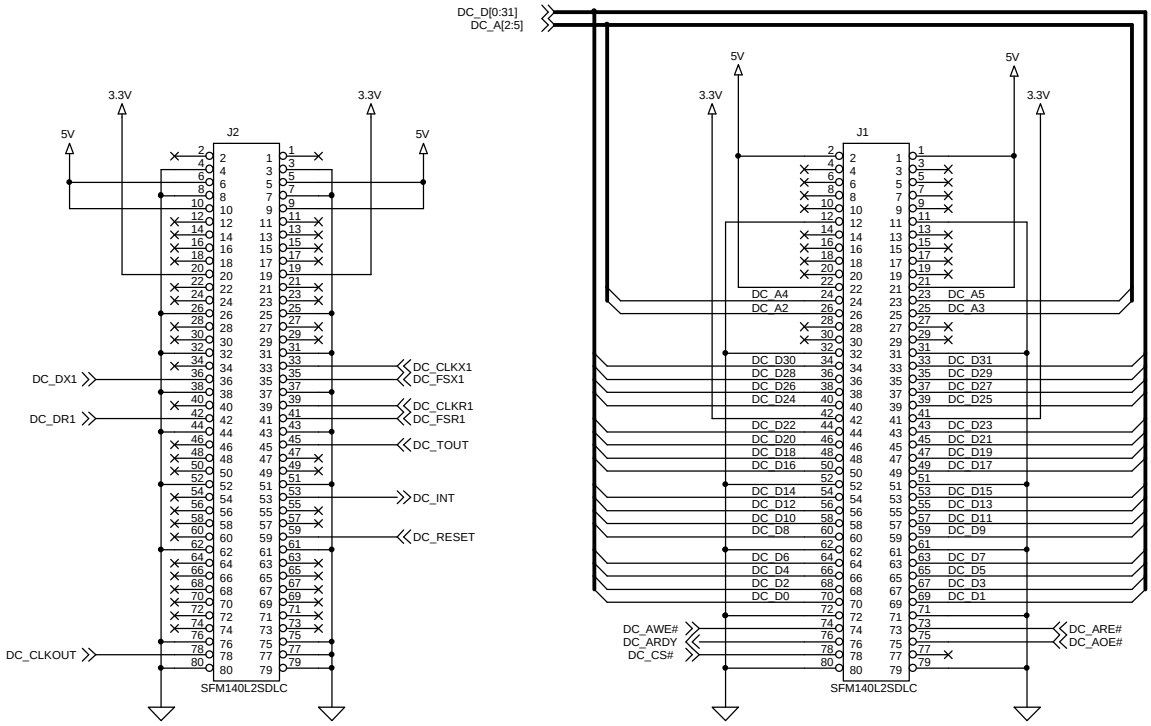


Figure 5. Least Common Denominator Signal Pinout

A daughtercard designed with only these common signals will work on all platforms. Such a card will not take advantage of any special features of any of the DSPs, however. There are a number of design options available to take advantage of other signals present on the different interfaces as well. A daughtercard can provide flexibility to allow the use of signals beyond the minimal set. Several design considerations are as follow:

Memory Interface

When designing the memory interface for the daughtercard, the simplest solution (using the least common denominator signal set) is to only require one chip select and to limit the address range to 16 words. If this is not acceptable, then there are two options: do not support all of the existing interfaces or provide hardware flexibility. The flexibility can be added to support:

- **Multiple chip selects:** If more than one chip select is required by the card, provide multiple source options that are selectable either with a switch, on-board logic, or 0-ohm resistors. All of the existing cards have two or more chip selects available, so the selection should come from these pin locations. If more than two chip selects are required, then additional source options can be used such as DC_CNTL[1:0].

- **Extended address range:** The 16 words available using the least common denominator pinout do not constitute a large memory space. A larger address range is usually required by a daughtercard containing either memory or a large number of configuration registers. Since the C6202 EVM is the only existing motherboard with this address range limitation, then if this range is not adequate either the C6202 board should not be supported or additional signals should be used to “add” address reach. Since the C6202 board is the one

that is address-limited, it is only necessary to look at additional signals present on this interface. There are a number of status signals that can be used as general-purpose outputs. These include: DMAC[3:0], TOUT[1:0], FSX[1:0], and CLKX[1:0]. Any of the signals not required by the daughtercard could be used. The daughtercard would need to provide logic to select between the always-present address signals and the general-purpose outputs of the C6202.

- **Byte enables:** Byte enables are not present on all of the interfaces. If they are included, they should be pulled to ground through resistors and optionally disconnected from the daughtercard connectors with either jumpers or 0-ohm resistors. If byte accesses are never required by the daughtercard hardware, these signals should always be disconnected.

- **Memory width:** Note that while the common memory width for all of the existing motherboards is 32-bit for the primary memory space, the default width of the C5402 is 16-bit. Therefore the performance of the C5402 is maximized for daughtercards designed with 16-bit wide memory.

- **Endian Mode:** Important to note is that for memory widths of less than 32 bits on the daughtercard will need to be designed according to the desired endian mode of operation. The C6000 devices support both big and little endian modes. The C6201 EVM supports 8-bit and 16-bit ROM to be located on the daughtercard in addition to 32-bit asynchronous memory. These reduced width memory are assumed to always be aligned with the least significant data bit (D0) aligned with DC_D0, regardless of endian mode. The C6211 DSK and C6711 DSK support 8-bit and 16-bit asynchronous memory (read and write) in addition to 32-bit. For these systems, the endian mode of the DSP affects the location of the reduced-width memory on the daughtercard. In little endian mode, the alignment is identical to that of the C6201 EVM: the least significant data bit (D0) is aligned with DC_D0. The memory alignment for the C6211 DSK and C6711 DSK in little endian mode and for the C6201 EVM in any endian mode is shown in Figure 6.

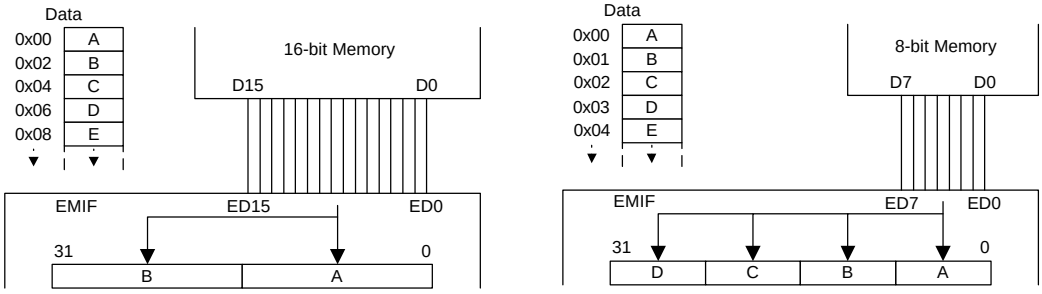


Figure 6. Little Endian Data Alignment

For big endian mode the memory must be aligned to the upper end of the data bus. The most significant bit (D7 or D15) must be aligned to DC_ED31. The memory alignment for the C6211 DSK and C6711 DSK in big endian mode is shown in Figure 7. If the data packing functionality of the C6000 is desired to be used in both big and little endian modes, then it is necessary to design the daughtercard such that it can use either the upper or the lower data lines. A daughtercard designed with a reduced-data width memory fixed at the lower data lines is still supported on the C6211 DSK and C6711 DSK, only without the data

packing support (must be addressed on 32-bit boundaries). It is important to note that the default (and most common) mode of operation of the C6211 DSK and C6711 DSK is little endian.

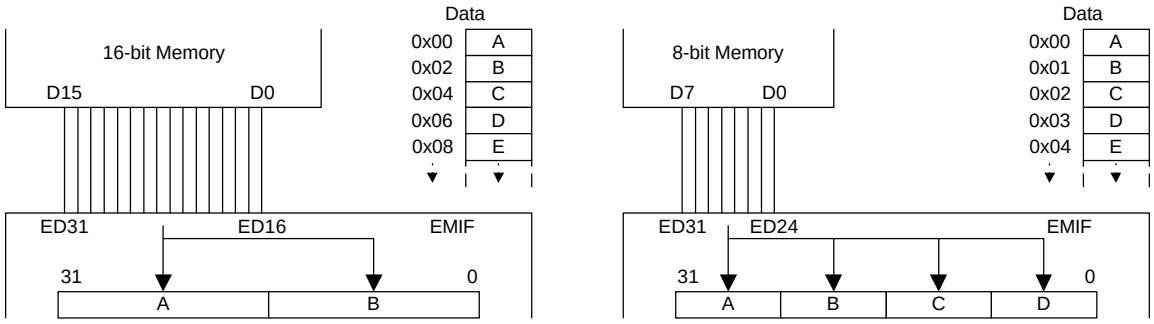


Figure 7. Big Endian Data Alignment

Serial Ports

If the serial ports are to be used, then there are several considerations to take into account to make the daughtercard operable across as many platforms as possible. The most important choice is to decide which signal set to use if only one serial port is required by the daughtercard. Since the C6211 DSK only has one serial port, and its location is the same as the serial ports of the other interfaces not shared with motherboard hardware, this is the one that should be used by the daughtercard. This is the primary serial port, denoted with the letter “a” following each signal name.

Another consideration is whether the daughtercard requires CLKS functionality. If it is not required by the hardware to drive the clock generator of the McBSP, then do not use it. This functionality is not available on the C5402 DSK, so the C5402 DSK would not support daughtercards requiring this signal.

Timers

The amount of timer resource varies widely between the existing interfaces, but depending on the timer function required by the daughtercard there are workaround options. If the only timer requirement is a single periodic pulse from the DSP system to the daughtercard, then the common TOUT signal should be used. If additional functionality is required, then there needs to be some built-in hardware flexibility to allow usage across platforms.

- **Events:** The C5402 DSK does not have timer inputs that can be used by the daughtercard to send events to be counted by the DSP. In order to count events the C5402 would need to manually count events in software, using external interrupts. If a daughtercard requires that events be counted by the DSP, then to maximize the number of boards with which the hardware is compatible, the events that need to be counted by the DSP should be connected to both the TINP[1:0] signals and to unused external interrupts. This should be done using a jumper, a switch, or 0-ohm resistors. This will allow the timer peripheral to count events on the C6000 platforms, and allow the CPU to count events on the C54x platforms.

- **Additional timer pulse:** If two timer pulse outputs are required, then the second one (one is always available on the common TOUT signal) should be selectable between TOUT1 and another output. Since the C5402 DSK is the only existing platform lacking a second TOUT pin, it is only necessary to find a suitable output pin on this interface. The DSP-to-daughtercard interrupt is well suited for this. The DSP can periodically set the interrupt to the daughtercard (this will need to be managed in software by the CPU).

- **Clock outputs:** If clock outputs are required to the daughtercard, then the TOUT[1:0] pins must be multiplexed with other signals. The TOUT of the C54x devices is not capable of generating a clock output. The only alternate clock sources are the serial port clocks, which can be divided down from the CPU clock (note that they would need to divide down to the same frequency). If there are unused serial port clocks available on the daughtercard, then they could be used.

Interrupts

Additional interrupts may need to be used beyond the single common interrupt. The C6201 EVM is the only platform with a single interrupt. All others have four or five available to the daughtercard. There are six possible alternate interrupt sources: the four serial port frame signals (FSR[1:0] and FSX[1:0]) and the timer inputs (TINP[1:0]). If the serial port frame signals are used, then the McBSPs can be configured to generate a CPU interrupt (no DMA/EDMA events) on every new rising edge, which is identical to the external interrupts. If the timer inputs are used then the signal can be used to generate either a CPU interrupt or a DMA/EDMA event. For the timer input signals it is required, however, to generate two pulses for every interrupt/event desired. This is due to the fact that the minimum timer period is 1 and it is necessary for the internal counter to toggle between 0 and 1.

Status Indicators

The status indicators are signals generated by the DSP to notify external devices about current status and conditions. Some (like the DMAC signals) are device-specific and cannot be replicated through another signal.

Status indicators that can be represented another way the IACK, INUM, and PD signals. For IACK and INUM, these could be replicated on the memory interface by providing an address location that decodes to an “interrupt” address. The CPU can then write the interrupt number being serviced to this address. An access to this address would be seen as the IACK and the data written could be the INUM. This requires the CPU to execute this write in the interrupt service routine. The daughtercard would need to select between using the IACK/INUM signals and the memory signals.

The PD signal can be replicated by any peripheral signal that is selectable as a general-purpose output. The CPU would need to manually set the general-purpose output when entering the appropriate power-down mode.

General-Purpose I/O

The general-purpose I/O signals provided on most of the platforms are not available on the C6202 EVM. Their functionality can be replicated using either the timers, the serial ports, or the DMA. TINPx and TOUTx can be general-purpose input and output signals, respectively. The serial port signals can be used for general-purpose I/O. Also, the DMACx signals can operate as general-purpose outputs. If any of these resources are unused by the daughtercard, then the daughtercard can optionally use these signals instead.

Host Interface

A host interface cannot be replicated. Currently only the C6202 EVM has a host interface included for use by a daughtercard.

2.9 Daughtercard Signals

A daughtercard may make use of some or all of the signals presented by the DSP motherboard. For signals with multiple instances the daughtercard should use the instance with the lowest letter first. For example, if a daughtercard requires two interrupts to the CPU, it should make use of DC_INTa and DC_INTb. A third interrupt would go on DC_INTc, etc.

The reason for always using the lowest instance of a given signal is two-fold. First, a DSP may share a resource between hardware on the motherboard and the daughtercard interface. For example, on several of the existing platforms one of the serial ports is able to communicate with either an on-board codec or with daughtercard hardware. The DSP motherboards have this shared resource routed to the secondary (higher letter) instance of the signal set so if the daughtercard uses only the primary, then the DSP will have both resources available for use.

Second, it is possible to design “stackable” daughtercards. These are cards with both the TFM connector pair to attach to a DSP motherboard, plus an SFM connector pair to pass on unused daughtercard signals to a second, stacked, daughtercard. The daughtercard should make use of as many high-priority signals as required for the hardware, then pass any unused signals to the high-priority instances on the “stacked” SFM connectors. As an example, again assume a daughtercard requires two interrupt and makes use of DC_INTa and DC_INTb. The daughtercard should then pass the two lower-priority interrupts, DC_INTc and DC_INTd from the TFM connector to the SFM connector. This will facilitate the stacking of as many cards as the resources permit, in any order.

2.10 Signal Characteristics

The signal characteristics of all existing motherboards comply with the guidelines outline in the following section. These guidelines should be used when designing a daughtercard. The most important considerations for the daughtercard design are the following:

- *Buffer the daughtercard input signals for loads exceeding 20pF*. The motherboard may not supply more drive capability than this.

- *Provide 3.3V outputs to the DSP motherboard*. While most existing (but not all) motherboards are 5V-tolerant on input signals, this will not be true for new platforms due to the requirement of additional hardware.

- *Regulate the 5V and +/-12V signals*. These voltages are not regulated by the motherboard. If a regulated supply at either of these voltage levels is required, it is the responsibility of the daughtercard hardware.

- *Use only 3.3V and 5V supplies if possible*. While all motherboards (now and future) will allow for +/-12V to be supplied to the daughtercard interface, the default power supply (if not a PCI card) accompanying the product may not supply +/-12V. It may be required for the user to provide a second supply to the motherboard (or directly to the daughtercard) to provide the +/-12V.

- *Obey power supply limits*. If a daughtercard requires a voltage that is not present at the interface, or if the card requires an excess amount of power, then power should be supplied separately from the motherboard. This may be done either as part of the daughtercard, or on a supplemental card[6]. The power available to the daughtercard should be stated with the DSP motherboard documentation. The minimum power supply requirements available on current and future interfaces are provided in the “Power Supply” portion of the next section

3 Future Daughtercard Interfaces

DSP motherboards designed with daughtercard interfaces need to be compatible to the existing interfaces to facilitate the portability of daughtercards. Due to the fact that there are differences between existing boards, the interface outlined in this specification is derived from the commonality between the existing cards. Designing a motherboard using the following recommendations will allow daughtercards to interface both to old and new platforms.

3.1 Interface Signals

Figure 8 shows the schematics of the two connectors, with the pin assignments to be used on future motherboards. All pins shown as “no connect” should be treated as “reserved” for future definition. If a motherboard is designed for a DSP that has signals of an existing motherboard (as described in this document) that is not on the recommended interface, these signals should be included using the same pin assignments as on the existing interface. For example, a motherboard designed for a C6203 DSP should include the DSP status signals (DMAC, INUM, IACK, PD), if possible, using the same pin assignments as on the existing C6201 EVM and C6202 EVM. Additional chip selects (beyond the two) could be provided to J2:69 and J2:70 if not used by the motherboard, as done on the C6201 EVM and C6202 EVM, as well.

Any additional signals, either new or not previously included on an interface, to be provided by the motherboard to the daughtercard interface are considered motherboard-specific and should be provided outside of the interface documented in this specification. For additional signals, additional connectors should be provided outside of the physical layout area shown here.

[6] Note that if a supplemental power source is provided in this manner, the supplemental power planes should NOT be connected to the power planes of the motherboard.

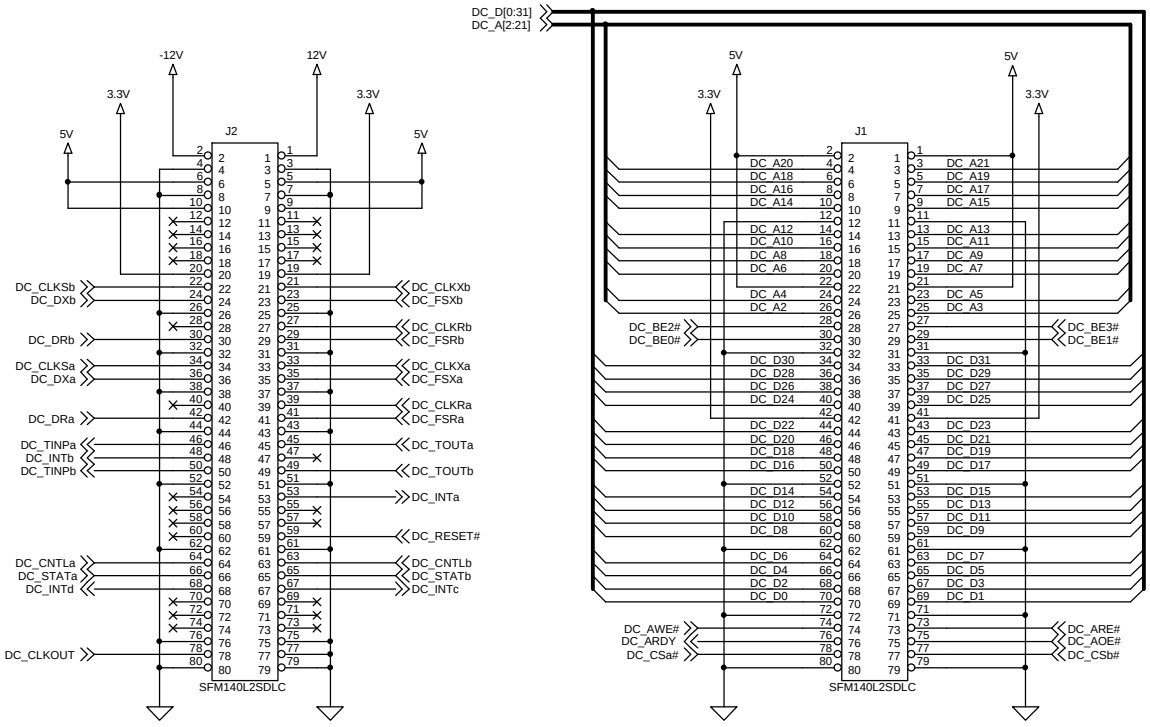


Figure 8. Recommended Future Daughtercard Interface Connectors

All of the peripheral connector signals are provided in Table 15. Signals with multiple instances are identified as “primary” or “secondary”. Signals that are shared with on-board peripherals and the daughtercard (e.g., McBSP connection to on-board codec or to daughtercard connector) should use the secondary signals. Non-shared signals, if present, should use the primary instances on the connector. This allows a daughtercard to make use one instance of the peripheral while still allowing the DSP to communicate with hardware on the motherboard. The I/O direction listed in the table is relative to the DSP on the motherboard.

Table 15. Peripheral Signal Descriptions

Signal Name	I/O	Pin	Description
DC_CLKSa	I	J2:34	Primary serial port clock source
DC_CLKRa	I/O	J2:39	Primary serial port receive clock
DC_CLKXa	I/O	J2:33	Primary serial port transmit clock
DC_FSRa	I/O	J2:41	Primary serial port receive frame sync
DC_FSXa	I/O	J2:35	Primary serial port transmit frame sync
DC_DRa	I	J2:42	Primary serial port receive data
DC_DXa	O	J2:36	Primary serial port transmit data
DC_CLKSb	I	J2:22	Secondary serial port clock source
DC_CLKRb	I/O	J2:27	Secondary serial port receive clock
DC_CLKXb	I/O	J2:21	Secondary serial port transmit clock
DC_FSRb	I/O	J2:29	Secondary serial port receive frame sync
DC_FSXb	I/O	J2:23	Secondary serial port transmit frame sync
DC_DRb	I	J2:30	Secondary serial port receive data
DC_DXb	O	J2:24	Secondary serial port transmit data
DC_TINPa	I	J2:46	Primary timer input
DC_TOUTa	O	J2:45	Primary timer output
DC_TINPb	I	J2:50	Secondary timer input
DC_TOUTb	O	J2:49	Secondary timer output
DC_INTa	I	J2:53	Primary interrupt
DC_INTb	I	J2:48	Secondary interrupt
DC_INTc	I	J2:67	Third interrupt
DC_INTd	I	J2:68	Fourth interrupt
DC_RESET#	O	J2:59	System reset signal
DC_CNTLa	O	J2:64	Daughtercard control
DC_CNTlb	O	J2:63	
DC_STATa	I	J2:66	Daughtercard status
DC_STATb	I	J2:65	
DC_CLKOUT	O	J2:78	Daughtercard clock

In all instances of signals shared between the motherboard hardware and the daughtercard interface, it is the responsibility of the motherboard hardware to make the selection. This may be done either through a hardware switch or jumper. The selection should remain static until changed by the user, and should not be changeable due to a software or hardware reset. The signals going to the daughtercard interface must placed in a hi-Z state when the signals are used by the motherboard hardware to protect any daughtercard hardware.

The memory signals that are required for the daughtercard interface connectors are described in Table 16. A 32-bit parallel memory interface is shown on the connector pair to be compatible with existing cards. Future DSPs may consist of 16-bit busses. Motherboards for these DSPs should still support the 32-bit interface to facilitate the use of existing daughtercards, along with the default data width. One way to implement this is to have the first read load a 32-bit word from the daughtercard to an on-board register. Subsequent reads from within that 32-bit word are read from the register, rather than directly from the daughtercard. And the opposite methodology for writes, with the first write to a new 32-bit word going to an on-board register and the second write causing the daughtercard access. In all likelihood the default width interface will yield higher performance, and daughtercards requiring the highest performance will take advantage of this.

Likewise, a parallel interface may be used that has a limited address range, such as in the case of the expansion bus. The full address range needs only to be present for interfaces that are intended to connect to RAM. Interfaces intended for I/O peripherals need only the address pins DC_A[2:5].

Table 16. EMIF Signal Descriptions

Signal Name	I/O	Pin	Description
DC_A[2:5]	O	J1:26:23	Address pins
DC_A[6:13]	O	J1:20:13	
DC_A[14:21]	O	J1:10:3	
DC_D[0:7]	I/O	J1:70:61	Data pins
DC_D[8:15]	I/O	J1:60:53	
DC_D[16:23]	I/O	J1:50:43	
DC_D[24:31]	I/O	J1:40:33	
DC_BE[0:3]#	O	J1:30:27	Byte enables
DC_CSa#	O	J1:78	Primary chip select
DC_CSb#	O	J1:77	Secondary chip select
DC_AOE#	O	J1:75	Asynchronous output enable
DC_ARE#	O	J1:73	Asynchronous read enable
DC_AWE#	O	J1:74	Asynchronous write enable
DC_ARDY	I	J1:76	Asynchronous ready

Daughtercard Interface Capability

When designing a daughtercard interface on a DSP motherboard there are several requirements to ensure that the interface will be useable by any daughtercard designed to the specification that uses the subset of signals made available. The key concerns are signal pinout, drive capability, timing delay, and input voltage tolerance. It is possible that DSPs used on a future motherboard will not have all of the signals specified in the recommended daughtercard pinout. In this case, it is acceptable to either leave these pins unconnected or to replicate the functionality in system hardware on the motherboard. The following are some guidelines for the interface signals.

- **Address signals**: All address signals (up to 20) available on the memory interface of the DSP must be provided to give the maximum address space to the daughtercard. This

facilitates up to 4Mbytes of external memory to be addressed per chip select. The lower 4 address signals must be provided for interfaces designed for I/O peripherals only.

- **Data signals**: 16 or 32 data signals must be provided to facilitate access to memory or parallel peripherals. The data width should be 32 bits if at all possible to allow for maximum daughtercard compatibility. If the memory interface of the DSP is of a width less than 32-bits, then the 32-bit interface may be unsupported. Alternatively (and preferred) the interface can be selectable between the different widths as done for the C5402 DSK. There are several methods that can be used for selection/detection. The bus width can be set either with a hardware switch or register setting on the motherboard or natively supported by the motherboard hardware. The interface is required to be at least 16 bits wide.

- **Chip selects**: Two chip selects must be provided to access individual memory and I/O spaces. If ROM-boot is supported on the daughtercard interface, the primary chip select (DC_CSa#) should be used for this. This may be accomplished either through a default boot mode of the DSP or by facilitating this operation in hardware after the DSP is reset. Additional chip selects may be provided using J2:69 and J2:70 if not used by the motherboard, as done on the C6201 EVM and C6202 EVM, as well.

- **Byte enables**: The four byte enables should be provided to access individual bytes within a 32-bit word. If not present on the DSP the byte enables should be pulled to ground through 30kohm resistors. Only the byte lanes the DSP uses should be pulled low (for those using less than 32-bit interfaces).

- **Asynchronous memory control**: Four asynchronous memory control signals must be available to communicate to the daughtercard memory: Output Enable (DC_AOE#), Read Enable (DC_ARE#), Write Enable (DC_AWE#), and Ready (DC_ARDY).

- **Serial Ports**: Two serial ports should be routed to the peripheral daughtercard connector. For devices or systems with only one serial port present, the primary signal set must be used. If CLKS functionality is not supported by the DSP, this should be clearly documented. Several DSP support the CLKS functionality on the CLKR signal of the McBSP. The receive clock (CLKR) is dual-purpose and can also function as CLKS. If the functionality is supported in this manner, than the motherboard should route the serial port to the daughtercard connectors as shown in Figure 9.

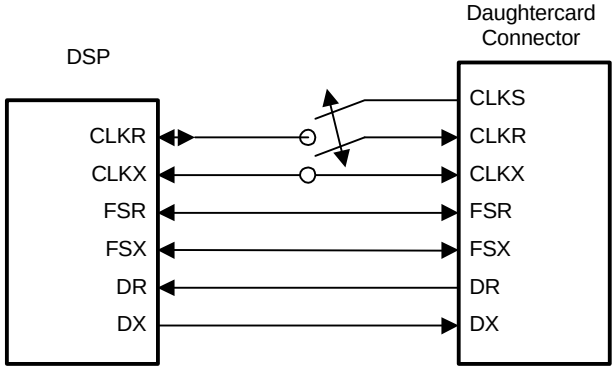


Figure 9. Recommended CLKS Implementation

- **Timers**: Two timers should be made available to the daughtercard interface. For C6000 devices this means both input and output signal pairs should be routed. On C55x devices the timer can only have an input or an output signal, so each timer signal should be routed to both the TINPx and TOUTPx pins of the daughtercard connectors. For C54x devices, which only have timer outputs, the TINPx signals should be left unconnected.

- **Interrupts**: Four interrupts (daughtercard to DSP) should be available to the daughtercard.

- **Reset**: A reset must be provided to the daughtercard. This should indicate a system reset and may optionally be set in software to provide a daughtercard-only reset.

- **Daughtercard control**: Two general-purpose signals from the DSP system to the daughtercard should be provided. These signals may be used for anything, but typically would be use as a static configuration setting or for handshaking. These should be implemented as bits in a hardware register on the motherboard or as general-purpose outputs from the DSP.

- **Daughtercard status**: Two general-purpose signals from the daughtercard to the DSP system should be provided. These signals may also be used for anything, but are typically used to report an action complete, or indicate the type of daughtercard present. These should be implemented as bits in a hardware register on the motherboard or as general-purpose inputs to the DSP.

Additional signals that are made available to the daughtercard must be done outside of the two connectors defined in this specification. Extra signal headers must conform to the component placement requirement documented and should always be considered platform-specific.

3.2 Signal Characteristics

Three things define the characteristics of the signals provided to the daughtercard: signal drive, voltage tolerance, and delay. The following paragraphs describe the signal characteristics on existing interfaces, as well as what is required of new ones.

Signal Drive

The primary requirement for a daughtercard interface is drive capability of the signals. Each signal driven to the daughtercard headers must be able to drive a 20pF load on a daughtercard. Output signals should be buffered accordingly to provide this minimum drive capability. All daughtercard interfaces currently support this.

Input Voltage Tolerance

Input signals from the daughtercard to the DSP are not required to be 5V-tolerant. Of the current interfaces, the C6201 EVM, C6211 DSK, C6711 DSK, and C5402 DSK are all 5V tolerant. Future motherboards will likely not include 5V-tolerance as it can add unnecessary signal delay, which reduces bus speed and increases system cost.

Timing Delay

Signals driven to and from the daughtercard should incur an AC timing delay on the DSP board that is as small as possible. The maximum one-way board delay of any signal should not exceed 15ns[7]. This maximum delay is for both inputs and outputs.

Lower signal delays are always advantageous. The maximum delay provided here is meant to be an absolute maximum, rather than a guideline. Delays should be as low as possible for maximum performance on any particular DSP board. If the drive requirements are met then the signals to the daughtercard interface may be left unbuffered. Current daughtercards meet this requirement.

3.3 Power Supply

The daughtercard interface requires the supply of four voltages: 3.3V, 5V, 12V, and -12V. These supplies are intended to provide basic power to the components on the card. The minimum current that the motherboard must be able to supply is provided in Table 17.

Table 17. Minimum Power Supply Requirements

Power Supply	Minimum Current Supplied
3.3V	1A
5V	1A
12V	500mA
-12V	100mA

Only the 3.3V supply is required to be regulated. The 5V and +/-12V supplies can be unregulated. It is the responsibility of the daughtercard to regulate these supplies. It is not required to provide the +/-12V with power supply that accompanies the hardware, however it should be possible to provide the +/-12V through the motherboard either by replacing the power supply or by adding a supplement supply.

3.4 Physical Requirements

The only physical restriction for a new DSP motherboard that is new to the interface requirements is that tall components are not present in both areas denoted as keepout zones in Figure 1. These two regions are intended to be available for access to I/O connectors on the daughtercards. The components on the motherboard in these zones should conform to the height restrictions of Zone 1 in Table 13. These keepout zones are to allow access to the connectors only, and are not for use by the daughtercards themselves.

[7] This is total time delay from the DSP to the daughtercard connector and includes propagation delay, buffer delay, and logic delay.

4 Summary

The daughtercard specification is designed to provide a common interface across DSP platforms within the TMS320 family. The purpose is to facilitate the design of a single daughtercard that can be used on multiple DSP platforms without requiring any hardware modifications. There are several existing interfaces for the C6000 and C5000 devices, which have some variation in pinout and functionality. Daughtercards designed to function on some or all of these motherboards require several design considerations. Likewise, a recommended signal placement is provided for new motherboards to be built while remaining compatible with the boards described in this specification. In addition to allowing a daughtercard to simply plug on to a motherboard, there are also defined means to facilitate sharing resources between the two and also stacking multiple daughtercards that use different resources. The specification is meant to be as flexible as possible from an implementation standpoint while still providing a set of rules to provide cross-platform alignment. Using this specification it is possible to use a daughtercard on many different systems with a low amount of effort required to transition. The effort is mostly in the form of software modification when switching DSP platforms.

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