NAND Memory Device Interface to the TMS320VC55x

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ABSTRACT

This document contains information needed to interface the TMS320VC55x™ (hereafter referred to as C55x™) to the NAND memory device. A complete reference design, including hardware and software interfaces, is provided. The software consists of a set of file system independent subroutines that perform the Write, Erase, Read, ReadID, Reset, and Status functions required to store and retrieve data from NAND memory device. Function descriptions are provided in this document. Source code is available electronically from the TI web site.

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1 Introduction

The C55x DSP is a suitable processor for a variety of handheld portable applications, many of which require a high-density, non-volatile storage memory. Examples of such applications include digital cameras, digital music players, and personal digital assistants (PDA's). The NAND memory device, easily interfaced to the C55x, meets these requirements. This application note describes how to interface the C55x to the 512 Mbit NAND memory device. A complete reference design is shown, including hardware and software interfaces. The software consists of a set of file system independent subroutines that perform the low level functions required to write, read, and erase data from a NAND memory device. Function descriptions are shown in this document, and the source code is available electronically from the TI web site.

2 NAND Memory Device Overview

The NAND memory device is a 3.3-V Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) device, organized as 528 bytes x 32 pages per block. The number of blocks and pages will vary with the different capacities of the NAND memory device. The NAND memory device has a 528-byte static register, allowing program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes or 528 bytes X 32 pages). Figure 1 below is layout diagram of the 512Mbit NAND memory device. The NAND memory is a serial-type memory device that uses the I/O pins for both address and data input and output, as well as for command inputs. The Erase and Program operations are automatically executed, making the device ideal for applications such as solid-state file storage, digital voice recording, image storage for digital cameras and other systems requiring high-density non-volatile memory data storage.

2.1 Data Storage

The unit of data storage for the 512Mbit NAND memory device is the page (1 page = 512 bytes + 16 bytes). The extra 16 bytes are for the user to store information about the page, ECC, logical sector number, etc. All reads and writes to a NAND memory device must be at least one page long.

Since the I/O pins are used for the data I/O and commands, the addressing of the NAND memory device's pages is done within the read, write, and erase commands. Figure 2, below, illustrates the four address cycles required by the 512Mbit NAND memory device. The details of the commands will be explained following each illustration.

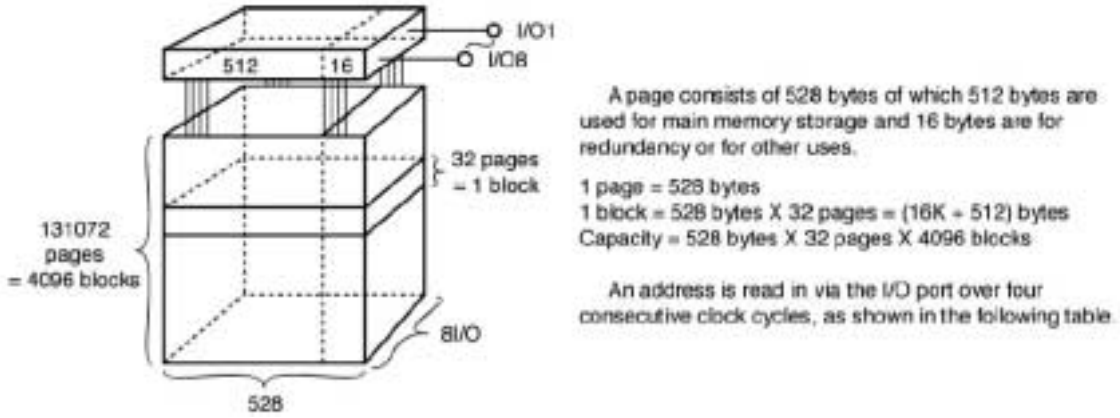

Figure 1. NAND Memory Device Layout 512Mbit

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	
First Cycle	A7	A6	A5	A4	A3	A2	A1	A0	A0 to A7: Column address
Second Cycle	A16	A15	A14	A13	A12	A11	A10	A9	A9 to A25: Page address
Third Cycle	A24	A23	A22	A21	A20	A19	A18	A17	(A14 to A25: Block address
Fourth Cycle	*L	*L	*L	*L	*L	*L	*L	A25	A9 to A13: NAND address in block)

* : A8 is automatically set to Low or High by an 00H command or an 01H command.
* : I/O2 to I/O8 must be set to Low in the fourth cycle.

Figure 2. NAND Memory Device Addressing 512Mbit

2.2 NAND Memory Device Interface

The NAND memory device interface consists of 18 pins as it can be seen from the package diagram below (Figure 3). The interface has eight I/O pins, six control pins, and a Ready/Busy pin. The eight I/O lines are used for sending commands, address, and sending/receiving data. The control lines are used to distinguish between address data and command data. Finally, the Ready/Busy line gives the status of the NAND memory device.

Figure 3. NAND Memory Device Package Diagram

The diagram below provides a detailed view of this interface. A detailed description of this interface is covered in subsequent sections of this document. There are several ways the NAND memory device is interfaced to the C55x in. Figure 4, below, illustrates the interface used in this application note.

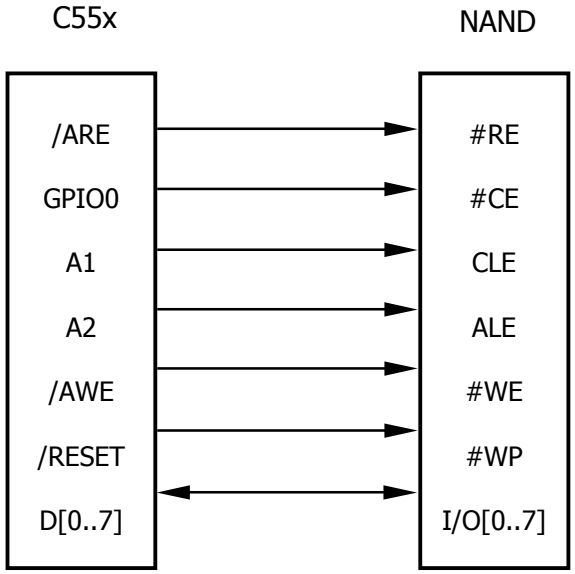

Figure 4. NAND Memory Device Interface to the C55x Diagram

2.3 NAND Memory Device Signal Descriptions

Table 1 lists the NAND memory device's I/O signal pins. A detailed description of each pin follows Table 1.

Table 1. NAND Memory Device Signals

I/O1 to 8	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready/Busy
GND	Ground Input
V_{CC}	Power Supply
V_{SS}	Ground

- **Command Latch Enable: CLE**

  The CLE input signal is controls loading of the operation mode command into the internal command register. The command latches into the command register from the I/O port on the rising edge of the WE signal while CLE is High.

- **Address Latch Enable: ALE**

  The ALE signal controls the loading of address information into the internal address register. Address information latches into the address register on the rising edge of WE when ALE is High.

- **Chip Enable: CE**

  The device goes into a low-power Standby Mode when CE goes High during a Read operation. The CE signal is ignored when the device is in the Busy state (R/B =L), such as during a Program or Erase operation, and will not enter Standby Mode even if the CE input goes high. The CE signal must stay Low during the Read Mode Busy state to ensure that memory array data is correctly transferred to the data register.

- **Write Enable: WE**

  The WE signal controls the acquisition of data from the I/O port

- **Read Enable: RE**

  The RE signal controls serial data output. Data output will be valid when RE goes low after tREA. The internal column address counter is also incremented (Address = Address + l) on this falling edge.

- **I/O Port: I/O 1 to 8**

  The I/O1 to eight pins are used as ports for transferring address, command, and input/output data to and from the device.

- **Write Protect: WP**

  The WP signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WP is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid. The signal assertion during the program or erase operation causes the operation to cancel, not interrupt, even if the card is busy.

- **Ready/Busy: R/B**

  The R/B output signal is used to indicate the operating condition of the device. The R/B signal is in Busy state (R/B = L) during the Program, Erase and Read operations and will return to Ready state (R/B = H) after completion of the operation. The output buffer for this signal is an open drain.

2.4 NAND Memory Device Status

The status of NAND memory device can be read using the Status Read command, 70H. The NAND memory device automatically implements the execution and verification of the Program and Erase operations. The Status Read function monitors the Ready/Busy status of the device, determines the result (pass /fail) of a Program or Erase operation, and determines whether the device is in Write Protect mode. The device status is output via the I/O port on the falling edge of RE after issuing the 70H, Status Read, command. The resulting information of the Status Read command 70H is outlined in the Table 2 below.

Table 2. NAND Memory Device Status

	Status	Output
I/O1	Pass/Fail	Pass: 0 Fail: 1
I/O2	Not Used	0
I/O3	Not Used	0
I/O4	Not Used	0
I/O5	Not Used	0
I/O6	Not Used	0
I/O7	Ready/Busy	Ready: 1 Busy: 0
I/O8	Write Protect	Protect: 0 Not Protected: 1

2.5 Ready/Busy Pin Status

The Ready/Busy status of the NAND memory device can be monitored using the Ready/Busy pin, pin seven. The R/B output signal is used to indicate the operating condition of the device. The R/B signal is in Busy state (R/B = L) during the Program, Erase and Read operations and will return to Ready state (R/B = H) after completion of the operation. The output buffer for this signal is an open drain (see Figure 5 below).

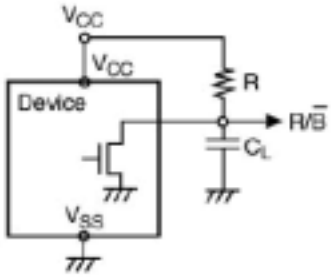

Figure 5. NAND Memory Device R/B Output Buffer

2.6 NAND Memory Device Commands

Table 3, below, lists commands for the NAND memory device. The following sections will describe each command in more detail and give the timing diagram. Commands 11H (AutoProgram (Dummy)), 15H (AutoProgram (Cache)), 71H (Status Read (2)), and 91H (ID Read (2)), used with multi block programming, will not be covered in this application note.

Table 3. NAND Memory Device Commands

	First Cycle	Second Cycle	Acceptable While Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	√
Auto Program (True)	10	—	
Auto Program (Dummy)	11	—	
Auto Program (Cache)	15	—	
Auto Block Erase	60	D0	
Status Read (1)	70	—	√
Status Read (2)	71	—	√
ID Read (1)	90	—	
ID Read (2)	91	—	

2.6.1 Read Mode (1) 00H

Read mode (1) is set when a 00H command is issued to the Command register. The three-byte address N, gives the page to be read and the 1-byte pointer M gives the offset into the page. Refer to Figure 6 below for timing details and the block diagram.

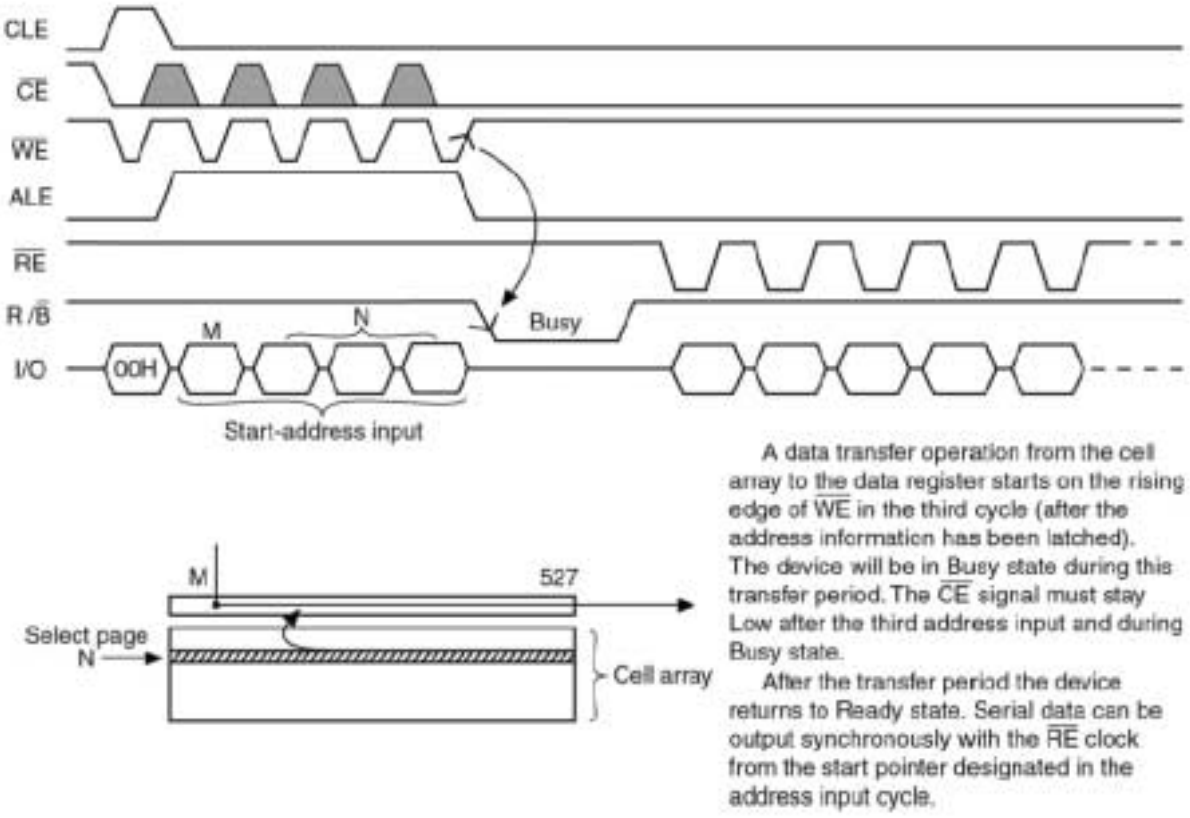

Figure 6. NAND Read Mode (1) Timing

2.6.2 Read Mode (2) 01H

Read mode (2) is set when a 01H command is issued to the Command register. The three-byte address N, gives the page to be read and the 1-byte pointer M gives the offset into the page. In read mode (2), the offset is into the second half of the page, byte 256-511. Refer to Figure 7 below for timing details and the block diagram.

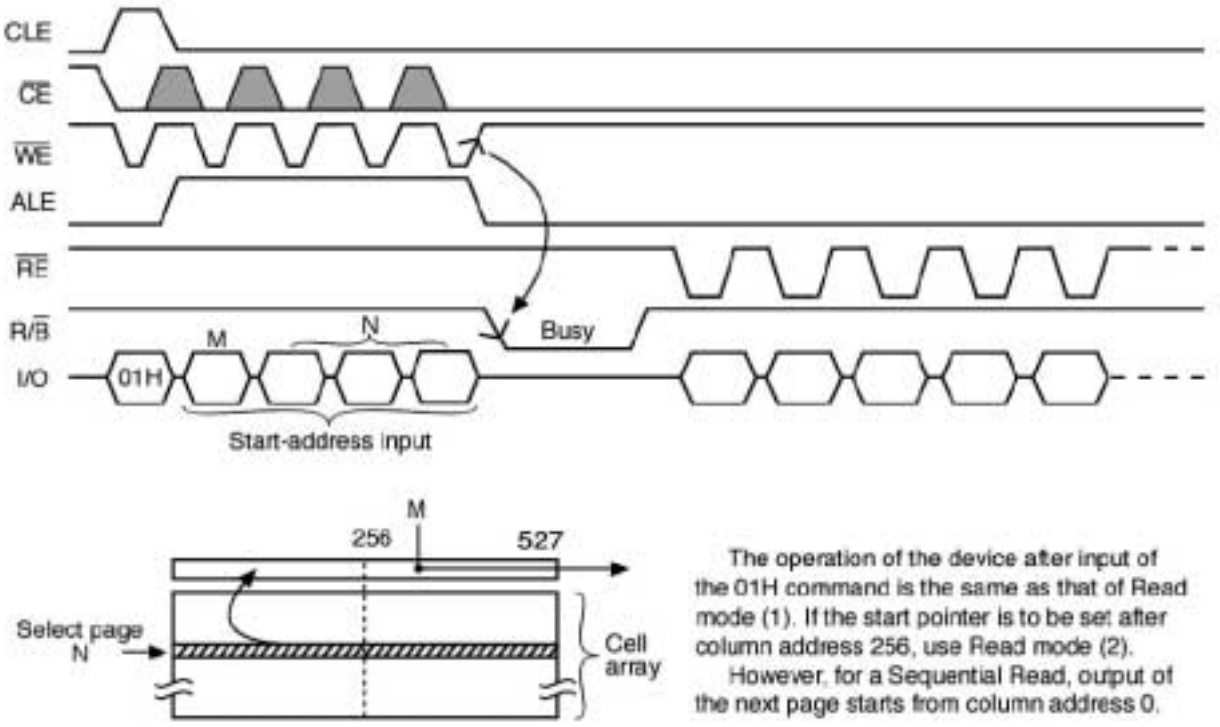

Figure 7. NAND Read Mode (2) Timing

2.6.3 Read Mode (3) 50H

Read mode (3) has the same timing as Read modes (1) and (2) but it is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527. Refer to Figure 8 below for timing details and the block diagram.

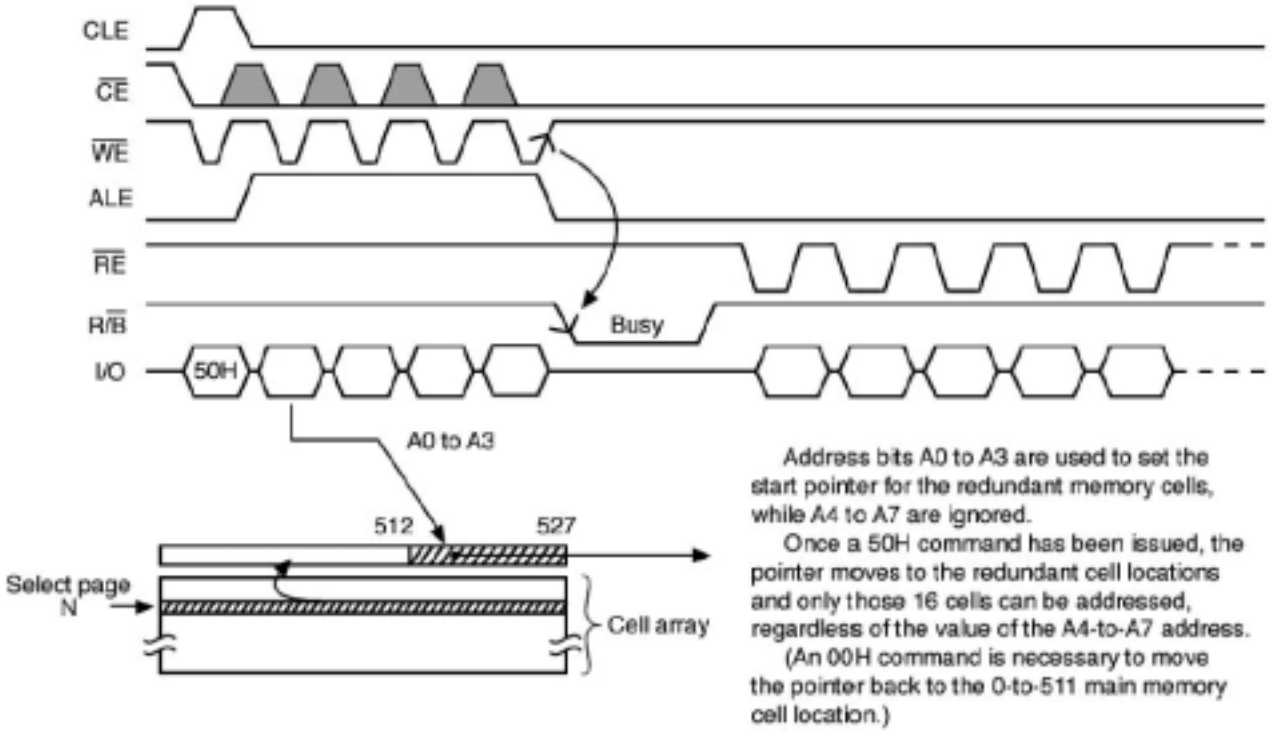

Figure 8. NAND Read Mode (3) Timing

2.6.4 Status Read 70H

The status of NAND memory device can be read using the Status Read command, 70H. The NAND memory device automatically implements the execution and verification of the Program and Erase operations. The Status Read function monitors the Ready/Busy status of the device, determines the result (pass /fail) of a Program or Erase operation, and determines whether the device is in Write Protect mode. The device status is output via the I/O port on the RE clock after issuing the 70H, Status Read, command. The timing diagram for the Status Read command is shown below.

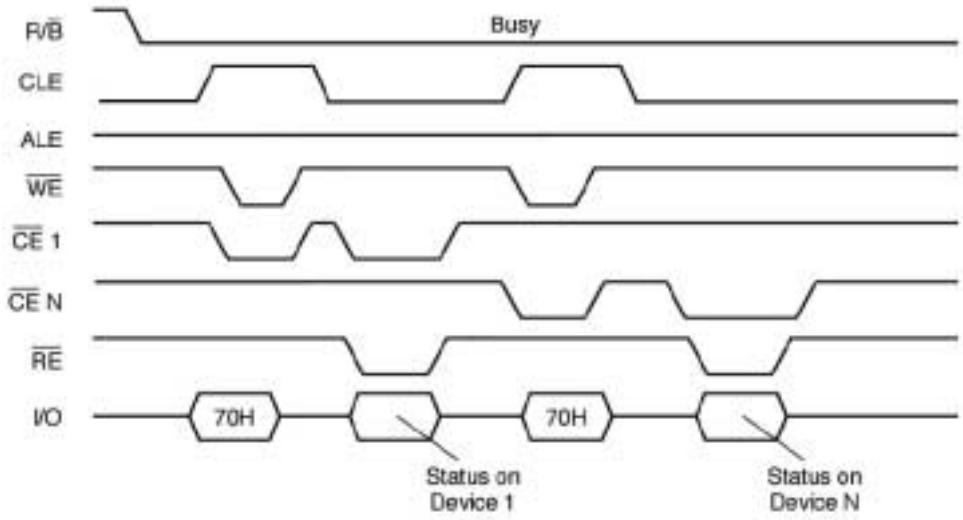

Figure 9. Status Read Timing

2.6.5 Auto Page Program Operation 80H and 10H

The NAND memory device carries out an Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of commands, address and data input is shown below. The data and page address is first sent to the NAND memory device using command 80H and then command 10H is sent to automatically program the data.

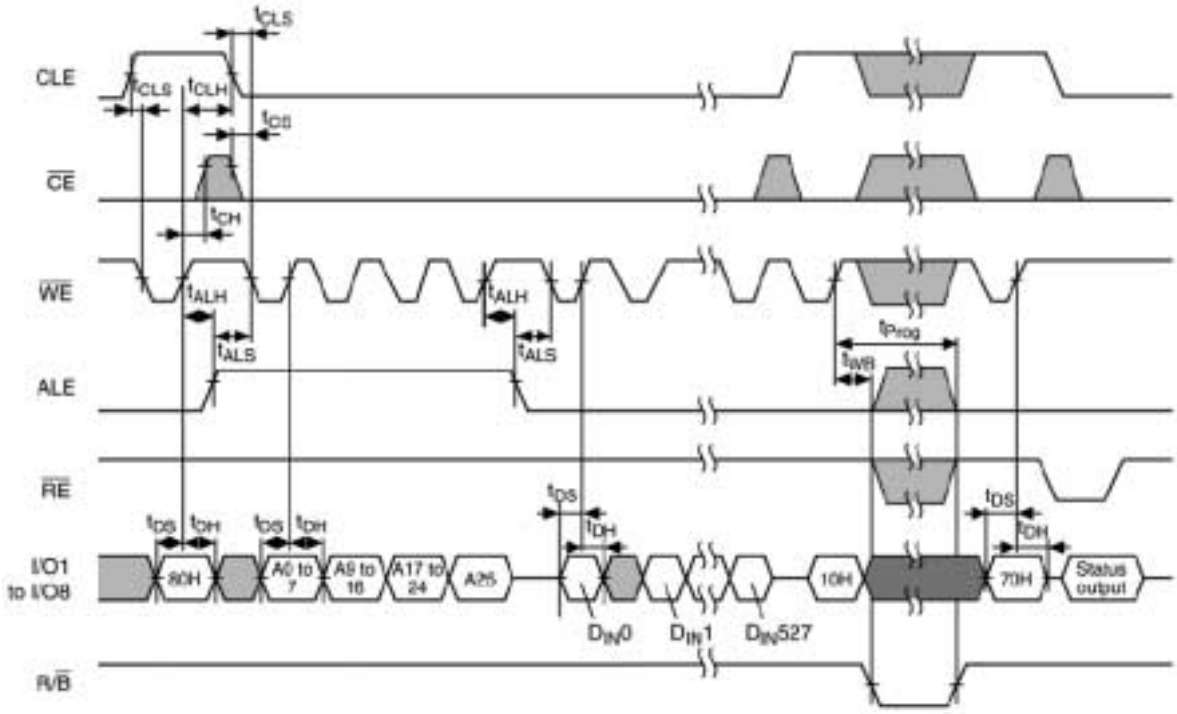

Figure 10. Auto Page Program Operation Timing

2.6.6 Auto Block Erase Operation 60H and D0H

The NAND memory device carries out an Automatic Block Erase operation when it receives a D0H Erase command after the address and data have been input. The sequence of commands for block address input is shown below. The block to be erased is first selected using command 60H and then command D0H is sent to automatically erase the block.

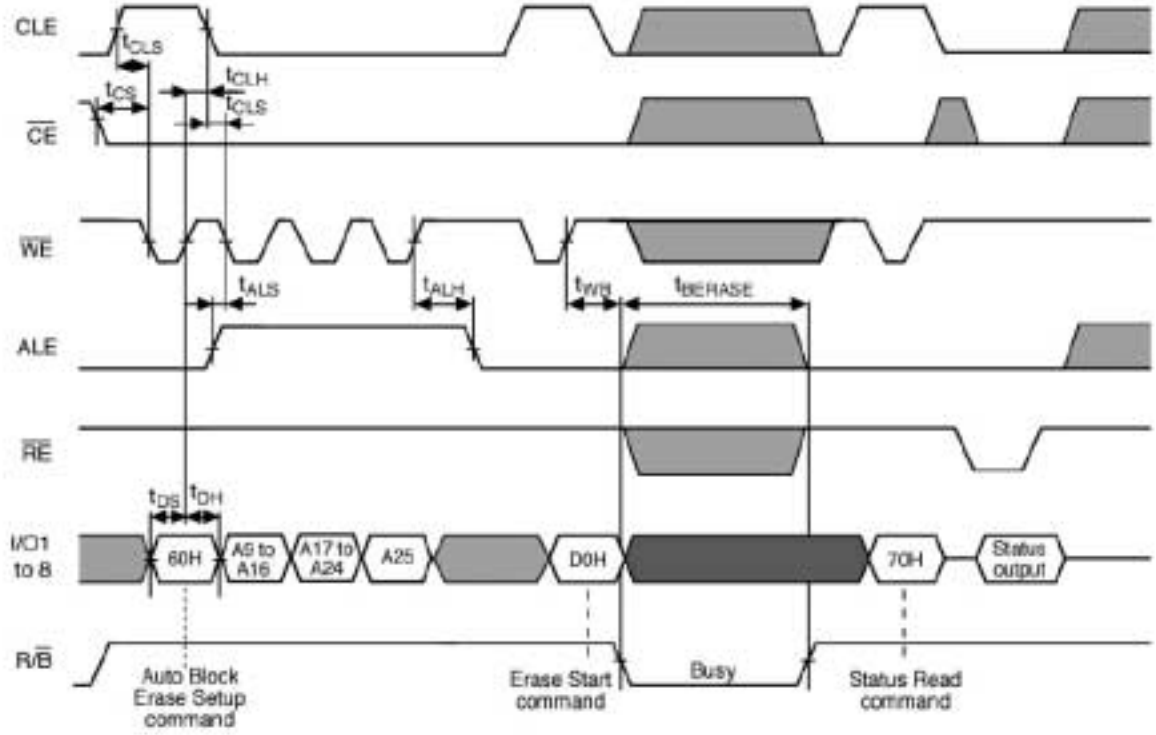

Figure 11. Auto Block Erase Operation Timing

2.6.7 Reset Operation FFH

The Reset command stops all operations. For example, in the case of a Program or Erase operation, the internally generated voltage is discharged to 0 volts, and the device enters the Wait state. After a Reset, the address and data registers are set as follows:

- Address Register: All “0”
- Data Register: All “1”
- Operation Mode: Wait state

The following three diagrams show the response of the NAND memory device when the reset command is issued from different NAND memory device’s operation states.

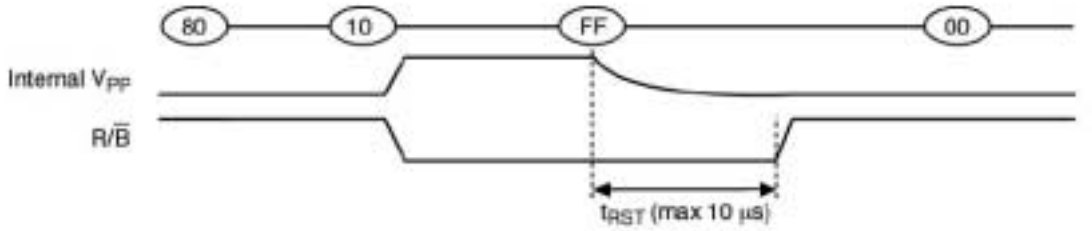

Figure 12. Reset Operation During Programming

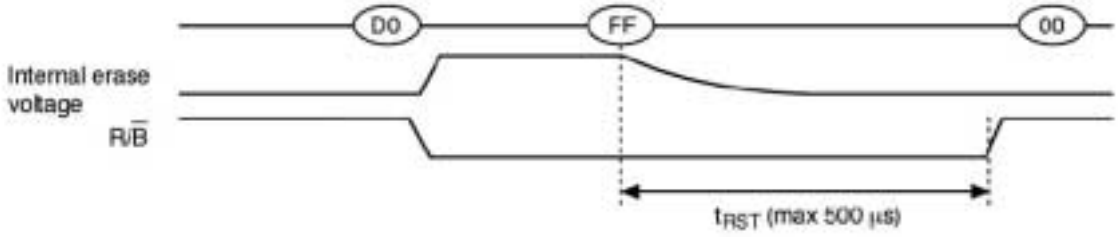

Figure 13. Reset Operation During Erasing

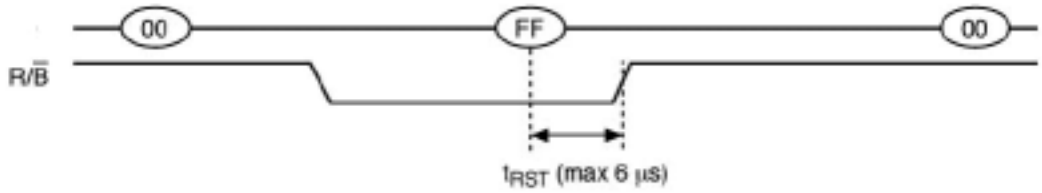

Figure 14. Reset Operation During Reading

2.6.8 ID Read Operation 90H

The NAND memory devices have ID codes that identify the device type and the manufacturer. The ID codes can be read using the following timing diagram in Figure 15:

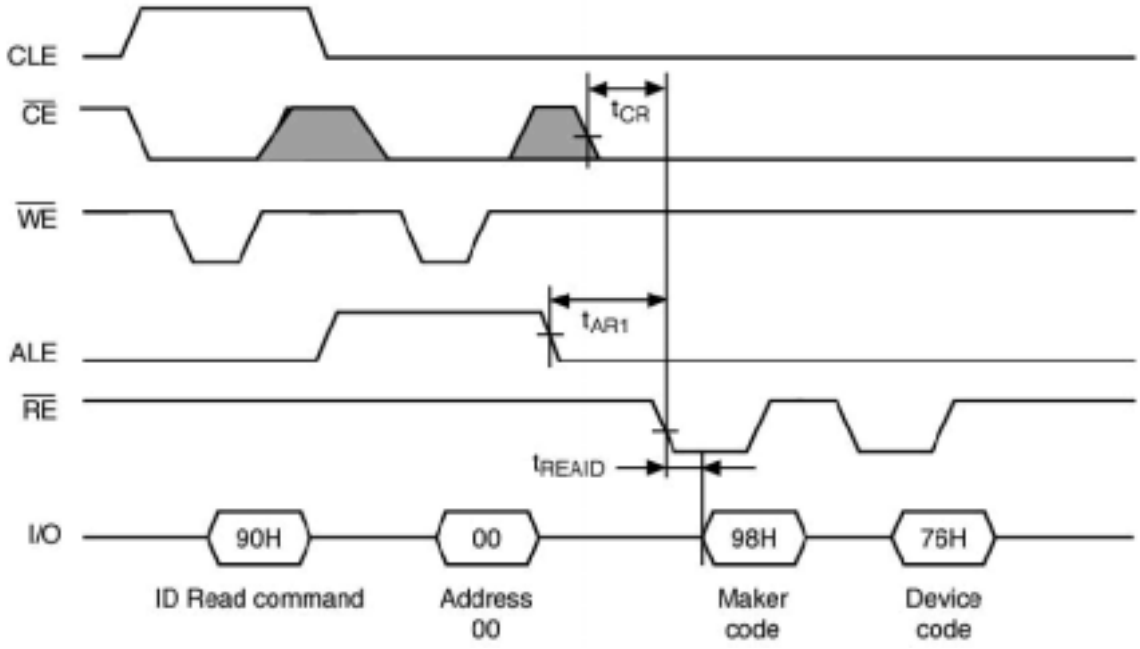

Figure 15. ID Read Operation

3 C55x External Memory Interface (EMIF)

This section describes the external memory interface (EMIF) of the TMS320C55x DSP. The EMIF controls all data transfers between the C55xE and the external memory. The following sections describe how the EMIF is interconnected with other parts of the DSP and with external memory devices. The EMIF registers configure the EMIF and will be described in Section 3.2.

3.1 EMIF Interconnections

Figure 16 illustrates how the EMIF is connected with other parts of the C55x DSP.

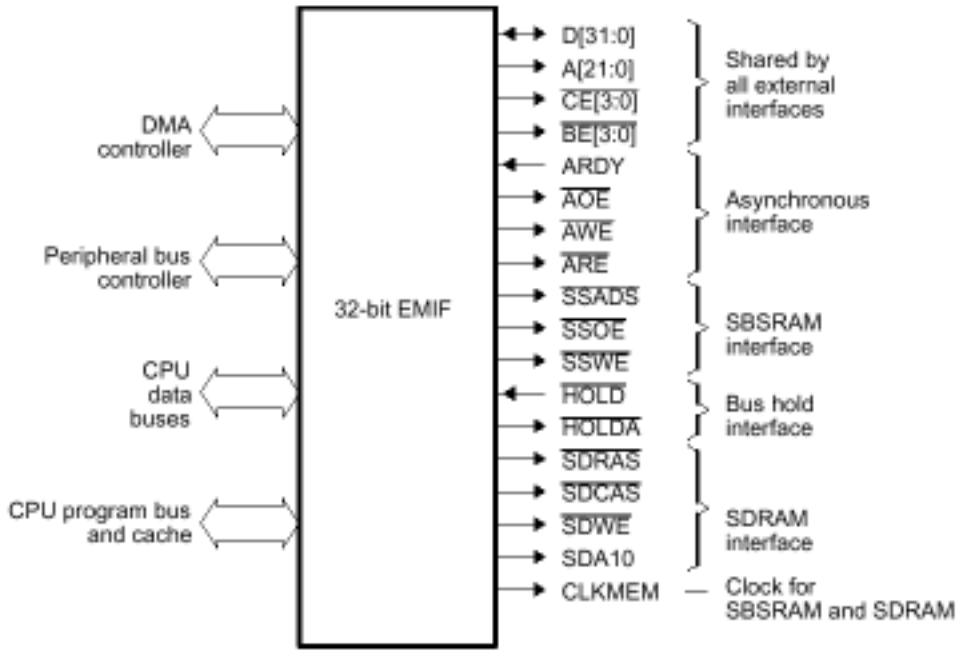

Figure 16. C55x EMIF Interconnections

The EMIF provides a glueless interface to three types of memory devices:

- Asynchronous devices, including ROM, flash memory, and asynchronous SRAM.
- Synchronous burst SRAM (SBSRAM) running at 1/2 or 1 times the CPU clock rate.
- Synchronous DRAM (SDRAM) running at either 1/2 or 1 times the CPU clock rate.

The EMIF supports program access and 8-bit, 16-bit, and 32-bit data accesses. For details on using any of the above three memory types and the description of the EMIF signals, refer to the corresponding sections in the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

3.2 EMIF Registers

The EMIF registers are used to configure the EMIF for accessing the external memory. Table 4, on the following page, lists the EMIF register with a brief description of each register. Different Chip Enable spaces, CE spaces, can be configured to access any of the three types of memory listed in the previous section. The access type (8-bit, 16-bit, or 32-bit) can also be selected using the EMIF registers. For the full details on the EMIF registers, refer to the corresponding section in the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

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Table 4. EMIF Registers

Register(s)	Description
EGCR	EMIF global control register
EMI_RST	EMIF global reset register
EMI_BE	EMIF bus error status register
CE0_1–CEx_1 (x = number of CE spaces – 1)	CE space control registers 1 (one for each CE space)
CE0_2–CEx_2 (x = number of CE spaces – 1)	CE space control registers 2 (one for each CE space)
CE0_3–CEx_3 (x = number of CE spaces – 1)	CE space control registers 3 (one for each CE space)
SDC1	SDRAM control register 1
SDC2	SDRAM control register 2
SDPER	SDRAM period register
SDCNT	SDRAM counter register
INIT	SDRAM initialization register

3.3 NAND Interface Signals

This section describes the external memory interface (EMIF) signals used to interface the C55x to the NAND memory device. For a full discussion on the EMIF, refer to the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).The EMIF consists of a data bus, an address bus, and a set of control signals for accessing off-chip memory and I/O devices. Table 5 lists and describes key signals for the external memory interface.

Table 5. Key External Interface Signals

Signal	Description
A15-A0	Parallel address bus A15 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. These lines are used to address external memory. This bus is used to select the command and address latch signals, CLE and ALE of the NAND memory device.
D15-D0	Parallel data bus D15 (MSB) through D0 (LSB). D7–D0 of this bus is used to transfer data to and from the NAND memory device.
/ARE	Asynchronous memory read enable. This signal is used to select the read enable signal, #RE of the NAND memory device.
/AWE	Asynchronous memory write enable. This signal is used to select the write enable signal, #WE of the NAND memory device.
GPIO0	General purpose I/O. This signal is used to select the NAND memory device's chip enable pin, #CE. It is also used to read the status of the R/#B pin on the NAND memory device.
/RESET	C55x reset signal. This signal is used as an input to the #WP pin of the NAND memory device. During startup, the reset pin is low, this prevents any unwanted writes or erases of the NAND memory device by holding the #WP low.

The NAND memory device is accessed using the asynchronous mode of the EMIF. In this example, a S/W programmable general purpose I/O pin, GPIO, is used for the NAND memory device's chip enable pin instead of one of the EMIF CE signals. Accordingly, the system software must insure that the NAND memory device is not enabled at the same time as other external memory devices on the bus. Alternatively, one of the EMIF CE signals can be dedicated to the NAND memory device's interface.

4 NAND Memory Device Interface to the C55x

This section describes the detailed physical interfaces of the NAND memory device to C55x interface. The schematic diagram below provides a detailed view of this interface. As mentioned before, the NAND memory device can be interfaced to the C55x in many ways, the following schematic diagram illustrates the interface used in this application note.

4.1 Hardware Interface

The NAND memory device can be easily interfaced to the C55x through the EMIF. To set the timing requirements of the EMIF, see the *SanDisk 512Mbit NAND Flash Product Manual* (80-36-00151, Rev. 1.3) for NAND memory device timing details, and the *TMS320C55x DSP Peripheral Reference Guide* (SPRU317) for the EMIF timing registers. The memory space control registers, CEx_1, CEx_2, and CEx_3 together with the EMIF global registers, EGCR, EMI_RST, and EMI_BE control the External Memory Interface, EMIF. The memory space control registers must be set to the timing values required by the NAND memory device's timing specifications. A block diagram view of this interface can be seen in Figure 16, and a detailed schematic diagram view can be seen in Figure 17.

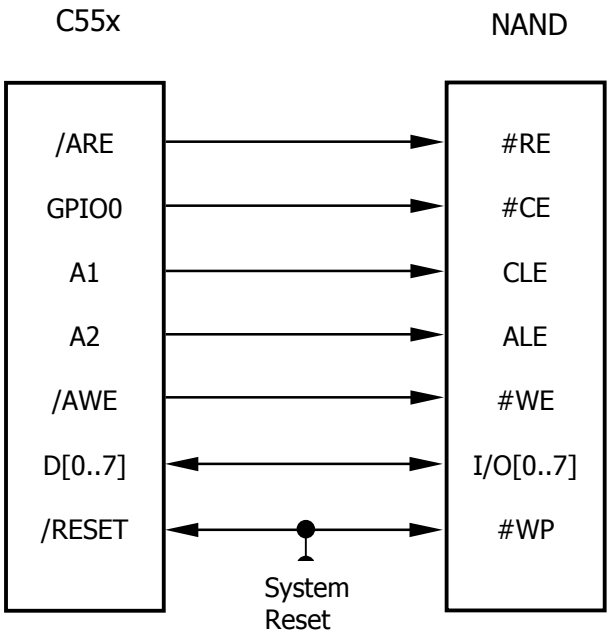

Figure 17. NAND Memory Device Interface to the C55x

Lines A1-A2 from the C55x parallel address bus are connected to the CLE and the ALE command and address latch enable lines on the NAND memory device control bus. The C55x general-purpose I/O line, GP0, is connected to the chip enable signal #CE of the NAND memory device. This configuration allows the C55x to access the command and address latches of the NAND memory device when address lines A1 and A2 are accessed. The C55x parallel data bus is connected to the NAND memory device's I/O bus and allows the C55x to handle address, command, and data transfers between the C55x and the NAND memory device. The C55x /ARE and /AWE signal are connected to the #RE and #WE signals of the NAND memory device to allow the C55x to read and write the NAND memory device's I/O bus. Finally, the C55x reset line, /RESET, is connected to the NAND memory device's #WP to prevent any unwanted writes or erasures of data during startup.

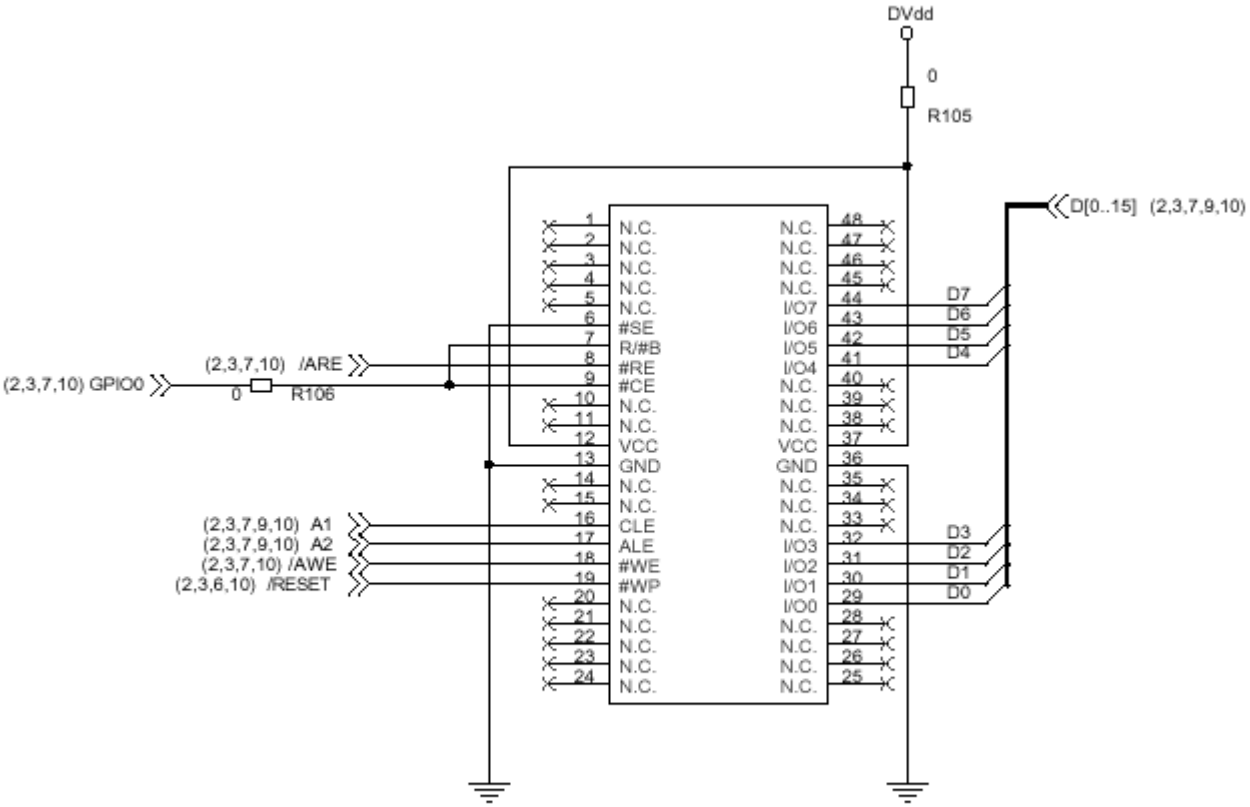

Figure 18. NAND Memory Device Interface to the C55x Schematic

4.2 Software Interface

This section describes the set of routines used to access the NAND memory device. The source code is available electronically from the TI web site.

void NAND_CmdWrite(unsigned int cmd)

Purpose:

To issue NAND commands to the NAND memory device. This routine takes the unsigned command integer and sends it to the NAND memory device.

Variables Modified:

None

Variables Accepted:

cmd

Returns:

None

void NAND_AddrWrite(unsigned long addr, int nbytes)

Purpose:

To write variable number of address data to the NAND memory device. This routine takes the unsigned long address and the number of bytes and shifts it out to the NAND memory device a byte at a time as address data.

Variables Modified:

None

Variables Accepted:

Addr, nbytes

Returns:

Nothing

void NAND_AssertCE()

Purpose:

To select the NAND memory device by asserting the /CE pin low.

Variables Modified:

None

Variables Accepted:

None

Returns:

None

void NAND_DeassertCE()

Purpose:

To de-select the NAND memory device by de-asserting the /CE pin to high.

Variables Modified:

None

Variables Accepted:

None

Returns:

None

int NAND_Busy()

Purpose:

To check the status of the Ready/Busy bit.

Variables Modified:

None

Variables Accepted:

None

Returns:

Status of Busy Bit

unsigned short NAND_ReadID(unsigned int *mfg, unsigned int *device)

Purpose:

To read the NAND device ID. This routine will issue the READ ID command and read the manufacturer and device Ids and return 0 if successful.

Variables Modified:

mfg, device

Variables Accepted:

*mfg, *device

Returns:

0 if successful, ERROR CODE if not successful

unsigned short NAND_ReadPage(unsigned long addr, unsigned char *buf, unsigned long len)

Purpose:

To read a specified page from the NAND memory device. This routine will take an address, character buffer pointer, the length of the buffer, read the page specified by the address, and put the requested amount of bytes in the buffer.

Variables Modified:

buf

Variables Accepted:

Page Address – addr

Byte Count – len

Byte Buffer – *buf

Returns:

0 if successful, ERROR CODE if not successful

unsigned short NAND_WritePage(unsigned long addr, unsigned char *buf, unsigned long len)

Purpose:

To write a specified page to the NAND memory device. This routine will take an address, character buffer pointer, the length of the buffer, and write the requested amount of bytes from the buffer to the page specified by the address.

Variables Modified:

None

Variables Accepted:

Page Address – addr

Byte Count – len

Byte Buffer – *buf

Returns:

0 if successful, ERROR CODE if not successful

unsigned short NAND_EraseBlock(unsigned long addr)

Purpose:

To issue the Erase Block command and erase the specified block.

Variables Modified:

None

Variables Accepted:

Block Address – addr

Returns:

0 if successful, ERROR CODE if not successful

unsigned short NAND_Test()

Purpose:

To test the NAND memory device by writing patterns to the entire device and then reading and verifying the patterns.

Variables Modified:

None

Variables Accepted:

None

Returns:

0 if successful, ERROR CODE if not successful

5 Conclusion

The information provided in this application note illustrated how to interface a C55x DSP to a NAND memory device. A complete reference design, including hardware and software interfaces, was provided. The software consists of a set of file system independent subroutines required to store and retrieve data from the NAND memory device. This software is available electronically from the TI web site.

6 References

1. *SanDisk 512Mbit NAND Flash Product Manual*. Lit. No. 80-36-00151 Rev. 1.3 6/01 http://www.sandisk.com
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3. *TMS320C55x DSP Peripherals Reference Guide* (SPRU317)

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