

## **H.263 Loopback on the DM642 EVM**

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*Video and Imaging Systems*

### **ABSTRACT**

The software demonstrates the D1 H263 encoder and decoder on the DM642 Evaluation Module (EVM). The demonstration encodes the captured frames and then decodes the generated H263 bit-stream to display the decoded frames.

The demonstration uses:

- H263 encoder library optimized for a DM642 EVM
- H263 decoder library optimized for a DM642 EVM
- H263 encoder and decoder library implemented using XDAIS interfaces
- Sample integration of the H263 encoder and decoder library using RF-5 framework

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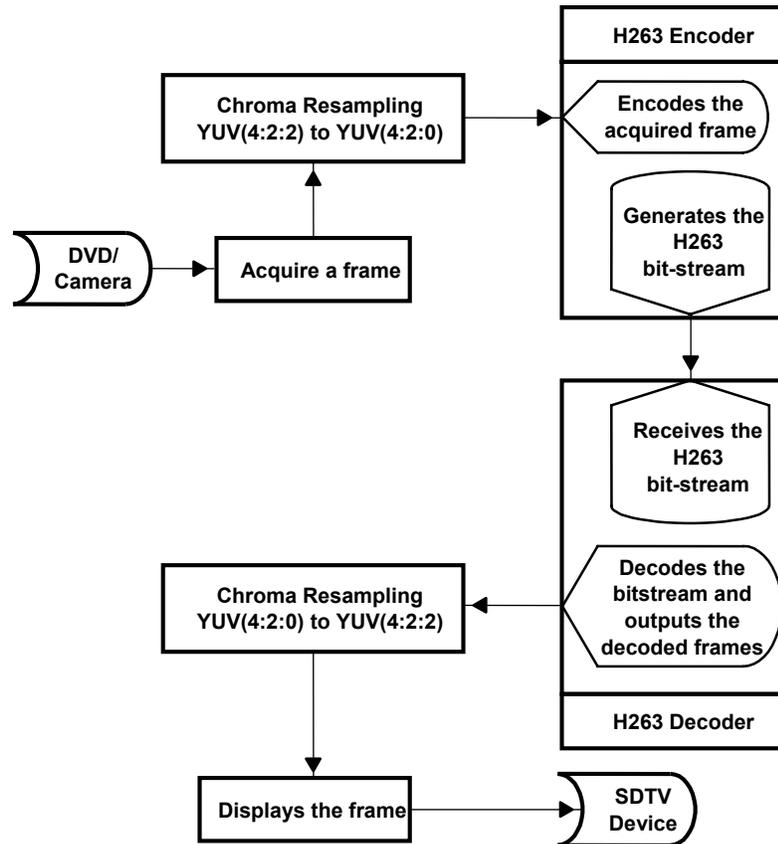
### **Contents**

<b>Software Architecture/Data Flow</b> .....	<b>2</b>
Data Flow Diagram for the Demonstration .....	2
Framework Flowchart.....	3
<b>System Requirements/Configuration</b> .....	<b>5</b>
Software Requirements.....	5
Hardware Requirements .....	5
<b>Hardware Setup</b> .....	<b>6</b>
<b>Demonstration Execution</b> .....	<b>6</b>
<b>Demonstration Code and Build Procedure</b> .....	<b>7</b>
Build Procedure.....	8
<b>Known Bugs and Constraints</b> .....	<b>8</b>

### **Figures**

<b>Figure 1. Data Flow Diagram</b> .....	<b>2</b>
<b>Figure 2. Framework Flowchart</b> .....	<b>4</b>
<b>Figure 3. Hardware Setup</b> .....	<b>6</b>
<b>Figure 4. Directory Structure</b> .....	<b>7</b>

## Software Architecture/Data Flow



**Figure 1. Data Flow Diagram**

### Data Flow Diagram for the Demonstration

The data flow in the demonstration follows this sequence:

1. A frame is captured from the input source (DVD/camera), and the acquired frame data, in YUV 4:2:2 format, is resampled to YUV 4:2:0 format.
2. The frame is fed to the H263 encoder library.
3. The H263 encoder encodes the input frame.
4. The H263 encoder outputs the coded bit-stream.
5. The generated H263 bit-stream is passed to the H263 decoder module.
6. The H263 decoder module decodes the H263 bit-stream and outputs the decoded frames.
7. The decoded frames received from the H263 decoder module are in YUV 4:2:0 format and are resampled to YUV 4:2:2 format.

8. The frame is then displayed on the output device (SDTV).

### Framework Flowchart

The demonstration uses RF-5 framework to integrate the H263 encoder and decoder library. It uses a three-task model. Before coming to the DSP BIOS™ task scheduler, the demonstration code initializes various modules used in the system. These include:

- Board and processor
  - The system performs DSP BIOS™ initialization and CSL initialization.
  - The L2 cache mode is set to 64K cache.
  - EMIFA CE0 and EMIF CE1 space are enabled for caching.
  - The DMA priority queue lengths are set to maximum.
  - Priority for L2 request is set as high.
- RF- 5 modules
  - The system initializes the channel module of RF-5.
  - The system initializes the ICC and SCOM modules of RF-5 required for intercell communication and messaging.
  - Channel setup is performed with the internal, external, and scratch heap buffers.
- Capture and display channels
  - An instance of capture channel is created and started.
  - An instance of display channel is created and started.
- Algorithm instances
  - The H263 encoder cell is created and registered in the channel.
  - The H263 decoder cell is created and registered in the channel.
  - The channel is opened, which leads to creation of instances of the encoder and decoder cells.

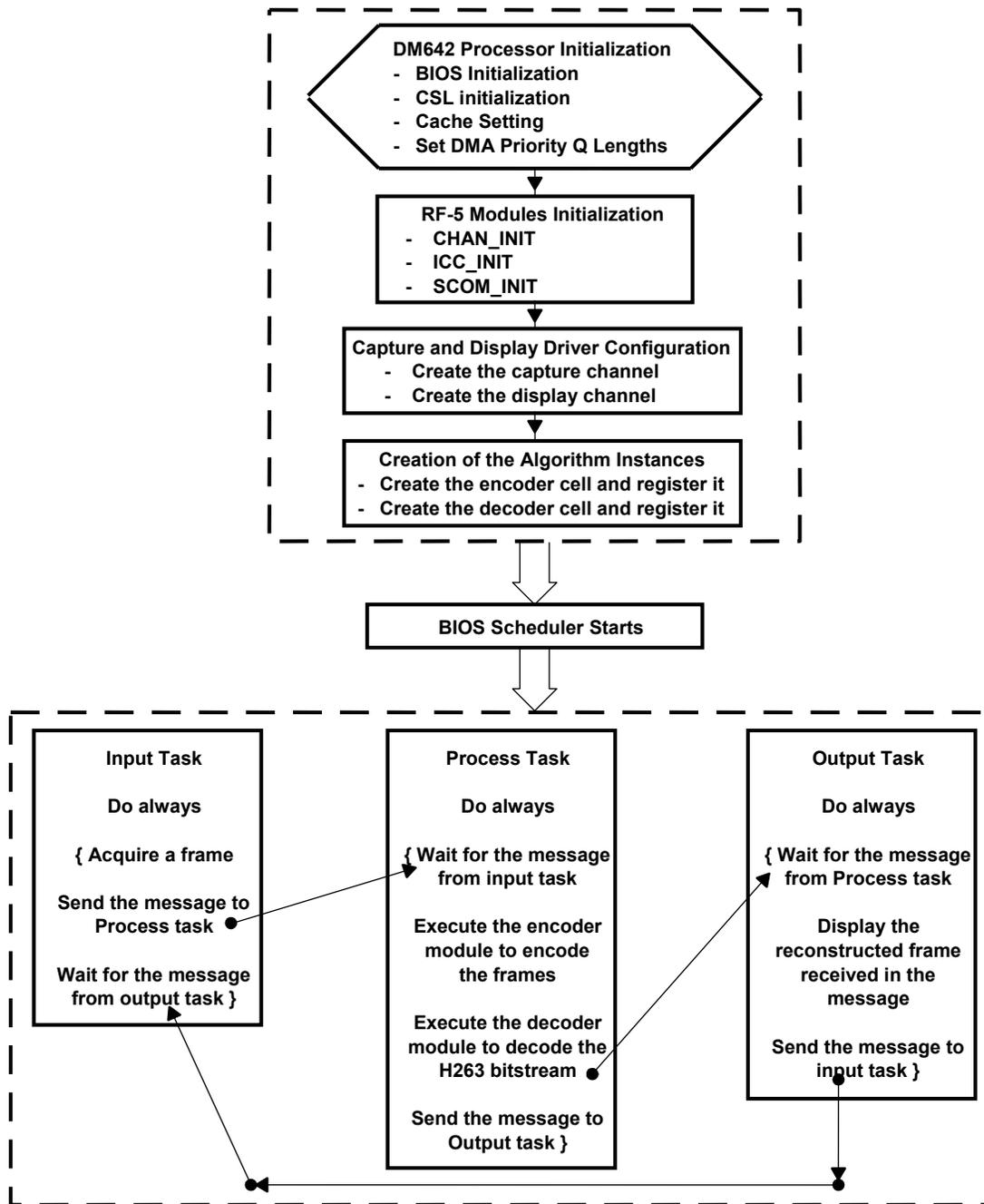


Figure 2. Framework Flowchart

After these initializations, the system enters the three-task system managed by the DSP BIOS™ scheduler. These three tasks use the SCOM module of RF-5 to communicate with each other:

- Input task

The input task is responsible for acquiring the frames from the NTSC input device. It uses FVID\_exchange calls provided by the driver to acquire a frame. The acquired frame is in YUV 4:2:2 format and is resampled to YUV 4:2:0. It sends the message to the process task

with the frame pointer embedded in the message. The task then waits for the message from output task to continue.

- **Process task**

The process task is responsible for encoding the frame, passing the bitstream to the decoder module, decoding the frame, and then passing in on to the output task. The process task achieves the loopback by executing the RF-5 channel. The RF-5 channel has both encoder and decoder cells registered in it. The ICC module manages the passing of the bitstream generated by the encoder cell to the decoder cell.

The task waits until it receives the message, with input frame, from the input task. The RF-5 channel in the demonstration code consists of a H.263 encoder cell and a H.263 decoder cell. During the channel execution, first the H.263 encoder cell executes and generates the bitstream. The generated bitstream is passed to the H.263 decoder cell and then the decoder cell executes to produce the decoded frames. It sends a message to the output task, with the decoded frame pointers embedded in the message. The task then waits for the message from the input task to continue further.

- **Output task**

The output task is responsible for displaying the frames on the NTSC output device. It uses FVID\_exchange calls provided by the driver to display a frame on the NTSC output device. The acquired frame is in YUV 4:2:0 format and is resampled to YUV 4:2:2 format. It then sends a message to the input task to continue. The task then waits for the message from the process task to continue.

## **System Requirements/Configuration**

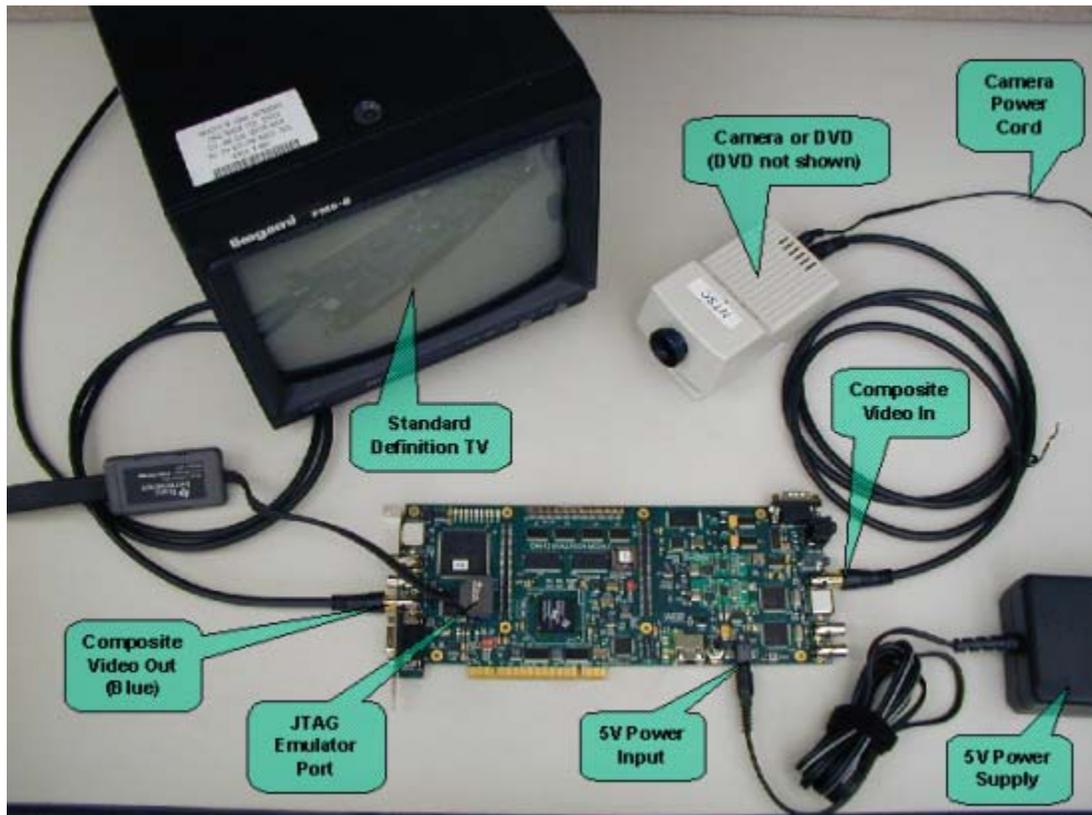
### **Software Requirements**

- Microsoft Windows NT (SP6)/Microsoft Windows 2000 (SP1 and SP2)
- Code Composer Studio™ Integrated Development Environment (IDE) version 2.20.18
- Driver software (DDK 1.1)

### **Hardware Requirements**

- Pentium machines with 450 MHz, 64MB RAM (minimum)
- DM642 EVM
- NTSC TV for display purposes
- Camera/DVD for NTSC capture purposes
- XDS 510/560 emulator

## Hardware Setup



**Figure 3. Hardware Setup**

To run the demonstration, the hardware must be set up properly, as shown.

- The XDS510/560 emulator must be connected to JTAG pins to download the demonstration code to the board and control it from Code Composer Studio™ IDE.
- The input video port (for composite video) must be connected to the NTSC input source (DVD/ camera) using RCA cable.
- The output video port (for composite video) must be connected to the NTSC output device (SDTV) using RCA cable.
- The DM642 EVM must be connected to the appropriate power source.

## Demonstration Execution

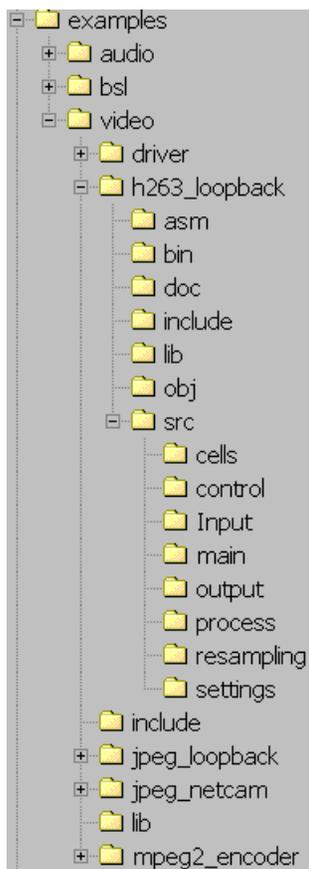
To run the demonstration:

1. Set up the hardware as described in *Hardware Setup*.
2. Power up the DM642 EVM board.
3. Start Code Composer Studio™ IDE version 2.20.18.

4. Check the color bar on the output device.
5. Go to the bin folder, as shown in Figure 4, and load .out.
6. Once the program is loaded, go to the Debug menu and press the Run option (F5).
7. On the output screen, watch the output frames from the H263 encoder/decoder loopback, with the TI logo at the top-right corner of the frames.
8. The target bit rate for the encoder can be changed on-the-fly using two global variables: bitRateChanged and bitRateTarget. To do so, add these variables to the watch window. Change the value of bitRateTarget to the desired bit rate (in Kbps), and then set the bitRateChanged to 1. The changes must be made in this order.

## Demonstration Code and Build Procedure

The demonstration code for H.263 loopback is located in evmdm642\examples\video\h263\_loopback directory.



**Figure 4. Directory Structure**

## Build Procedure

1. Start Code Composer Studio™ IDE version 2.20.18
2. Open H263 loopback project (h263loopback\_dm642.pjt) in the folder called examples\video\H263\_loopback.
3. Go to Project->Build Options->Compiler->Preprocessor and define the symbols as required for appropriate demonstration setup.

Default options: The following must always be defined for proper compilation of the demonstration:

`_NTSC;CHIP_DM642`

4. If the C\_DIR is not defined, or the DDK package has been installed outside the Code Composer Studio™ IDE folder, modify the include paths to point to the appropriate <ccs install dir>\ti\... paths in project build options. If the C\_DIR is defined properly, there is no need to modify the include paths.
5. Build the project and load the executable h263loopback\_dm642.out build in the examples\video\H263\_loopback \bin directory.
6. Before running the executable, make sure the input (camera/DVD) and output (SDTV) are connected correctly. For all input purposes and for SDTV output purpose, RCA cables must be used.
7. Press F5 to watch the output frames from the H263 encoder/decoder loopback, with the TI logo on the top-right corner of the frames.

## Known Bugs and Constraints

The H263 libraries in the project have been compiled to work only for the baseline profile.

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