TMS320C6416 Hardware Designer's Resource Guide

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ABSTRACT

The TMS320C6416 DSP Hardware Designer's Resource Guide is organized by development flow and functional areas to make your design effort as seamless as possible. Topics covered include Getting Started, Board Design, System Testing, and Checklists to aid in your initial design and debug efforts. Each section includes pointers to valuable information including technical documentation, models, symbols, and reference designs for use in each phase of design. Particular attention is given to peripheral interfacing and system level design concerns.

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1 Getting Started

1.1 Registering on my.TI

my.TI is a customizable area within the Texas Instruments web site. By registering on my.TI, you can receive the following benefits:

- Quick Reference to information you select as part of your profile.
- Email alerts that inform you of updates to products, technical documentation, and errata.
- The my.TI newsletter providing information on the latest innovations and product releases.

To register on my.TI for updates related to the this device:

1. Go to the device product folder.
2. Select the link called “ADD To my.TI” in the upper right hand corner, and follow the on-screen instructions.
3. Select Customize my.TI to specify what you would like to receive notification about.

The following is a link to the product folder.

TMS320C6416 DSP product folder.

1.2 Training and Support

Texas Instruments offers a variety of training options tailored for your specific needs and requirements. Options include on-line training, webcasts, seminars, single and multi-day workshops, and conferences. For more information about training, visit Texas Instruments Training Home. For assistance with technical questions regarding TI Semiconductor products and services, you can access the Semiconductor Technical Support KnowledgeBase .

1.3 Technical Documentation

1.3.1 Where to Start

The key area for obtaining documentation for this device is the product folder. When getting started, it is of great importance to have the latest data sheet and silicon errata. Listed below are links to this key information:

- TMS320C6416 DSP product folder
- TMS320C6416 Data Sheet (SPRS146)
- TMS320C6416 Errata (SPRZ011)
- How to Begin Development with the TMS320C6416 (SPRA718)

1.3.2 Using TI Literature Numbers

All TI documentation is assigned a literature number. This number can be used to search for the document on the Web. Technical documentation revisions are indicated by the alpha character at the end of the literature number on the title page, and in the file name.

Use the literature number (without the trailing alpha character) to search the TI website for the document. For example, if a data manual has a literature number of SPRS205B, the ”B” indicates the revision of the document. If the document has no trailing alpha character, it is the original version of the document. When searching for this document on the TI web site, you can simply enter ”SPRS205” as the search keyword.

1.3.3 Peripheral Reference Guides

Each peripheral has a reference guide that provides beneficial information for completing a design. Each peripheral and its respective reference guide is listed here. There are two categories. The first category contains peripherals which connect directly to external devices. The second category lists the internal peripherals.

Peripherals that connect directly to external devices:

- TMS320C6000 DSP External Memory Interface (EMIF) Reference Guide (SPRU266)
- TMS320C6000 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide (SPRU580)
- TMS320C64x DSP Universal Test and Operations PHY Interface for ATM (UTOPIA) Reference Guide (SPRU583)
- TMS320C6000 DSP General-Purpose Input/Output (GPIO) Reference Guide (SPRU584)
- TMS320C6000 DSP Peripheral Component Interconnect (PCI) Reference Guide (SPRU581)
- TMS320C6000 DSP Host-Port Interface (HPI) Reference Guide (SPRU578)

Internal peripherals:

- TMS320C6000 DSP Interrupt Selector Reference Guide (SPRU646)
- TMS320C64x DSP Turbo-Decoder Coprocessor (TCP) Reference Guide (SPRU534)
- TMS320C64x DSP Viterbi-Decoder Coprocessor (VCP) Reference Guide (SPRU533)
- TMS320C6000 DSP Power-Down Logic and Modes Reference Guide (SPRU728)
- TMS320C6000 DSP Enhanced Direct Memory Access (EDMA) Controller Reference Guide (SPRU234)
- TMS320C64x DSP Two-Level Internal Memory Reference Guide (SPRU610)
- TMS320C6000 DSP 32-bit Timer Reference Guide (SPRU582)

1.3.4 Application Reports

Application reports are documents written to describe functionality and usability for a specific application or design. Listed below are application reports that provide useful information about peripherals.

External Memory Interface (EMIF):

- *TMS320C6000 EMIF:Overview of Support of High Performance Memory Technology (SPRA631)*
- *TMS320C6000 EMIF to USB Interfacing Using Cypress EZ-USB SX2 (SPRAA13)*
- *TMS320C6000 EMIF-to-External SDRAM Interface (SPRA433)*
- *TMS320C6000 EMIF to TMS320C6000 Host Port Interface (SPRA536)*
- *TMS320C6000 EMIF to External Flash Memory (SPRA568)*
- *Interfacing the TMS320C6000 EMIF to a PCI Bus Using the AMCC S5933 PCI Controller (SPRA479)*
- *TMS320C6000 EMIF to External Asynchronous SRAM Interface (SPRA542)*
- *TMS320C6000 EMIF to External FIFO Interface (SPRA543)*
- *TMS320C6000 EMIF to External SBSRAM Interface (SPRA533)*

Multichannel Buffered Serial Port (McBSP):

- *TMS320C6415/6416: Using PCI EEPROM Interface and McBSP2 in a Single System (SPRA814)*
- *TMS320C6000 McBSP Interface to an ST-BUS Device (SPRA511)*
- *Using the TMS320C6000 McBSP as a High Speed Communication Port (SPRA455)*
- *TMS320C6000 McBSP to Voice Band Audio Processor (VBAP) Interface (SPRA489)*
- *TMS320C6000 McBSP: AC'97 Codec Interface (TLV320AIC27) (SPRA528)*
- *TMS320C6000 McBSP Interface to SPI ROM (SPRA487)*
- *TMS320C6000 McBSP: IOM-2 Interface (SPRA569)*
- *TMS320C6000 McBSP: UART (SPRA633)*
- *TMS320C6000 McBSP as a TDM Highway (SPRA491)*
- *TMS320C6000 Multichannel Communications System Interface (SPRA637)*
- *TMS320C6000 McBSP: I^2S Interface (SPRA595)*

Host Port Interface (HPI):

- *TMS320C6000 Host Port to MC68360 Interface (SPRA545)*
- *TMS320C6000 Host Port to the i80960 Microprocessors Interface (SPRA541)*
- *TMS320C6000 Host Port to MPC860 Interface (SPRA546)*

Peripheral Component Interconnect (PCI):

- *TMS320C6415/6416: Using PCI EEPROM Interface and McBSP2 in a Single System (SPRA814)*
- *TMS320C64x DSP Peripheral Component Interconnect (PCI) Performance (SPRA965)*

2 Board Design and Layout

2.1 High−Speed DSP Systems Design Reference Guide

Today's digital signal processors (DSPs) are typically run at a 1GHz internal clock rate while transmit and receive signals to and from external devices operate at rates higher than 200MHz. These fast switching signals generate a considerable amount of noise and radiation, which degrades system performance and creates electromagnetic interference (EMI) problems that make it difficult to pass tests required to obtain certification from the Federal Communication Commission (FCC). Good high−speed system design requires robust power sources with low switching noise under dynamic loading conditions, minimum crosstalk between high−speed signal traces, high− and low−frequency decoupling techniques, and good signal integrity with minimum transmission line effects. This document provides recommendations for meeting the many challenges of high−speed DSP system design.

For more information, refer to High−Speed DSP Systems Design Reference Guide (SPRU889).

2.2 Reference Design

This reference design is intended to be used as a design aid for custom systems. The primary goal is to demonstrate proper printed circuit board (PCB) construction for DSP use and proper interfacing of the DSP to common external peripherals. The following is a link to this reference design.

TMS320C64x DSP Reference Design (SPRAA21)

2.3 Schematics

This section includes ORCAD symbols that should help in schematic generation. The method that we have chosen to provide the ORCAD symbols is a multi-section package further defined as a heterogeneous package. That is to say that the logical parts in the package have different graphics, numbers of pins, or properties. In the case of the TMS320C6416 DSP, we have created an ORCAD library that contains 14 parts. This allows the schematic designer to easily connect the various parts on separate schematic pages and yet retain the same reference designator for the part across all schematic pages. The list below describes which pins are assigned to a part.

Several peripherals use multiplexed pins. In cases in which pins are shared, one peripheral will be enabled and the other will be disabled. Please refer to the data sheet for more information concerning multiplexed pins.

You can find the ORCAD symbols here:

TMS320C6416 Orcad Symbol (SPRC138)

2.4 Signal Integrity and Timing Considerations

Today's high-speed interfaces require strict timings and accurate system design. To achieve the necessary timings for a given system, input/output buffer information specification (IBIS) models must be used. These models accurately represent the device drivers under various process conditions. Board characteristics, such as impedance, loading, length, number of nodes, etc., affect how the device driver behaves. The following application reports discuss how to use IBIS models on this device.

- TMS320C6416 IBIS model (IBIS Model)
- Using IBIS Models for Timing Analysis (SPRA839)

2.5 Board Layout

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has recently been increasing. This increase has led to more stringent requirements for the electromagnetic properties of equipment. Two property aspects are of interest: the ability of a circuit to generate the lowest (or zero) interference, and the immunity of a circuit to the effects of the electromagnetic energy it is subjected to. The effects on electronic circuits and systems is well documented, but little attention has been paid to circuit behavior and the interference it generates. The following link discusses the important criteria that determine the EMC of a circuit.

Printed-Circuit Board Layout for Improved Electromagnetic Compatibility (SDYA011).

2.6 Power Supply and Sequencing Considerations

Texas Instruments offers several Power Management Products for the TMS320C6416 DSP. In the Power Management selection guide below, refer to the TMS320C6000 section for more information on available solutions. For a complete list of product offerings, visit the power.ti.com website. The following applications reports are helpful in choosing the right power solution:

- *Power Management Selection Guide (SLVT145)*
- *Providing a DSP Power Solution from a 5-V or 3.3-V Only System (SLVA069)*
- *Power Supply Sequencing Solutions for Dual Supply Voltage DSPs (SLVA073)*
- *Dual Output Power Supply Sequencing for High Performance Processors (SLVA117)*

2.7 Power/Thermal Management Considerations

Circuit designers must always consider the effects of thermal stack up – the cascaded effect of the transfer of heat from a device die to the surrounding package. The flow of heat from the device die to ambient must be sufficient to maintain an acceptably low junction temperature, and maximize device reliability. The thermal resistance characteristics for this device are documented in the data sheet. The following application reports discuss thermal analysis, heat sink selection, and power consumption.

- *TMS320C6x Thermal Design Considerations (SPRA432)*
- *TMS320C6414/5/6 Power Consumption Summary (SPRA811)*

2.8 Boot Mode Configurations

The TMS320C6416 has three types of boot modes:

- Host boot
- EMIF boot (using default ROM timings)
- No boot

At /RESET the DSP uses EMIFB address pins 18 and 19 for selecting one of the boot modes. Boot mode bit 0 maps to EMIFB address pin 18 and boot mode bit 1 maps to EMIFB address pin 19. To select the boot modes use the following table.

Boot Mode BEA[19:18]	Boot Process
00	None
01	Host Boot
10	EMIFB 8-bit ROM with default timings
11	Reserved

For more information, please refer to the data sheet and the following application reports.

- *TMS320C6000 Tools: Vector Table and Boot ROM Creation (SPRA544)*
- *TMS320C6000 Boot Mode and Emulation Reset (SPRA978)*

2.9 Joint Test Access Group (JTAG) Interface

DSP devices have a JTAG interface that allows for emulation hardware and software to communicate with the DSP. The JTAG port also supports boundary scan testability. Listed below are links to this key information.

- *TMS320C6000 DSP Designing for JTAG Emulation Reference Guide (SPRU641)*
- *TMS320C6000 Board Design: Considerations for Debug (SPRA523)*
- *TMS320C6000 Board Design for JTAG (SPRA584)*
- *60-pin Emulation Header Technical Reference (SPRU655)*

2.10 Board Manufacturing

When designing with a high−density BGA package, it is important to be aware of different techniques that aid in the quality of the manufacture. The following is a link to this key information.
Flip Chip Ball Grid Array Package Reference Guide (SPRU811).

3 System Test

3.1 Boundary Scan Description Language (BSDL) Model(s)

BSDL models can be used to facilitate board level testing. Currently we have two different versions of the BSDL, one model for revision 1.1 silicon and another model for revision 2.0 silicon. You can find BSDL models for the TMS320C6416 DSP here:

- *TMS320C6416 silicon revision 2.0 BSDL Model (SPRM138)*
- *TMS320C6416 silicon revision 1.1 BSDL Model (SPRM043)*

4 Checklists

4.1 Design Checklist

The Design Checklist was put together by Texas Instruments application and field support staff as a guide to considerations made during the design phase of development. Use this check list to keep track of considerations you make during the design phase of development.

☐	Check the data sheet and errata for the most up to date information.
☐	Are decoupling capacitors placed on the board near the DSP? Voltages from traces on a printed circuit board can couple to each other in places where it is not desired, (like power supply planes). To decouple the traces, we add capacitors to absorb some of the voltage and help reduce this effect. For more information on how to correctly place decoupling caps, see the data sheet section for power-supply decoupling.
☐	Are there provisions for power sequence? To operate properly, the DSP needs to be powered up in the correct sequence. Check the sequencing for power, according to data sheet specifications.
☐	Voltage levels changes? The board should be able to accommodate some voltage level changes. It can be useful to accommodate some changes by simply changing a resistor.
☐	Are the CLKMODEx pins configured correctly? In addition to checking the CLKMODE[1:0] pins to see if they are set up to generate the correct frequency, the CLKOUT4/6 pins should be checked with an oscilloscope. To do this, you must clock EMIFA. If the CLKOUT4/6 signal is correct, this verifies lock of the PLL, in addition to the correct frequency of operation for your DSP. If the CLKOUT4/6 signal is not correct, check that the PLL and the CLKMODE pins are con figured correctly. Does the PLL have the correct circuitry around it, following the data sheet recommenda tions?
☐	Are there provisions for changing the clock during debug time? It can be very helpful to set up a jumper on your board to change the clock frequency. This can allow you to detect whether or not problems are related to the high clock rate.

☐	Reset circuitry? For debugging it is important to be able to reset the DSP when/if it gets into an unstable state. To perform this, one of the easiest things to do is to have a reset button on the board itself. For information on proper reset circuitry, see the *Reset Circuit for the TMS320C6000 DSP* (SPRA431) link listed below. Having a reset supervisor on board enables you to do things like monitor the supply rails for sags in power. The TPS3110 class of devices is the most commonly used reset supervisors from TI. For more information, see the data sheet. *Reset Circuit for the TMS320C6000 DSP (SPRA431)*
☐	Are boot mode pins configured correctly? The three boot modes for the C6000 devices are: no boot, boot over the HPI, or boot from a ROM device located at Chip Enable Space 1. Check the definition for these modes in the Boot loading Guide section of this document and choose the correct configuration you need. It is very useful to include the ability to choose an alternate boot configuration. Use unpopulated resistor pads to allow the choice of different boot modes.
☐	Are the AARDY/BARDY pins used? If using asynchronous RAM, make sure AARDY (EMIFA) and BARDY (EMIFB) are being used appropriately. If NOT using asynchronous RAM, the pins are pulled up internally.
☐	Is the HOLD/HOLDA method being used? If using asynchronous RAM, make sure $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ are used properly. If NOT using asynchro nous RAM, make sure the NOHOLD bit in GBLCTL register is set to 0.
☐	Are the HDS/HAS signals correctly configured to access the DSP? If using the HPI, then you have a choice of configurations. Examples of timing diagrams for when $\overline{\text{HAS}}$ is used or unused (tied high) are in *TMS320C6000 DSP Peripherals Overview Reference Guide* (SPRU190). Also, there is a choice on how to assert $\overline{\text{HSTROBE}}$ using both, one, or none of the $\overline{\text{HDS1/2}}$ in combination with $\overline{\text{HCS}}$. The gate logic for these pins should be checked in the aforementioned HPI reference guide as well.

☐	Is the emulation configured properly? Check to make sure EMU[1:0] pins are connected according to your needs. The JTAG port can function in one of two ways, emulation mode or boundary scan mode. The table below documents the selection based on EMU[1:0] pins. **EMU[1:0]** — **Operation** 00 — Boundary Scan/Normal Mode 01 — Reserved 10 — Reserved 11 — Emulation/Normal Mode **NOTE:** Check the data sheet for more information about these pins. To use with Code Composer Studio, Emulation/Normal mode should be selected. $\overline{\text{TRST}}$ has an internal pull-down, though it may be useful to include an external pull-down. In the future, TI will be switching to more advanced emulation using a 60-pin header instead of the traditional 14-pin. See the aforementioned *60-Pin Emulation Header Technical Reference* for details. For now, leave the extra emulation pins EMU[11:2] unconnected because they have internal pull-ups. For full details on designing with JTAG, see *IEE Std 1149.1 (JTAG) Testability Primer* (SSYA002). The IEEE Std 1149.1 (JTAG) Testability Primer provides additional information that is useful. These resources will allow you to check your JTAG circuitry for correctness. *IEEE Std 1149.1 (JTAG) Testability Primer (SSYA002)*
☐	Are the McBSP signals pinned to via for scope trace? For debugging informaiton it can be very useful to have the McBSP signals pinned out to a via. This allows you to check the signals (clock, frame sync, data, etc.,) on a scope for correct operation.
☐	Do the DSP vias go all the way through the board? For debugging information it can be very useful to have the McBSP signals pinned out to a via. This allows you to check the signals (clock, frame sync, data, etc.) on a scope for correct operation. It is extremely helpful to have the DSP pins available through all layers. This will increase the layout difficulty. However, this will also allow visibility into all possible pins on the DSP, which can be a useful for debug.
☐	How much general visibility is there on the board? If space allows it, the more signals and pins that are accessible, the easier it is to debug. One common consideration is adding hooks for a logic analyzer on the EMIF bus. This can help with any timing issues that might come up during development.
☐	Are there any GPIOs pinned out to via or LED for probing? GPIOs can be very useful for debugging. If a GPIO pin is available for use, it is worthwhile to pin it out to a via or an LED to observe the operation.

4.2 Debug Checklist

☐	Are the power supplies clean? Noisy supplies can create several problems in your system. Be sure that your power supplies are working as expected.
☐	Do EMIF timings match the data sheets? The data sheets for both the DSP and the external memory device should have timing diagrams. Check the timings from the point of view of both the DSP and external memory, and make sure the signals match their respective data sheets. An IBIS model can also be used to examine timings.
☐	Are the EMIF Clocks set up properly? To interface correctly with external memory like SDRAM, check the specifications for your memory's speed, then set the clock to the EMIF. Three options exist for the EMIF clock: CPU/4, CPU/6, or external ECLKIN. Check clocks with a scope for proper frequency.
☐	Are the CE spaces configured correctly? Using the EMIF control registers for each CE space make sure that each space is configured for the appropriate form of external memory. *Important note:* If booting from ROM, the ROM device needs to be on CE1, since the on-chip boot loader automatically looks there to start a ROM boot.
☐	Is the scan chain length set correctly? If the scan chain length is not detected properly on your board, Code Composer Studio will not correctly recognize power to the DSP. If it is a multiprocessor board, a scan chain test should return the correct number of devices.
☐	If it is a multiprocessor, is the TDI/TDO connection tied properly? In multiprocessor environments, the TDI (JTAG test-port data in) and TDO (JTAG test-port data out) pins need to be tied correctly. The TDI pin on the JTAG header should tie to the TDI pin on the first DSP, and the TDO pin on the first DSP should tie to the TDI pin on the second DSP. This sequence should continue for subsequent DSPs, until the TDO pin of the last DSP connects to the JTAG header's TDO pin. For more information on designing for JTAG emulation, see Chapter 16 of *TMS320C6000 Designing for JTAG Emulation Reference Guide* (SPRU641).

☐	If you can launch Code Composer Studio are you able to access the CPU registers? A good test to see if the emulation software can communicate with the DSP is to launch Code Composer Studio and then select the CPU registers from the toolbar and modify an A-side or B-side register.
☐	Simple memory accesses can be performed with no code. Before you have code available you can test memory accesses using Code Composer Studio. A simple method of doing this involves selecting the EMIF registers view from the toolbar in Code Composer Studio and setting these registers to their appropriate value based on the type of memory you will access. You can then open a memory window from the toolbar and read or write the memory of interest.

5 Summary

Using the information provided in this document, along with documentation that is pointed out for each step of the design process, a DSP designer will be able to make more knowledgeable decisions concerning their design.

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