Preliminary

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TEXAS INSTRUMENTS

Implementing DDR2 PCB Layout on theTMS320TCI6482

Michael Shust   *High Speed HW Productization*

ABSTRACT

This application report contains implementation instructions for the DDR2 interface contained on the TCI6482 DSP device. The approach to specifying interface timing for the DDR2 interface is quite different than on previous devices.

The previous approach specified device timing in terms of data sheet specifications and simulation models. The customer was required to obtain compatible memory devices, as well as their data sheets and simulation models. The customer would then take this information and design their printed circuit board (PCB) using high speed simulation to close system timing.

For the TCI6482 DDR2 interface, the approach is to specify compatible DDR2 devices and provide the PCB routing rule solution directly to the customer. TI has performed the simulation and system design work to ensure DDR2 interface timings are met. The DDR2 system solution is referred to as the TCI6482 DDR2 collateral. This document describes the content of this collateral.

The TCI6482 DSK and EVM provide example PCB layouts following these routing rules that pass FCC EMI requirements. The DSK contains a single TCI6482 device and the EVM is a DSK with an attached daughter card containing another TCI6482 device. Both DDR2 layouts on the DSK/EVM meet the routing rules detailed in this document. The customer may copy these DDR2 layouts directly, but the intent is to allow enough flexibility in the routing rules to meet other PCB requirements and allow the customer to derive an optimized layout for their specific application.

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1   Prerequisites

1.1   High Speed Design

While the goal of the TCI6482/Device_Name2_Short collateral is to make system implementation easier for the customer by providing the system solution, it is still expected that the PCB design work be supervised by a knowledgeable high speed PCB designer as an assumption is made that the PCB designer is using established high speed design rules. Ground plane cuts should be avoided if at all possible as they are tricky to do correctly. Crosstalk and EMI impacts due to PCB design should be evaluated as the PCB design progresses as it can be difficult to go back and fix issues later. Thorough planning will aid in the design cycle.

1.2   Familiarity with the JEDEC DDR2 Specification

The DDR2 interface on the TCI6482/Device_Name2_Short device is designed to be compatible with the JEDEC JESD-79A DDR2 specification. It is assumed that the reader is familiar with this specification and the basic electrical operation of the interface. In addition, several memory manufacturers provide detailed application notes on DDR2 operation.

2   TCI6482 DDR2 Supported Devices

Table 1 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-533 speed grade DDR2 devices.

Table 1. Compatible JEDEC DDR2 Devices

No.	Parameter	Min	Max	Unit	Notes
1	JEDEC DDR2 Device Speed Grade	DDR2-533			See [1]
2	JEDEC DDR2 Device Bit Width	x16	x16	Bits	
3	JEDEC DDR2 Device Count	1	2	Devices	See [2]
4	JEDEC DDR2 Device Ball Count	84	92	Balls	See [3]

[1]   Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.
[2]   1 DDR2 device is used for 16 bit DDR2 memory system. 2 DDR2 devices are used for 32 bit DDR2 memory system.
[3]   92 ball devices retained for legacy support. New designs will migrate to 84 ball DDR2 devices. Electrically, the 92 and 84 ball DDR2 devices are the same.

3   Other Documentation

Specific examples of the implementation of this specification including schematics and a PCB layout can be obtained from the TCI6482 DSK documentation. In addition, the interested reader is referred to the *High Speed DSP Systems Design Guide* (SPRU889).

For configuration of the DDR interface, refer to the *TMS320TCI648x DSP DDR2 Memory Controller User's Guide* (SPRU894).

4   Schematics and Electrical Connections

Figure 1 shows a high level schematic of the DDR2 interface. Specific pin numbers can be obtained from the TCI6482 and JEDEC DDR2 data sheets. The 32 bit DDR2 interface of TCI6482 is connected to two 16 bit DDR2 devices, thus the clock, address, and control connections are three point nets and the data lines are point to point nets.

Figure 1. TCI6482 DDR2 High Level Schematic
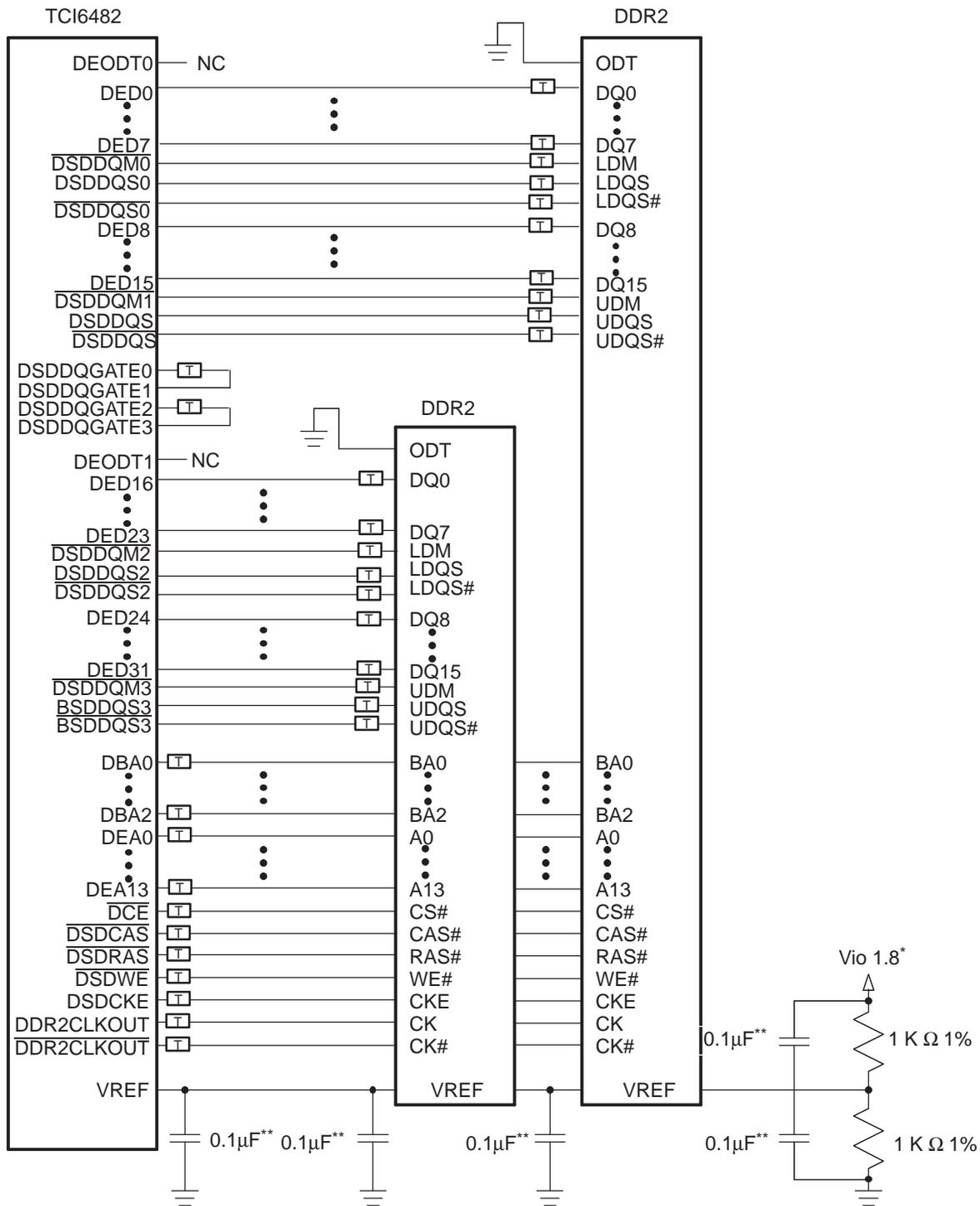
⊡ Terminator, if desired. See terminator comments.

* Vio1.8 is the power supply for the DDR2 memories and TCI6482 DDR2 interface.

** One of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin.

4.1 Differences Between the TCI6482 DDR2 Interface and the Typical PC Application

There are some subtle differences between the embedded DDR2 application used on TCI6482 and the typical PC motherboard/DDR2 DIMM application. The TCI6482 DDR2 interface does not use stub series termination (the SST in SSTL). Stub series terminators are parallel terminators and they are not used in this case due to their high power consumption. Consequently, the termination voltage, V*tt*, is also not used nor is it required for the TCI6482 DDR2 interface. The terminators shown in Figure 1 are series resistor terminators.

4.2 DDR2 Power Supplies

The power supply for the DDR2 interface is 1.8 V ± 0.1 V. This power supply is used for the TCI6482/Device_Name2_Short DDR2 power pins (DV_{DD18}) as well as the JEDEC DDR2 devices. VREF is derived from the DDR2 power supply via a resistive divider. Bypassing for the 1.8 V and VREF supplies are covered in this document.

4.3 Signal Terminations

In order to meet the maximum interface speed (267MHz/533Mbps) memory device drive strength, configurable by bit A1 in the memory device EMRS1 register, should be set to 100% strength. This requires the series terminations which are specified in Section 6.3.4 to avoid excessive under-shoot/over-shoot. If 60% drive strength mode is used, series terminations can be eliminated but the maximum operating frequency is reduced to 200MHz/400Mbps. The no termination approach for new designs is not without risk, however.

Terminations on the PCB will allow the DDR2 signals to be tuned to meet EMI certification requirements. A PCB which fails EMI certification without terminations will likely have to be re-spun in order to address the EMI shortcomings. It can take multiple PCB spins to correct EMI issues. Note that re-spinning a dense non-terminated PCB layout to include terminators can be a very difficult effort because physical room must be made for the terminations. This means an entire PCB design may have to be redone. It is much easier to remove terminations rather than adding them after the PCB has been found to fail EMI.

Customers who are sensitive to the cost/schedule issues with respect to EMI may wish to include terminations on their boards even though they plan not to have terminations on the final product. This way, the terminations can easily be replaced with zero ohm resistors and checked for EMI compliance. If the PCB fails EMI, it is then straightforward to install the necessary terminations without re-spinning the PCB. Once the termination scheme has been verified to pass EMI, the remaining zero ohm terminations can be carefully removed from the PCB layout in a single PCB design spin.

5 Stackup

The minimum stackup required for routing TCI6482 is a 6 layer stack as shown in Table 2. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the TCI6482/DDR2 PCB footprint.

Table 2. Minimum PCB Stackup

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

Systems utilizing the RIO interface should have the target PCB impedance optimized for the differential impedance required by that interface. Single ended controlled impedance with a nominal value between 50 and 60 ohms is acceptable for the DDR2 interface. DDR2 impedance should be controlled to within +/-15% of its nominal impedance.

5.1 Ground Reference Planes

It is critical that all signal routing layers have a *ground reference plane*, meaning that there is a full, contiguous ground plane next to every DDR2 routing layer. Two routing layers can share a ground plane (one signal layer above, and one signal layer below the ground plane). Ground plane cuts are not allowed in the DDR2 region (Ground plane cuts are generally a bad idea, and should only be done very carefully, only if absolutely necessary on other areas of the PCB). The purpose of the ground plane is to provide a path for return currents to minimize crosstalk and EMI. Power planes cannot be used as signal returns for the DDR2 interface. *Improper ground plane stackup will likely cause the DDR2 interface to fail or operate unreliably.*

5.2 Stackup Routing Impacts

The internal routing planes (stripline) have different flight times than top/bottom (microstrip) routing planes. Ideally the trace routes within the same net class (covered in detail in Section 7.4) should either all be microstrip or stripline so that trace length matching can be done. If a combination of microstrip and stripline is used within a net class the trace length should be adjusted to offset the delay difference. The trace flight times for microstrip and stripline should be determined for the specific board stackup being used.

6 Placement

Figure 2 shows the required placement of the TCI6482 device as well as the DDR2 devices. The distances shown are maximums and there are no restrictions on how close the devices can be to each other. Generally, closer is better both from a cost and signal integrity point of view, but the tightness of the layout will be limited by the room required by the signal traces. Note that minimum placement is usually limited by the number of vias required to route the design, not the traces themselves. The PCB designer needs to take the routing requirements into consideration while determining placement.
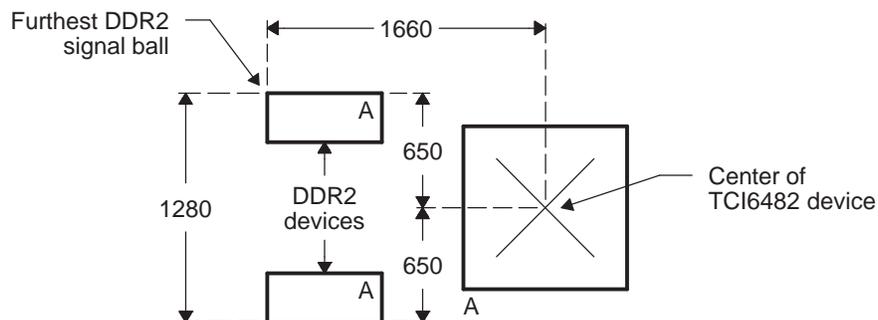
Maximum placement distances from center of TCI6482 package to furthest DDR2 signal ball. Does not include distances to possible DDR2 NC outrigger balls. All dimesions in mils.

Figure 2. TCI6482 and DDR2 Device Placement Specification

6.1 Minimizing PCB Area

The maximum placement and minimum PCB stackup uses the lowest cost PCB technology and generally results in the lowest unit cost PCB at the penalty of the largest footprint for the DDR2 interface. Customers need to evaluate the cost/benefit tradeoffs of smaller feature sizes and additional signal layers for their systems. Note that the minimum feature size and stackup may be limited by other circuitry on the PCB.

6.2 DDR2 Keep Out Region

Figure 3 shows an example DDR2 keep out region. This keep out region will vary with the individual design. Its purpose is to ensure other signals do not interfere with the DDR2 interface. The only signals allowed on the DDR2 signal layers are those for this interface. The 1.8V power partial plane should encompass at least the entire DDR2 keep out region.
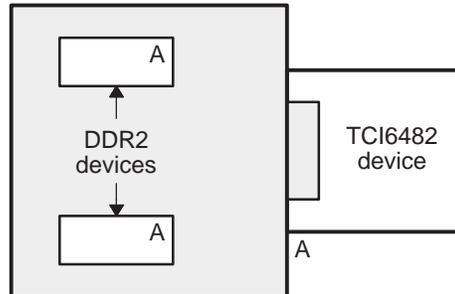
Example DDR2 keepout region. Region should encompass all DDR2 circuitry and will vary depending on placement. Non−DDR2 signals shall not be routed on the DDR2 signal layers. Non−DDR2 signals may be routed in this region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks shall be allowed in the reference ground layers in this region. In addition, 1.8V power plane should cover the entire keep out region.

Figure 3. Example DDR2 Keep Out Region

6.3 Discrete Device Placement

The TCI6482 DDR2 interface uses a number of discrete devices consisting of resistors, resistor packs, capacitors, and EMI filters. Figure 5 shows an example placement of discrete devices around TCI6482 and the DDR2 devices. It is useful to refer to it while reading the next sections.

6.3.1 PLL and DLL Filters

The PLL and DLL power supply pins on the TCI6482 device draw small currents, but they are noise sensitive. All the PLL and DLL power supplies are derived from the Vio1.8 supply. Each supply filters the Vio1.8 using a filter circuit and two capacitors. Figure 4 shows the placement and routing rules for the PLL and DLL power supplies. The filter capacitors are 0402 in physical size. Note that the PLLV1 is the PLL for the CPU core clock but is covered in this solution since it impacts the placement and layout of the DDR interface.

Vio1.8

EMI filter

TCI6482 pin

Figure 4. PLL and DLL Filters Requirements
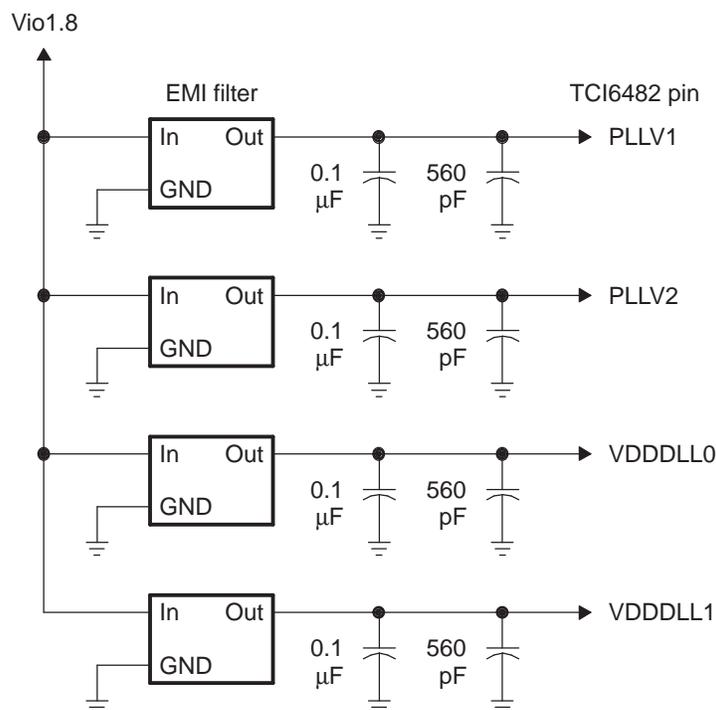
Center of EMI Filter component should be placed no longer than 350 mils from associated TCI6482 ball.

Capacitors shown in this figure should be placed in between EMI filter and the TCI6482 ball.

Traces for the nets in this figure should be 15 mils wide minimum. Necking down for BGA fanout is acceptable.

6.3.2 Resistors and Resistor Packs

The TCI6482 DDR2 interface uses resistors for VREF generation and may use resistors or resistor packs for signal terminations. Specific placement requirements for these components are specified by the routing rules for VREF and the other net classes of the interface. These routing rules are presented later in this document.

Generally speaking, termination resistors can be either discrete resistors or resistor packs and they are placed in between the DDR2 memories and the TCI6482. The VREF divider resistors will be placed somewhere in between the DDR2 devices and the TCI6482.

6.3.3 Decoupling Capacitors

Decoupling capacitors are critical to the reliable operation of a high speed PCB. Great care should be taken to ensure the following guidelines are followed. Failure to follow these guidelines will likely result in an unstable system.

For details on the overall quantity and type of decoupling and bulk capacitors refer to the *TMS320TCI6482 Design Guide and Comparisons to TMS320TCI100* (SPRAAC7). The small decoupling capacitors should be 0402 size or smaller.

Exact placement of capacitors is not critical. Figure 5 is an example placement. Decoupling capacitors should be placed near the device being decoupled. Distance from the capacitor to the power pins being decoupled should not exceed 125 mils.

6.3.3.1   *Decoupling Capacitor Vias, Connections to Power Planes, and Placement*

Each decoupling capacitor requires two vias, one for each pin. Via sharing for decoupling capacitors is not permitted. This is due to the inductance of the vias. Via sharing seriously compromises the performance of the decoupling capacitor due to this inductance. For the same reason, sharing of vias by power and ground pins of the TCI6482 or DDR2 devices is also not permitted. Vias used for decoupling capacitor and device power connections are referred to as power vias.

To minimize inductance, power vias should be as large as possible. Use care to ensure power vias are not so large as to inadvertently cut planes. Power vias should be connected to the device pads with the shortest possible traces that are as wide as possible. Ideally, the trace length from the power via to the device pad should not exceed 30 mils. Maximum trace length from power via to decoupling capacitor is 60 mils. Maximum trace length from power via to power ball pad is 35 mils.

Figure 5 shows an example placement for the decoupling capacitors. Placement of the bulk capacitors is not that critical and they can be placed to accommodate other circuitry with more constrained placement and routing requirements. The PCB designer should keep the trace length specifications in this section in mind when placing the capacitors.
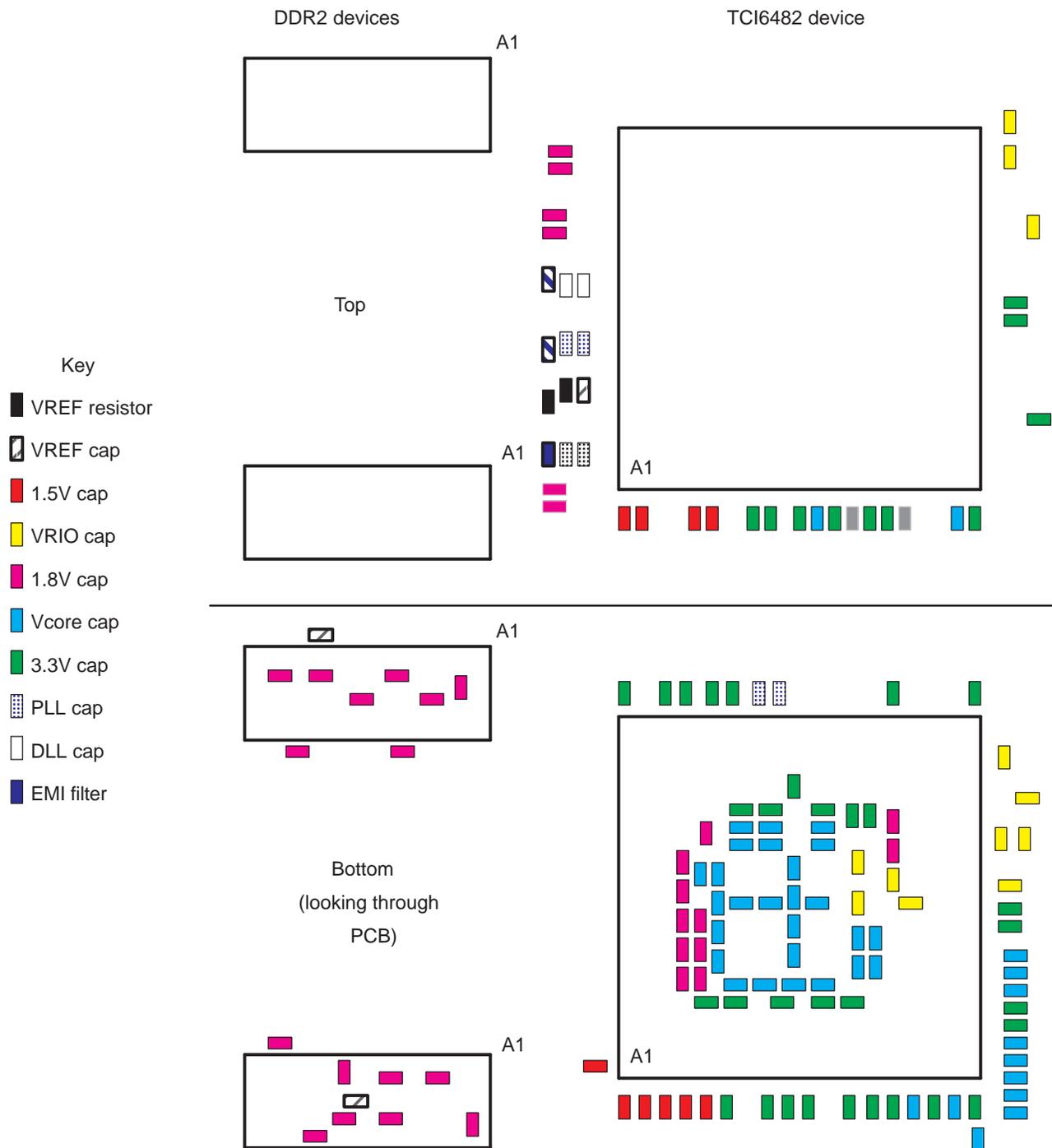
Figure 5. Discrete Part Placement

6.3.4   DDR2 Signal Terminations

Series terminations are required if the DDR device is operated at 100% strength. The combination of series terminations and 100% drive strength can provide operation up to 267MHz. Termination is not required to meet reflection and overshoot specifications provided the DDR2 device is operated at 60% strength, but no termination and 60% strength limits the operating frequency to 200MHz.

Recommended terminations are shown in Table 3 . There is room in the placement shown in Figure 2 for the terminations in Table 3. Termination values may have to be adjusted once hardware is available to pass EMI regulations.

Table 3. DDR2 Signal Terminations

Net Class	Termination
CK	10 ohm series resistor/resistor packs located near DSP
ADDR_CTRL	22 ohm series resistor/resistor packs located near DSP
DQB0 (DED0-DED7)	22 ohm series resistor/resistor packs located near DDR2
DQB0 (DSDDQM0)	22 ohm series resistor/resistor packs located near C6482
DQB1 (DSDDQM1)	22 ohm series resistor/resistor packs located near C6482
DQSB0	22 ohm series resistor/resistor packs located near DDR2
DQB1 (DED8-DED15)	22 ohm series resistor/resistor packs located near DDR2
DQSB1	22 ohm series resistor/resistor packs located near DDR2
DQB2 (DED16-DED23)	22 ohm series resistor/resistor packs located near DDR2
DQB2 (DSDDQM2)	22 ohm series resistor/resistor packs located near C6482
DQSB2	22 ohm series resistor/resistor packs located near DDR2
DQB3 (DED24-DED31)	22 ohm series resistor/resistor packs located near DDR2
DQB3 (DSDDQM3)	22 ohm series resistor/resistor packs located near C6482
DQSB3	22 ohm series resistor/resistor packs located near DDR2
DQGATEL	10 ohm series resistor/resistor packs located near DQGATE0
DQGATEH	10 ohm series resistor/resistor packs located near DQGATE2

7   Routing

7.1   Required PCB Feature Sizes

The minimum PCB feature sizes referenced in this document are the largest that can be accommodated in order to physically route the PCB due to the size of the BGA packages. Smaller feature sizes can also be used as well to improve PCB density as long as the routing rules are followed.

The PCB routing rules in this document assume a minimum PCB route width and spacing of 4 mils. The PCB route trace width is defined as w for the purposes of defining minimum trace separation for the various net classes discussed later in the routing rules. Thus, if the PCB is designed with the widest possible traces, then the trace width is w = 4 mils.

Pad stacks for the DDR2 and TCI6482 BGA pads should be 14 mil diameter copper with 20 mil diameter solder masks (non-solder mask defined pads). Escape and general DDR2 routing vias should have 8 mil holes with 18 mil pads. BGA escape is accomplished by the typical dog bone method.

It is also a good idea to maximize the size of the vias used for decoupling capacitors and power pins. This is done to minimize via inductance. It is the via and decoupling capacitor stray inductance that limits the performance of the decoupling capacitors. Use care to ensure that vias are not sized so large as to cut off a portion of a plane.

7.2   VREF

VREF is used by the input buffers of the DDR2 memories as well as TCI6482's DDR2 interface to determine logic levels. VREF is specified to be ½ the power supply voltage and is created using a voltage divider constructed from two 1K ohm, 1% tolerance resistors, see Figure 1. VREF is not a high current supply, but it is important to keep it as quiet as possible with minimal inductance. The minimum nominal trace width for VREF is 20 mils. Necking down VREF to accommodate BGA escape and localized via congestion is acceptable, but care should be taken to keep VREF 20 mils wide as much as possible. VREF is a DC net and as such, trace delay is not critical, however, overall trace length should be kept to a minimum. The four or five decoupling capacitors on the VREF net are intended to reduce AC noise. Two are used at the divider, and one each is used near the VREF input of the three loads (2 DDR2's and TCI6482). See Figure 6.

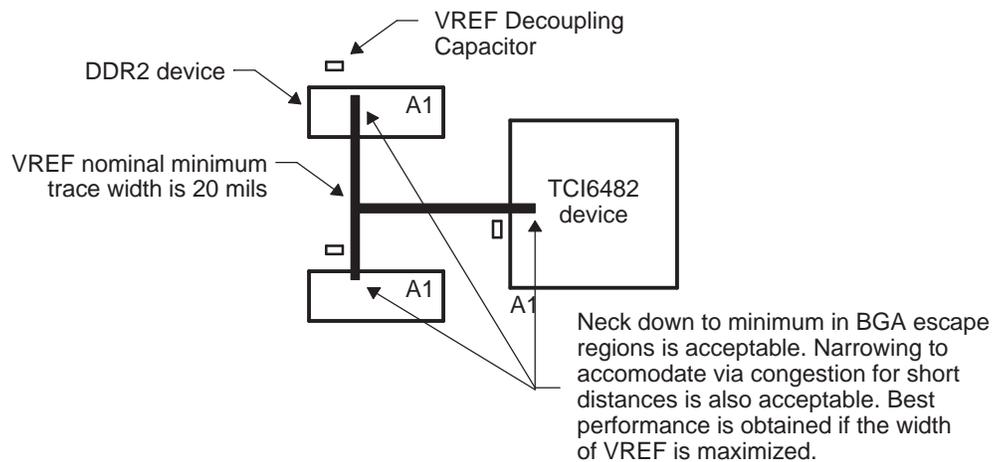**Figure 6. VREF Specification**

7.3 General DDR2 Routing

Figure 7 through Figure 11illustrate the general routing of the DDR2 interface. The address, bank address, control signals, as well as the DDR2 clock route from the center of the TCI6482 device to the DDR2 devices in a "balanced T" route. Each data byte is routed point to point, with the lower two bytes routing to the lower DDR2 memory and the upper two bytes routing to the upper DDR2 memory. The figures show the maximum PCB area placement. Tighter placements are achieved by reducing feature size and/or adding PCB layers and pulling the DDR2 memories toward each other and/or closer to the TCI6482 device. The routing of the DDR2 interface should look similar to these figures when a proper placement is used. Note that the most extreme minimum placement of DDR2 devices, overlapping each other with one on the top and the other on the bottom of the PCB should work; however, all routing rules must still be followed. This type of placement will require advanced PCB technology.
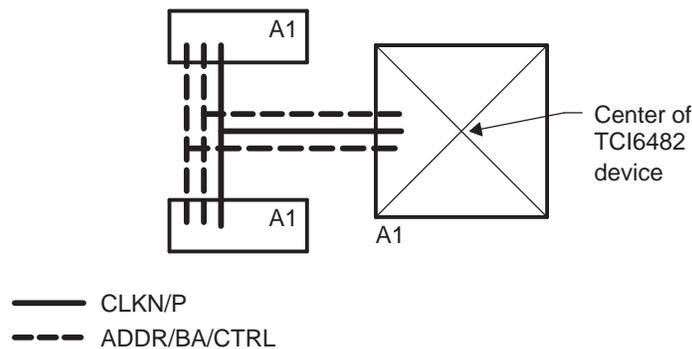
Address/BA/Control Routing

Figure 7. General Address, Bank Address, Control and Clock Routing

DQS0N/P

DQ0−7,DQM0
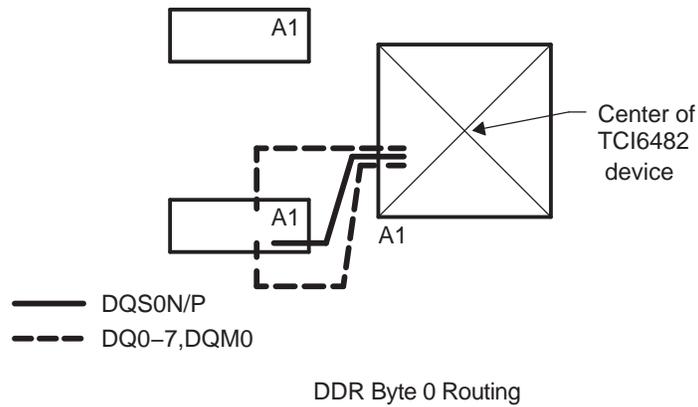
DDR Byte 0 Routing

Figure 8. General Data Byte 0 Routing

DQS1N/P

DQ7−15,DQM1

DDR Data Byte 1 Routing
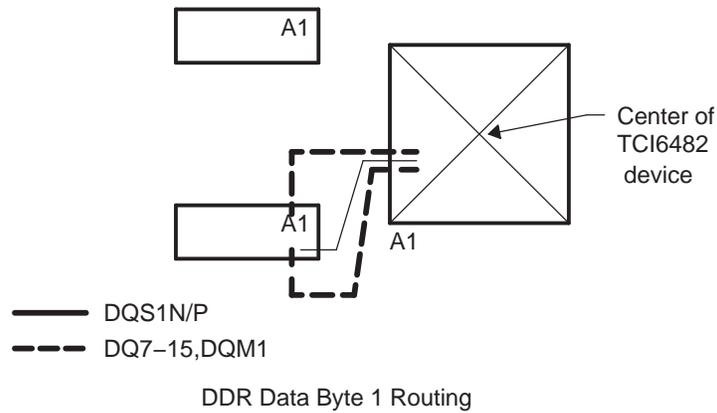
Figure 9. General Data Byte 1 Routing

DQS2N/P

DQ16−23,DQM2

DDR Data Byte 2 Routing
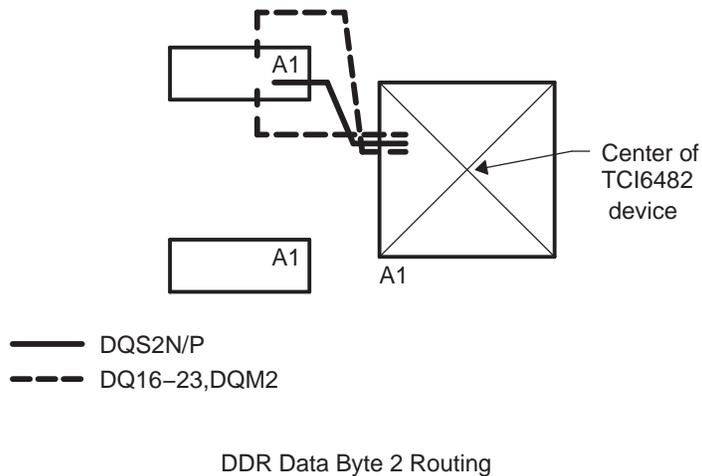
Figure 10. General Data Byte 2 Routing
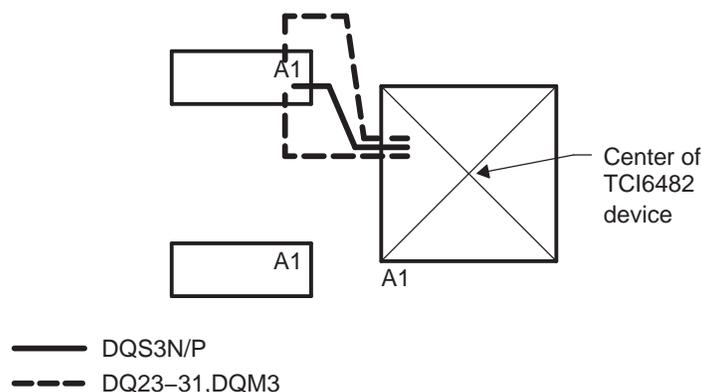
DDR Data Byte 3 Routing

Figure 11. General Data Byte 3 Routing

7.4 Signal Routing Rules

The routing rules for the TCI6482 DDR2 system design are divided among net classes. Each net class contains all the signals within a clock domain. There are five clock domains: CK, DQS0, DQS1, DQS2, and DQS3. The general requirement is to skew match within a domain and to minimize crosstalk. Crosstalk across domains is especially troublesome and steps should be taken to minimize coupling between signals in different domains.

7.4.1 Net Classes

7.4.1.1 Clock Net Classes

Net classes are used to associate the assorted groups of nets in the DDR2 interface to each other and their clock domain. These net classes are used in the DDR2 routing rules. The DDR2 interface has five clock net classes, four of which are bi-directional. The clock net classes are shown in Table 4.

All of the clock signals in the TCI6482 DDR2 interface are differential signals. As such, each clock domain net class needs to be routed as a differential signal with matched lengths for the non-inverting and inverting signals. Differential impedance should also be controlled.

7.4.1.2 Signal Net Classes

Table 5 shows the seven additional net classes that use the clock net classes as their reference. Generally speaking, the nets within a net class and their associated clock net class should be skew matched to each other. The goal is to minimize the skew within each clock domain and crosstalk between signals – especially between signals of differing clock domains.

Table 4. Clock Net Classes

Clock Net Class	Description	DSP Pin Names
CK	DDR2 Interface Clock	DDR2CLKOUT, $\overline{\text{DDR2CLKOUT}}$
DQSB0	DQS for byte 0	DSDDQS0, $\overline{\text{DSDDQS0}}$
DQSB1	DQS for byte 1	DSDDQS1, $\overline{\text{DSDDQS1}}$
DQSB2	DQS for byte 2	DSDDQS2, $\overline{\text{DSDDQS2}}$
DQSB3	DQS for byte 3	DSDDQS3, $\overline{\text{DSDDQS3}}$

Table 5. Signal Net Classes

Net Class	Associated Clock Net Class	Description	DSP Pin Names
ADDR_CTRL	CK	Bank Address, Address, Control	DBA0-A2, DEA00-DEA13, $\overline{DCE}$, $\overline{DSDCAS}$, $\overline{DSDRAS}$, $\overline{DSDWE}$, DSDCKE
DQB0	DQSB0	DQs for byte 0	DED00-DED07, $\overline{DSDDQM0}$
DQB1	DQSB1	DQs for byte 1	DED08-BED15, $\overline{DSDDQM1}$
DQB2	DQSB2	DQs for byte 2	DED16-DED23, $\overline{DSDDQM2}$
DQB3	DQSB3	DQs for byte 3	DED24-DED31, $\overline{DSDDQM3}$
DQGATEL	CK, DQSB0-1	DQ gate timing loop for lower word	DSDDQGATE0, DSDDQGATE1
DQGATEH	CK, DQSB2-3	DQ gate timing loop for upper word	DSDDQGATE2, DSDDQGATE3

7.4.1.3 A Word About Trace Separation and BGA Escapes

The net class routing rules in the next section give minimum trace separation requirements for the respective net class. It is understood that in the region near the BGA devices that the traces will have to be routed quite close together, many times at minimum trace separation. Minimum separation routing should be kept to a minimum and the total minimum separation routed length should not exceed 500 mils for each net.

7.5 Net Class Routing Rules

7.5.1 General Rules for Net Classes

Vias add a significant delay. Within a net class the number of vias on each net should ideally be kept the same. An allowance of 1 mismatch in the number of vias is acceptable for single ended signals. Differential signals must have the same number of vias on each side of the differential pair:

- CK must have the same number of vias as CK#
- DQS must have the same number of vias as DQSn#

Trace routes should be made as short and direct as possible. All trace routes should be less than 3 inches when measured from source to destination (not include the full "T" trace length).

7.5.2 CK and ADDR_CTRL

This net class is completely sourced by the TCI6482 DSP to the DDR2 devices. Each net is a balanced "T" route, see Figure 12. Ideally, the PCB delay of the CK net class is identical to the delay for the ADDR_CTRL net class. All nets in the CK and ADDR_CTRL net classes should be matched in length to each other within 100 mils. The nets in the CK net class must be laid out as a differential pair. The trace separation between the differential pair of net class CK should be such to maintain the desired differential impedance. Other traces should be kept away from the CK net class traces by at least 4w center to spacing (recall that w = minimum trace width/space). Traces within the ADDR_CTRL net class should be spaced at least 3w center-to-center from each other. Traces of other net classes should be kept 4*w* away from the ADDR_CTRL net class. The length of segment A should be maximized and the overall length from A to B or A to C should be minimized.

7.5.3 DQSBn and DQBn

The 8 net classes that make up the 4 DQS's and 4 DQ bytes have the same routing rules. Note the individual byte net classes do not have to be skew matched to each other. Skew matching is only required between the DQBn net class and its associated DQSBn net class. Figure 13 shows the topologies for the DQSBn and DQSB nets.

These net classes are sourced by the TCI6482 device during writes and are sourced by the DDR2 devices during reads. The DQS acts as the data strobe at it is always sourced with the DQs. For write cycles, the DQS transitions in the middle of the bits cells on DQ. For read cycles, the DQS transitions at the same time as the DQS. The interface is more sensitive to DQS <-> DQ crosstalk during reads. The data mask bits (DSDDQMn) are static during reads, thus they can be used as shields between the DQ and DQS to improve read crosstalk performance.

Ideally, the PCB delay of the DQSBn net class is identical to the delay for the DQBn net class. All nets in the DQSBn and DQBn net class should be matched in length to each other within 100 mils. The longest trace permissible is equal to the longest manhattan distance of the DQSBn and DQBn net classes. The nets in the DQSBn net class must be laid out as a differential pair. The trace separation between the differential pair of net class DQSBn should be such to maintain the desired differential impedance. Other traces should be kept away from the DQSBn net class traces by at least $4w$ center to spacing (recall that w = minimum trace width/space). Traces within the DQBn net classes should be spaced at least $3w$ center to center from each other. Traces of other net classes should be kept $4w$ away from the DQBn net class.

There is a fairly loose timing requirement for DQSn relative to CK. For this reason, the DQSn trace lengths should be within +/- 1.5 inch of CK.

7.5.4 DQGATEL and DQGATEH

These two net classes are used by the TCI6482 to predict the round trip delay of the PCB layout. The result is two out and back PCB traces that match the delay of the clock net plus the DQS. The rules for these net classes are shown in Figure 14.

For DQGATEL, the TCI6482 DSDDQGATE0 pin should be routed out and back to the TCI6482 DSDDQGATE1 pin. The total length of this route should be equal to the length of the CK net class plus the average length of the DQSB0 and DQSB1 net classes.

For DQGATEH, the TCI6482 DSDDQGATE2 pin should be routed out and back to the TCI6482 DSDDQGATE3 pin. The total length of this route should be equal to the length of the CK net class plus the average length of the DQSB2 and DQSB3 net classes.

Route Spacing Requirements
ADDR_CTRL and CK

Matching and Topology Requirements
ADDR_CTRL and CK

For ADDR_CTRL and CK:

1) Length B should match length C within 100mils.

2) Length A to C and A to B should match within 100 mils
within ADDR_CTRL net class.

3) Series terminating resistor, if desired, should be lo-
cated closest to DSP as possible.

4) Length A should be maximized while meeting the
above specifications.

In addition, for CK:

5) The length of CK should match length of net CK#
within +/−10 mils.

Figure 12. Routing Spacing, Matching, and Topology Requirements for ADDRL_CTRL and CK Net Classes
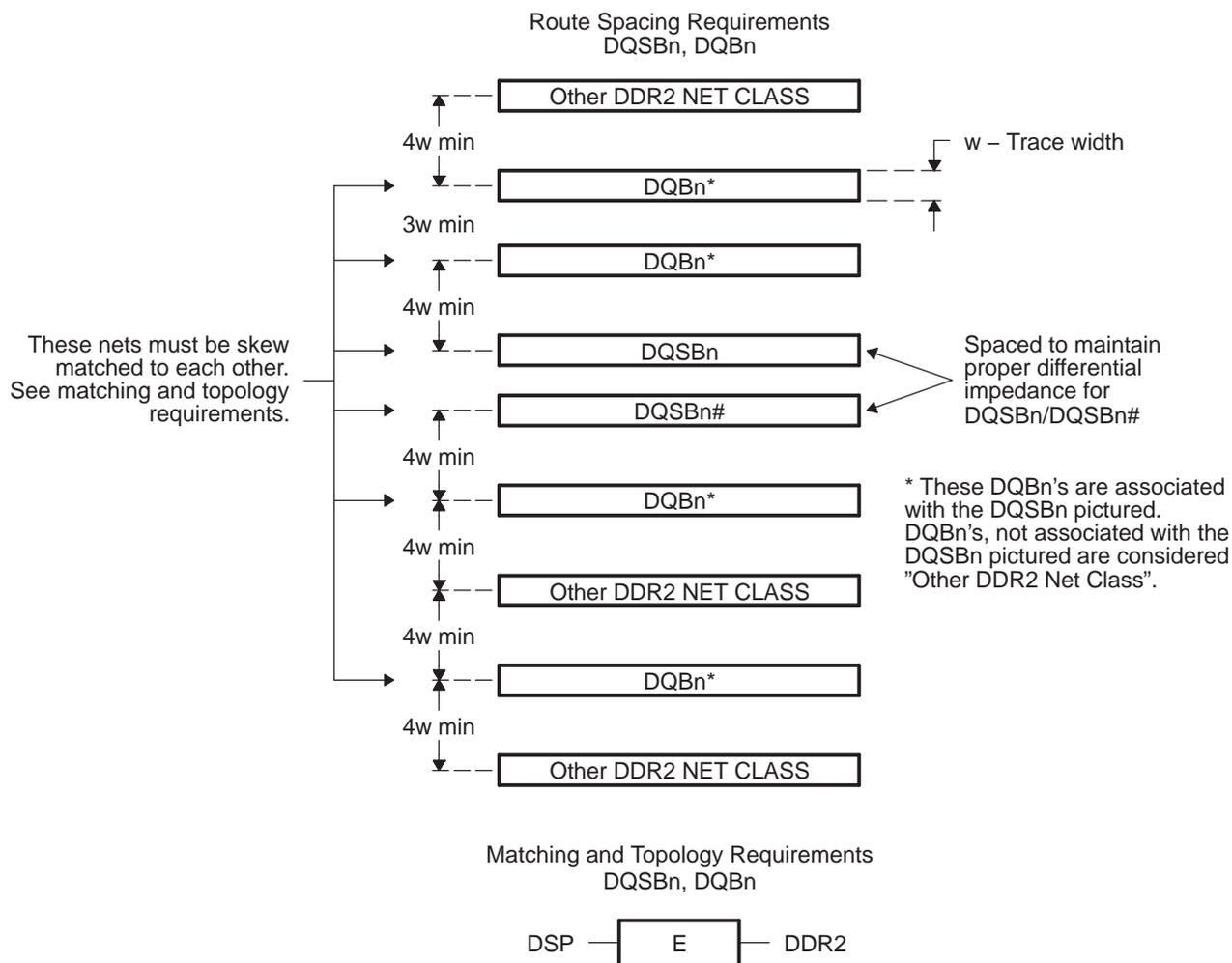
Route Spacing Requirements
DQSBn, DQBn

Matching and Topology Requirements
DQSBn, DQBn

For DQBn and DQSBn:

1) Length E should match within 100 mils within the DQSB0 and DQB0 net classes.

2) Length E should match within 100 mils within the DQSB1 and DQB1 net classes.

3) Length E should match within 100 mils within the DQSB2 and DQB2 net classes.

4) Length E should match within 100 mils within the DQSB3 and DQB3 net classes.

5) Series terminating resistor, if desired, should be located closest to DDR2 as possible for data bits (DEDn) and closest to DSP as possible for data masks (DSDDQMn).

In addition, for DQSBn:

6) The length of DQSBn should match length of net DQSBn# within +/−10 mils.

7) The length of DQSBn/DQSBn# should be within +/−1.5 inches of CK/CK#.

Figure 13. Route Spacing, Matching, and Topology Requirements for the DQBn and DQBSn Net Classes

Routing Space Requirements
DQGATEL, DQGATEH

Matching and Topology Requirements
DQGATEL, DQGATEH
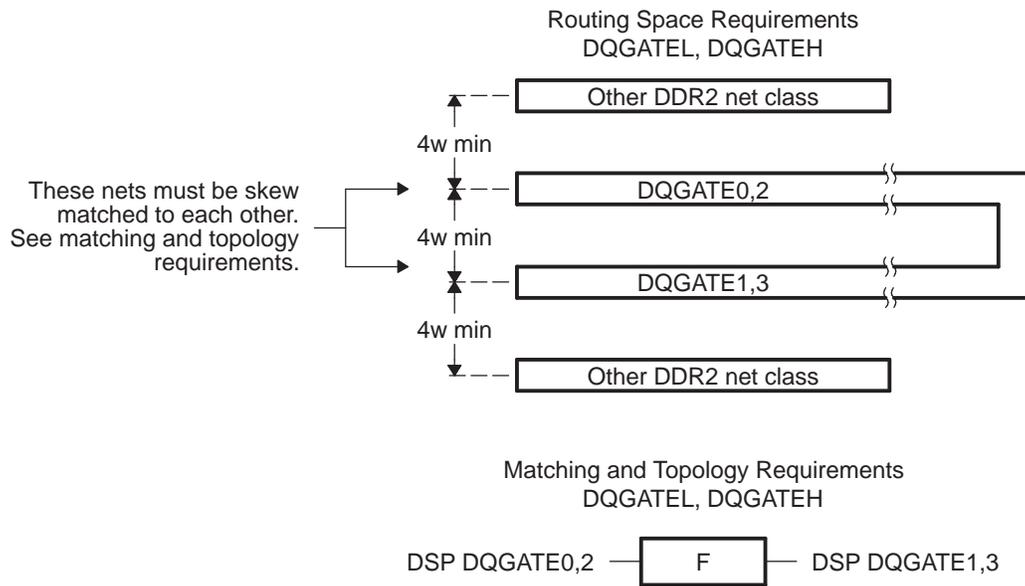
For DQGATEL and DQGATEH:

1) Length F should be equal to the length of the CK net class plus the average of the DQSB0 and DQSB1 for the DQGATEL net class.

2) Length F should be equal to the length of the CK net class plus the average of the DQSB2 and DQSB3 for the DQGATEH net class.

3) Series terminating resistor, if desired, should be located closest to DSP DQGATE0 or DQGATE2 as possible.

Figure 14. Route Spacing, Matching, and Topology Requirements for the DQGATEL and DQGATEH Net Classes

Appendix A Revision History

This document has been revised to include the following technical change(s).

Table 6. Revisions

Location	Additions, Deletions, Edits
Section 2	This section has been replaced.