Application Report
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Implementing Serial Rapid I/O PCB Layout on a TMS320TCI6482 Hardware Design

Todd Hiers — *High Speed HW Productization*

This application report contains implementation instructions for the Serial Rapid I/O (SRIO) interface on the TMS320TCI6482 DSP device. The approach to specifying interface timing and physical requirements for the SRIO interface is quite different than previous approaches for other interfaces.

Serial Rapid I/O is an industry-standard high-speed switched-packet interconnect. Physical layer data transmission utilizes analog serializer/deserializers (serdes) to feed low-output-swing differential CML buffers. Proper printed circuit board (PCB) design for this interface resembles analog or RF design, and is very different than traditional parallel digital bus design.

Due to this analog nature of SRIO, it is not possible to specify the interface in a traditional DSP digital interface manner. Furthermore, it is undesirable to specify the interface in terms of the raw physical requirements laid out by the SRIO specification. Understanding the SRIO specification and producing a compliant PCB based on the explicit and implicit requirements there demands significant time, experience, and expensive tools.

For the TMS320TCI6482 SRIO interface, the approach is to reduce the specification to a set of easy-to-follow PCB routing rules. TI has performed the simulation and system design work to ensure SRIO interface requirements are met. This document describes the content of this SRIO implementation.

Contents

1 Prerequisites

The goal of the TCI6482 collateral is to make system implementation easier for the customer by providing the system solution. For this Serial RapidIO (SRIO) interface, it is not assumed that the system designer is familiar with SRIO, serializer-deserializer (SERDES) technology, or RF/Microwave PCB design. However, it is still expected that the PCB design work be supervised by a knowledgeable high speed digital PCB designer and an assumption is made that the PCB designer is using established high speed design rules.

2 TMS320TCI6482 Supported Serial RapidIO Devices

RapidIO is an industry-standard high-speed switched-packet interconnect. The RapidIO specification allows a device to connect to any other device, so long as the two devices conform to a common physical-layer specification. TI DSPs support connecting to any Serial RapidIO device that complies with the Serial RapidIO specification revision 1.2 or later.

3 Description of the Serial Rapid I/O Hardware Design Files

The SRIO Hardware Design files included with this report are described in Table 1.

Table 1. SRIO Hardware Design Files

File Name	Description
DSP_SRIO_Example.brd	Allegro 15.x design database file containing the PCB layout. This file can be viewed and edited using Cadence Allegro PCB design tools. It can also be viewed using the free Allegro viewer compatible with version 15.x databases. The free viewer can be downloaded from http://www.cadence.com.
DSP_SRIO_Example.dsn DSP_SRIO_Example.opj DSP_SRIO_Example.pdf	Reference design SRIO schematics in ORCAD design, project, and .pdf file formats. These schematics contain circuitry for the SRIO interface.

4 PCB Routing Rules

4.1 Minimum PCB Stackup

The minimum PCB stackup for routing the TMS320TCI6482 is a six-layer stackup as described in Table 2.

Table 2. Minimum PCB Stackup

Layer	Type	Description
1	Signal	Top Routing
2	Plane	Ground
3	Plane	Split Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing

Additional layers may be added as needed. All layers with SRIO traces must be able to achieve 100 ohms differential impedance.

Note: The provided sample board file shows a twelve-layer stackup, but not all of these layers are necessary to use the SRIO interface.

4.2 General Trace/Space and Via Sizes

The key concern for RapidIO signal traces is to achieve 100 Ohm differential impedance. This differential impedance is impacted by trace width, trace spacing, distance between planes, and dielectric material. Verify with a proper PCB manufacturing tool that the trace geometry for all SRIO traces results in exactly 100 Ohms differential impedance traces.

Of secondary concern is the insertion loss caused by the traces. Due to the skin effect, wider traces will have lower losses than narrower ones. Therefore, longer SRIO runs should use wider traces for lower loss. Layers in the stackup that are set to 100 Ohm differential impedance with wider traces may be less desirable for routing other signals. Table 3 shows recommendations for minimum trace width by SRIO signal run length.

Table 3. Minimum Trace Width

Signal Run Length, up to	Minimum trace width
10 in / 25 cm	4 mil / .1 mm
20 in / 50 cm	6 mil / .15 mm
30 in / 75 cm	8 mil / .2 mm

The TCI6482 sample PCB is routed using 4 mil traces and 4 mil minimum trace spacing. 100 Ohms differential impedance is achieved with 4 mil traces and 10 mil spaces on the Top and Bottom layers, and 4 mil traces with 5 mil spaces on internal layers. Escape and general SRIO routing vias have 8 mil holes with 18 mil pads. Micro and/or blind/buried vias are neither required nor prohibited.

The PCB BGA pad requirements for the TCI6482 device are documented by the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811a), available at www.ti.com. The TCI6482 is a 0.8 mm ball pitch part and should follow the 0.8 mm guidelines. The PCB BGA pad requirements for the SRIO link partner device should follow its manufacturer's guidelines.

4.3 Serial RapidIO Interface Routing Requirements

The approach used in this reference design for specifying suitable RapidIO routing breaks the physical connection down into three component pieces: receiver end, transmitter end, and interconnect. The receiver and transmitter end are the pieces closest to the packages of the connected devices. The receiver end goes from the BGA pads to the capacitors. The transmitter end is simply the BGA escape paths for the differential pairs. Those two pieces of the reference layout are designed to be copied exactly into the target board. The interconnect joins the receiver and transmitter ends, and it is not intended to be copied directly, as board placements will vary from the sample.

4.3.1 Receiver End

Figure 1 below shows the connection on the receiver end. The trace from the BGA pad to the capacitor pad must be on the top layer. On the other side of the capacitor, it is recommended to via to another layer. The BGA breakout should be implemented exactly as shown. The trace widths and separation should be altered based on the board stackup to meet the 100Ω differential impedance requirement. Also, traces may be necked down to escape the BGA, if necessary.

An 0402 or smaller size, 0.1µf capacitor is recommended for AC coupling of the data lines.

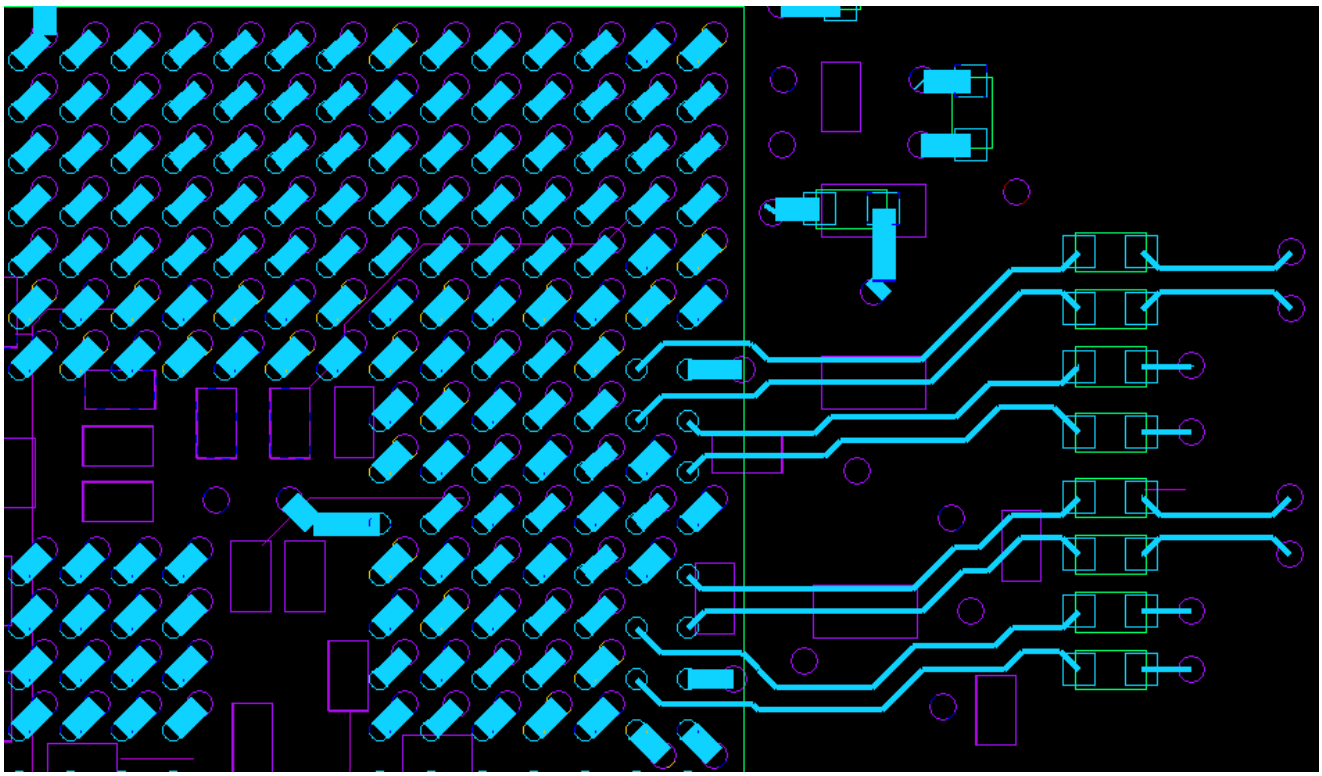

Figure 1. Receiver END BGA Breakout

4.3.2 Transmitter End

Figure 2 below shows the connection on the transmitter end. This trace may be on any signal layer besides the top. Internal layers are recommended for their superior shielding characteristics. The BGA breakout should be implemented exactly as shown. The trace widths and separation should be altered based on the board stackup to meet the 100Ω differential impedance requirement. Also, traces may be necked down to escape the BGA, if necessary.

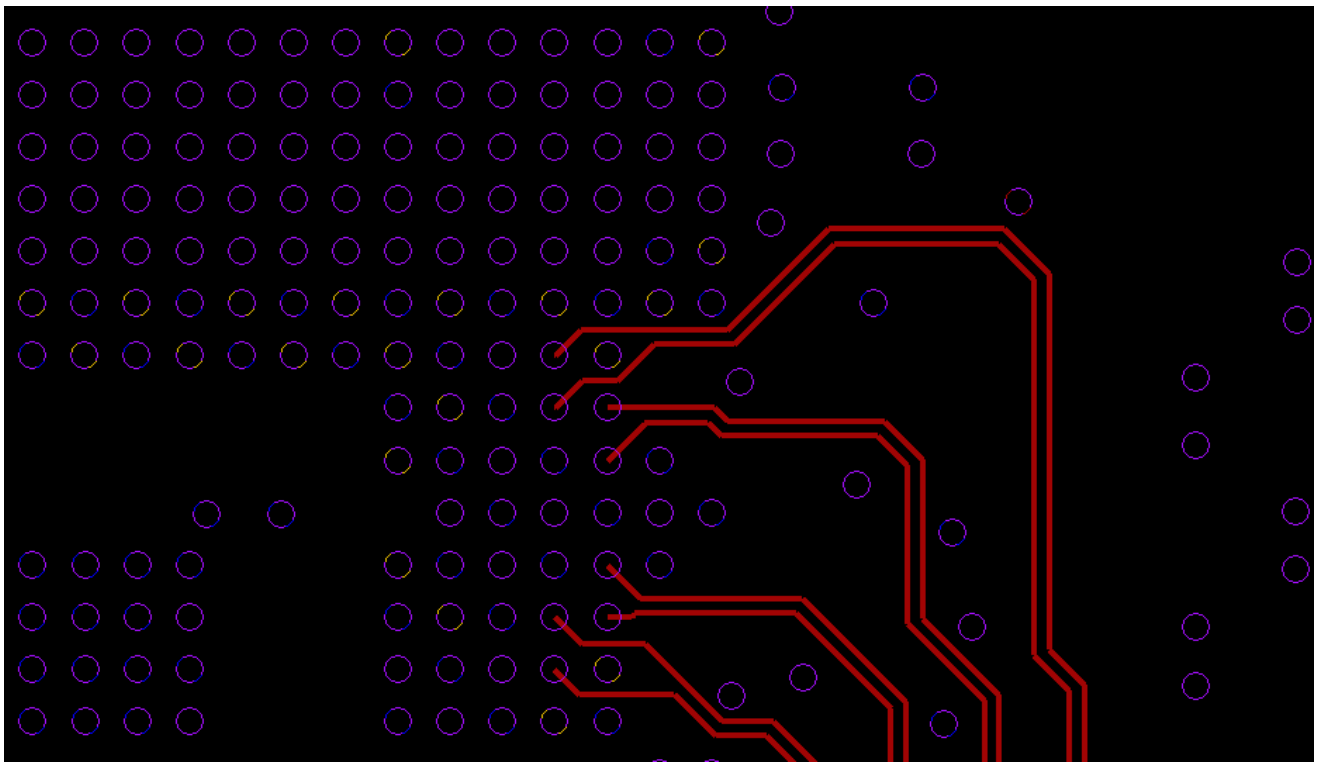

Figure 2. Transmitter End BGA Breakout

4.3.3 Interconnect

The geometry of the traces to link the transmitter and receiver ends is determined by the placement in the target system. Therefore, it is not possible to specify an exact layout for the interconnect. Instead, the trace may be placed as required, so long as it meets the following requirements:

- Edge-coupled, matched-length (± 50 mils) differential pair.
- No stubs.
- No more than 30 inches (75cm) pin-to-pin, for 8-mil (.2mm) wide traces over FR4 material.
- 100 Ω differential impedance.
- No more than 3 sets of vias (not including via for BGA breakout on transmit end).
- Other signals are separated by at least 2x the differential spacing.
- Internal layers are strongly preferred. Avoid top and bottom layers.
- If connectors are used, they must be of a suitable 100 ohm differential-impedance, high-speed type, and count as 1” of trace for each connector pair.
- If cabling is used, it must be of a suitable controlled-impedance type (100 ohm differential or 50 ohm single ended), and counts as 1" of trace for each 1' of cable.
- If a mid bus probe is used, it must follow both TI’s and the probe manufacturer’s guidelines, and counts as 2” of trace.

4.3.4 Length Matching

If the SRIO peripheral will be used in 1x mode, then there is no lane-to-lane length matching requirement.

If the SRIO peripheral will be used in 4x mode, then:

- All TX lanes connected to a device must all be +/- 5 inches (12.5 cm) in length from each other.
- All RX lanes connected to a device must all be +/- 5 inches (12.5 cm) in length from each other.
- There is no requirement that the TX lengths match the RX lengths.

4.3.5 Mid Bus Probe (Optional)

A mid bus probe can be used to observe traffic flowing down a link. Because the probe requires a special attachment point, it can degrade signal quality. The following rules must be observed to include a mid bus probe:

- Follow the Probe manufacturer's guidelines for probe pads and layout.
- If the stubs can be kept under 250 mils (6.35 mm) then connecting the probe lands as stubs to the transmission line is acceptable.
- If the stubs cannot be kept under 250 mils (6.35 mm) then the probe lands should be connected in-line with the rest of the transmission line.

4.3.6 Connectors (Optional)

Any connectors used must be controlled impedance (50 Ohm single ended or 100 Ohm differential) and suitable for microwave transmissions. Suitable connectors are typically categorized as "backplane" type connectors. The connectors should have less than 1 dB insertion loss below 6 GHz. Some suggested connectors are:

- CN074 – AMC Connector
- Tyco Z-DOK
- Tyco Z-PAK HM Zd

4.3.7 Cabling (Optional)

Any cabling used must be controlled impedance (50 Ohm single ended or 100 Ohm differential) and suitable for microwave transmissions. Recommended cable types are listed below:

- 50 Ohm Coaxial – Commonly used with SMA connectors, 4 cables required for 1x link, 16 for 4x link
  - q RG142
  - q RG316
  - q RG178
- Infiniband – assembled cables available in 1x and 4x widths

4.4 Power Supply Requirements

The power supply and bypassing requirements for SRIO are documented as part of the *TMS320TCI6482 Design Guide and Comparisons to TMS320TCI100* (SPRAAC7B).

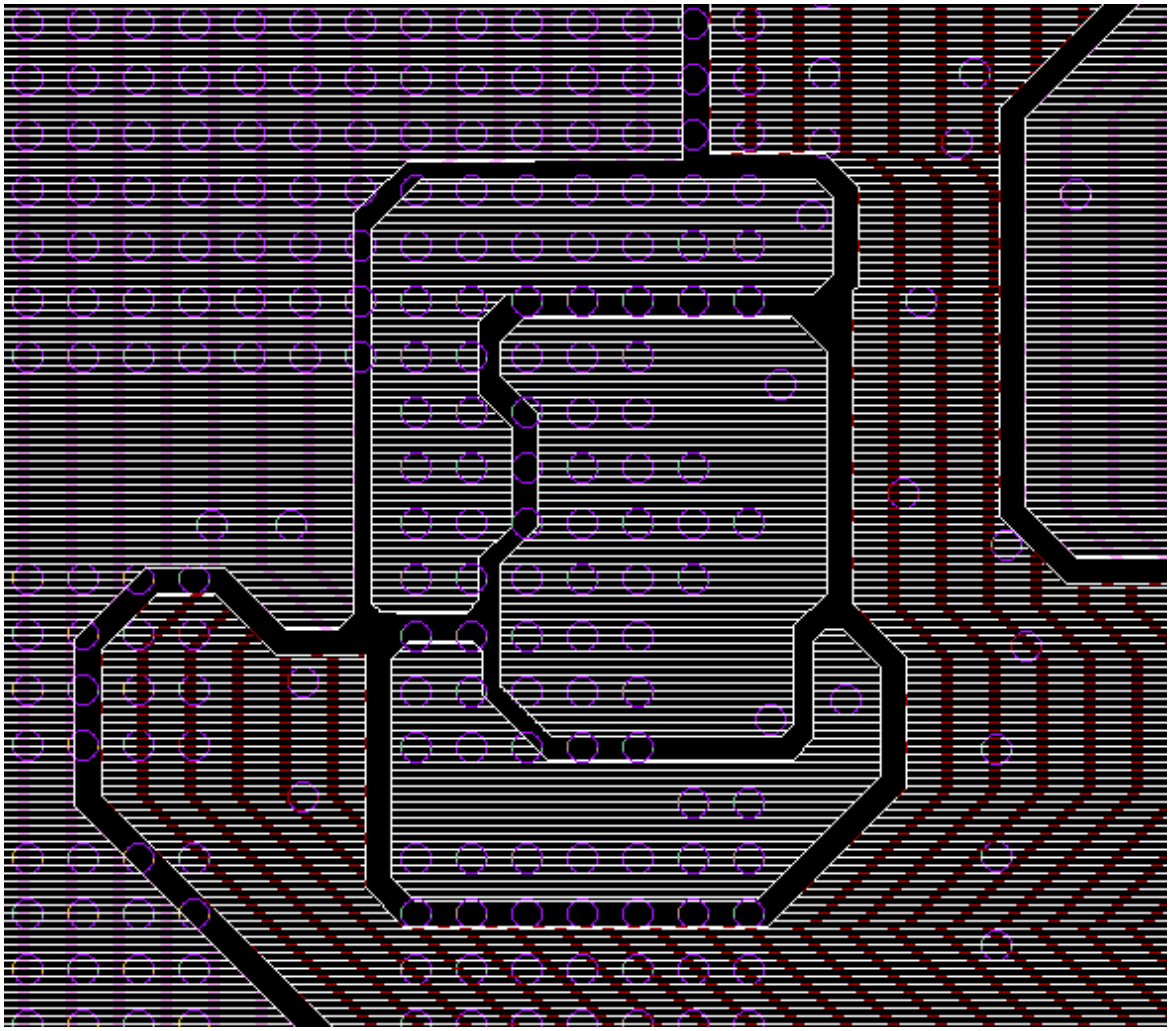

Figure 3. Power Plane Splits

5 Device Settings

Some of the SERDES register values should be set based on parameters from the physical PCB. Others are not dependent on the PCB, but are set based on the SRIO electrical specification. The following sections describe the recommended settings for the receivers and transmitters. More information about these registers can be found in the *TMS320TCI648x DSP Serial Rapid I/O User's Guide* (SPRUE13).

5.1 Receive Channel Configuration

Table 4 lists the recommended settings for receiver channels that can be set in the SERDES Receive Channel Configuration Registers (SERDES_CFGRXn_CNTL).

Table 4. SERDES Receive Channel Configuration Register Settings

Bits	Field	Setting	Description
19:22	EQ	0001	Fully Adaptive Equalization
18:16	CDR	000	First Order. Sufficient for SRIO clocking scheme (asynchronous with low frequency offset)
15:14	LOS	00	Disabled. Loss of Signal detection not used in SRIO
13:12	ALIGN	01	Comma Alignment. SRIO uses comma alignment during lane initialization
10:8	TERM	001	Common point is 80% of VDDT. This is the appropriate setting for AC coupled lines
7	INVPAIR	0	Non-inverted – use when TXP connects to RXP and TXN connects to RXN
		1	Inverted – use when TXP connects to RXN and TXN connects to RXP (1)
6:5	RATE	00	Full – Use for 3.125 GHz and 2.5 GHz line rates
		01	Half – Use for 1.25 GHz line rate
4:2	BUS-WIDTH	000	10-bit. SRIO uses 10-bit character groups.
0	ENRX	0	Disabled – for unused lanes
		1	Enabled – for active lanes

(1) On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both

5.2 Transmit Channel Configuration

Table 5 lists the recommended settings for transmitter channels that can be set in the SERDES Transmit Channel Configuration Registers (SERDES_CFGTXn_CNTL).

Table 5. SERDES Transmit Channel Configuration Register Settings

Bits	Field	Setting	Description
16	ENFTP	1	Fixed Phase. Required for 4x mode. Do not care in 1x mode.
15:12	DE	1000	-4.16 dB. Use for lines up to 10 inches (25cm)
		1001	-4.86 dB. Use for lines up to 14inches (35cm)
		1010	-5.61 dB. Use for lines up to 18 inches (45cm)
		1011	-6.44 dB. Use for lines up to 22 inches (55cm)
		1100	-7.35 dB. Use for lines up to 26 inches (65cm)
		1101	-8.38 dB. Use for lines up to 30 inches (75cm)
11:9	SWING	100	750mV. Use for lines up to 10 inches (25cm)
		101	1000mV. Use for lines up to 20 inches (50cm)
		111	1375mV. Use for lines up to 30 inches (75cm)
8	CM	1	Raised Common Mode. Helpful in preventing signal distortion at SWING amplitudes over 750mV
7	INVPAIR	0	Non-inverted – use when TXP connects to RXP and TXN connects to RXN
		1	Inverted – use when TXP connects to RXN and TXN connects to RXP (1)
6:5	RATE	00	Full – Use for 3.125 GHz and 2.5 GHz line rates
		01	Half – Use for 1.25 GHz line rate
4:2	BUS WIDTH	000	10-bit. SRIO uses 10-bit character groups.
0	ENTX	0	Disabled – for unused lanes
		1	Enabled – for active lanes

(1) On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both

6 References

RapidIO specifications may be downloaded from the RapidIO Trade Association's web site, www.rapidio.org.

The *TMS320TCI648x DSP Serial Rapid I/O User's Guide* (SPRUE13) explains the functional operation of the SRIO peripheral.

The *TMS320TCI6482 Design Guide and Comparisons to TMS320TCI100* (SPRAAC7B) contains information related to powering, clocking, and configuring the TCI6482, including the SRIO peripheral.

The *High Speed DSP Systems Design Guide* (SPRU889) contains general guidance on many matters of high performance DSP system design.

The *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811a) provides guidance with respect to PCB design and Texas Instruments BGA packages. It contains PCB design rules, PCB assembly parameters, rework process, thermal management, troubleshooting tips plus other critical information.

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