Application Report
SPRAAF1A–November 2007

TMS320TCI6482 Power Consumption Summary

Douglas Harrington *Digital Signal Processing Solutions*

ABSTRACT

This application report discusses the power consumption of the Texas Instruments TMS320TCI6482 digital signal processor (DSP). The power consumption on the TCI6482 device is highly application-dependent; therefore, a power spreadsheet that predicts power consumption is provided along with this document. The power spreadsheet can be used for the purpose of modeling power consumption for user applications such as power supply design, thermal design, etc. To get good results from the spreadsheet, realistic usage parameters must be entered, see Section 3.1. The low-core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The data presented in this application report and accompanying spreadsheet was measured from devices at the maximum end of the power consumption for production devices. No production devices will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www-s.ti.com/sc/techlit/spraaf1.zip.

Table 1. Typical Activity

		Power at Frequency(1)		
Core Voltage	CPU Frequency	Internal Logic	I/O	Total
1.25 V	1000 MHz	1.97	1.12	3.10
1.2 V	850 MHz	1.67	1.07	2.74
1.2 V	720 MHz	1.52	1.05	2.57

(1)Assumes the following conditions: 50% CPU utilization; DDR2 at 20% utilization (250 MHz), 50% writes, 32 bits, 50% bit switching; EMIFA at 40% utilization (133 MHz), 50% writes, 64 bits, 50% bit switching; McBSP0/1 at 100 MHz, 10% utilization, 50% switching; VCP2 at 50% utilization; TCP2 at 20% utilization; EMAC, 1000 Mbps, RGMII, 50% utilization, 50% switching; SRIO 3.125, 4 lanes, 50% utilization, 50% switching; One 100-MHz Timer at 10% utilization; device configured for HPI32 mode, 50 MBps, 30% utilization, 50% writes, 32, 50% switching, with pull-up resistors on HPI pins; room temperature (25°C).

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1 Activity-Based Models

Power consumption for the TCI6482 DSP can vary widely depending on the use of on-chip resources. Therefore, the power consumption cannot be estimated accurately without an understanding of the DSP components in use, and the usage patterns for those components. By providing the usage parameters that describe how and what on the DSP is being used, accurate power consumption numbers can be obtained for power-supply and thermal analysis. By choosing the peripherals in use, you can determine expected power consumption for worse case utilization.

The power spreadsheet divides the power consumption into two major components: baseline power and activity power.

1.1 Baseline Power

Baseline power consumption is the power consumed that is independent of chip activity such as, static leakage power, and core power; core power includes clock tree, internal memory, on chip module power, etc. Baseline power is highly dependent on voltage, temperature, and central processing unit (CPU) frequency.

1.2 Activity Power

Activity power consumption is power that is consumed by all active parts of the DSP: CPU, enhanced direct memory access (EDMA), peripherals, etc. Activity power is independent of temperature, but highly dependent on activity levels of CPU, EDMA, peripherals, etc. In the power spreadsheet, activity power is separated by the major modules/peripherals within the device; therefore, individual module/peripheral power consumption can be estimated independently. This helps with tailoring power consumption to specific applications. The parameters used to determine the activity level of a module are frequency, mode, % utilization, % write, bus size, and % switching probability.

Module activity power consumption includes some necessary EDMA and CPU activity used to transfer data on-chip and off-chip when required. The power consumption associated with EDMA and CPU activity were minimized to only show power consumption with respect to the module/peripheral tested.

2 Spreadsheet Parameters

The spreadsheet provides the configurable parameters, which allow you to estimate power consumption based on configured usage parameters. To ensure realistic results, take care to configure the spreadsheet accurately. For more details, see Section 3.1 of this document. The spreadsheet parameters are as follows:

- Frequency: The operating frequency of a module or the frequency of external interface to that module.
- Modes: Selects Ethernet media access controller (EMAC) mode (RGMII, GMII, RMII, or MII) and serial RapidIO® (SRIO) number of lanes.
- % Utilization: The relative amount of time the module is active or in use versus off or idle.
- % Write: The relative amount of time (considering active time only) the module is transmitting versus receiving.
- Bits: The number of data bits being used in a selectable-width interface.
- % Switch: The probability that any one data bit on the relative data bus will change state from one cycle to the next.

The TCI6482 has the capability to disable peripherals that are not being used. When a peripheral is disabled, its clock is gated and the peripheral is held in reset, thereby, reducing the power consumption of the device. The spreadsheet that accompanies this application report includes a field that allows you to disable unused peripherals, thus reducing the power consumption. For more information on disabling or enabling the peripherals on the device, see the device-specific data sheet.

2.1 Modules

The TCI6482 power estimation spreadsheet contains the following modules with adjustable parameters:

- CPU
- EMIFA
- SYSCLKOUT
- DDR2
- VCP2
- TCP2
- UTOPIA
- VLYNQ
- EMAC
  - RGMII
  - GMII
  - RMII
  - MII
- SRIO
- Timer[0:1]
- HPI
- RSA[0:1]

EDMA is not listed as a separate module because the module activity already includes any necessary EDMA activity used for memory-to-memory transactions only. For available peripherals configuration, see the *TMS320TCI6482 Communications Infrastructure Digital Signal Processor Data Manual* (SPRS246).

The current version of the power estimation spreadsheet does not include the PCI peripheral of the TCI6482 device. To estimate power consumption for the PCI, use the host port interface (HPI) by entering similar bus utilization and data throughput numbers.

3 Using the Power Estimation Spreadsheet

Using the power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. The following steps explain how to use the spreadsheet:

1. Choose the appropriate operating CPU frequency (700 MHz to 1000 MHz).
   a. Core and SRIO voltages are set based on the selected operating CPU frequency
      i. CPU = 851 MHz to 1000 MHz, core and SRIO voltages will be set to 1.25 V
      ii. CPU = 850 MHz or less, core and SRIO voltages will be set to 1.2 V
2. Choose the case temperature for which want to estimate power 0°C to 90°C
3. Enable the appropriate peripherals used for your application including the mode, frequency, and bus width for that peripheral, if necessary.
4. Fill in the appropriate peripherals or modules % utilization, % writes, and % switching

The spreadsheet takes the provided information and displays the details of power consumption for the chosen configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, i.e., the peripherals clock frequency out of allowed range, etc. For best results, the information should be entered from left to right starting at the top and moving downward.

3.1 Choosing Appropriate Values

The frequency and bits user values are determined by design and it will be clear what the correct values to enter are. You can disable modules in the spreadsheet that are completely unused and disabled from the peripheral configuration register by selecting the *Disabled* button/tab in the column labeled *Status*. The utilization, read/write balance, and bit switching require estimation and a good understanding of the user application to choose appropriate values.

3.1.1 Utilization

For modules, except CPU, utilization is simply the percentage of the time the module spends doing something useful, versus being unused or idle. For these peripherals, there are no varying degrees of use, so the value is just the average over time. For example, the external memory interface (EMIFA) performs read and writes one-quarter of the time, and has no data to move for the other three-quarters of the time though it continues to perform background tasks like refreshes; this is considered 25% utilization.

The CPU utilization is not as straightforward because there are varying degrees of use for the CPU. Here, 0% utilization means the CPU is active and does no useful work (NOP execution), whereas, 100% utilization is representative of a high activity condition with all eight functional units active every cycle making use of the software pipelined (SPLOOP) buffer hardware, with a maximum amount of data brought in every cycle. Few DSP algorithms achieve 100% utilization, because this requires every cycle to use all eight functional units, with no stalls. Even intense applications do not spend all of the time in such highly parallel loops. Time is typically also spent executing control code or less demanding algorithms. Control type code may only execute a few instructions in parallel, which significantly reduces the input/output (I/O) of the CPU, thus, reducing overall utilization. Since you must consider the balance of CPU use for the application, entering 100% utilization is not practical for real applications.

For example, an application that executes control code (estimated at 25% of CPU capability) half of the time, and very dense DSP code (estimated at 90% of CPU capability) the other half, would have an average utilization of about 60% (25% $\times$ 50% + 90% $\times$ 50%). If the balance were changed to 25% control code and 75% DSP code, the weighted average would be approximately 74% utilization (25% $\times$ 25% + 90% $\times$ 75%). If the 25%/75% relation is kept, but the DSP code does not fully use all the CPU resources (estimate now at 75% of CPU capability), then the overall utilization returns approximately 63% (25% $\times$ 25% + 75% $\times$ 75%). By using estimates of intensity and duration of blocks of code in the application, you can obtain an estimate of the overall CPU utilization.

System level issues may also reduce utilization. Though the spreadsheet accepts 100% utilization for all peripherals, this is not possible in reality. As memory and EDMA bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks and, therefore, do not achieve 100% utilization. In applications with a lot of memory and/or EDMA usage, enter the individual module utilization numbers keeping this overall limitation in mind.

3.1.2 % Writes

Peripherals that transmit as much as they receive have 50% writes; the spreadsheet assumes the remaining 50% of the time is spent on reads. In some applications, peripherals transmit in only one direction, or have a known balance of data movement. In these cases, the % writes option is not available for configuration. For the peripherals that have the % write configuration, 50% is a typical number that should be used.

3.1.3 %Switching

Random data has a 50% chance that any bit will change from one cycle to the next. Some applications may be able to predict this chance using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

3.2 Peripheral Enabling and Disabling

As mentioned earlier, the TCI6482 device provides the capability to enable only the peripherals that will be used. When a peripheral is disabled, the peripheral's clock is gated and the peripheral is held in reset.

A peripheral can be enabled or disabled in the spreadsheet from the column labeled *Status*. If the peripheral is disabled, the core and I/O power for the peripheral will be zero. If the peripheral is enabled with 0% utilization, the CV_{DD} supply reflects the delta power associated with enabling the peripheral versus the peripheral disabled.

Note: The power associated with enabling the peripherals will scale with CPU frequency; however, if the peripherals are driven by a fixed external clock source, the power will not scale unless you change the external clock source.

For more information regarding peripheral enabling, see the device-specific data sheet.

3.3 Graphs

The output/results graphs in the spreadsheet provide a visual breakdown of the power consumption for the following:

- Module core and I/O power consumption
- Total System-on-Chip (SoC) power consumption
  - Leakage power
  - Clocking power
  - Activity and dynamic power consumption
- Percent total SoC power consumption

4 Using the Results

The power data presented in this document and the accompanying spreadsheet is collected from devices considered at the maximum end of power consumption for a production device; no production units will have an average power consumption that exceeds the spreadsheet values. Therefore, the power consumption estimated by the spreadsheet is considered average power consumption over time, not instantaneous power. That is, transient currents may cause power to spike above the spreadsheet values for a small amount of time; however, over a long period, the observed average power consumption will be below the spreadsheet value. The spreadsheet value may be used for board thermal analysis and power supply design as a maximum long-term average.

4.1 Adjusting I/O Power Results

I/O power is dependent not only on the DSP and activity, but also on the load being driven. For loads with CMOS inputs, the power required to drive the trace dominates. For the data presented in the spreadsheet, the EMIFA, multichannel buffered serial port (McBSP), VLYNQ™ communications interface products, universal test and operations interface for ATM (UTOPIA), EMAC, SRIO, and Timer interfaces were loaded with approximately 4.5 inches of 50 Ω trace, with serial termination. Peripheral component interconnect (PCI) and HPI were loaded with approximately 2.5 inches of 50 Ω trace. For information regarding DDR2 bus loading topology, see *Implementing DDR2 PCB Layout on the TMS320TCI6482* (SPRAAA9).

To reduce 3.3-I/O power, with respect to HPI data buffers, the spreadsheet has an option to enable 3.3-I/O pull-up resistors for HPI data pins HD[31:0]. Be aware that enabling the pull-up resistor in the *Status* column significantly reduces the 3.3-I/O power consumption. Note that the PCI specification prohibits the use of any kind of termination resistor.

4.2 Spreadsheet Layout and Details

The following sections discuss the spreadsheet layout and details.

4.2.1 Baseline Section of Spreadsheet

The baseline power portion, of the results section of the power spreadsheet, consolidates the average power associated with leakage, and clock tree power. The clock tree power includes things like phase-locked loop (PLL) power and the power consumed by active clocks in the system. The Total SoC (mW) column sums up the rows for leakage, and clock tree power.

Note: The baseline portion of the srio-1.25/1.2 column shows the power consumption associated with enabling the SRIO macro. If the SRIO peripheral is disabled, the macro power will be zero.

4.2.2 Activity Section of Spreadsheet

The activity section of the spreadsheet contains the average power consumption associated with enabling a peripheral, along with power consumed due to peripheral activity. The activity level of a peripheral is defined by the peripheral frequency, % utilization, % writes, % switching, bus width, and peripheral mode.

When the peripheral is disabled, the core and I/O power associated with that peripheral equals zero. If the peripheral is enabled with % utilization equal to zero, the core power associated with the peripheral is equal to the power consumption of the module when enabled. When the module is enabled, the increased power consumption is dependent on the CPU frequency. Configuring the % utilization and other associated parameters increases the power of the core and I/O to reflect the power consumption when using the peripheral.

Note: The activity row for SRIO only shows the power associated with actively transmitting and receiving data.

To calculate total SRIO power, the baseline portions of the srio-1.25/1.2 supplies should be considered as well. The total SRIO power is calculated by the following equation:
srio_total_power = srio_core_activity(Cvdd-1.25/1.2) + srio_io_baseline(srio-1.25/1.2) + srio_io_activity(srio-1.25/1.2)

4.2.3 Totals SoC Section of the Spreadsheet

The totals section provides the total in each column for each power supply for Baseline plus Activity power. The total (mW) is equal to the total power for core and I/O all summed up, i.e., total device power.

4.2.4 Idle Power Section of Spreadsheet

The IDLE power is the power consumption associated with the CPU PLL configured. CPU executing an *IDLE* instruction, with all peripherals disabled.

5 Spreadsheet Example

Section 5.1 demonstrates an example on how to choose appropriate values for a particular application. The values used in this example may be imported into the spreadsheet by clicking the appropriate macro button.

5.1 Sample Application

The following example provides an estimation of power consumption when the DSP is being used to process data for a base station application. The spreadsheet provides the estimated total power for core and I/O using the parameters defined below as input.

In the spreadsheet, there is a button labeled *Base Station* that populates the spreadsheet with the following values.

- CV_{DD}: 1.25 V
- Case temperature: 25°C
- CPU: 1000 MHz, 50% utilization
  - Viterbi-Decoder Coprocessor 2 (VCP2) active with 8% utilization
  - Turbo-Decoder Coprocessor 2 (TCP2) active with 5% utilization
  - Rake/search accelerator (RSA0) active with 20% utilization
  - RSA1 active with 20% utilization
- SYSCLKOUT active = 133 MHz
- EMIFA (133 MHz, 25% utilization, 50% writes, 50% switching, 64-bits)
- DDR2 (250 MHz, 60% utilization, 50% writes, 50% switching, 32-bits)
- HPI (50 MB\sec, 30% utilization, 50% writes, 50% switching, 32-bits)
- McBSP0 disabled
- McBSP1 disabled
- SRIO active with 3 links at 3.125 Gbps with 15% utilization

Entering the appropriate values into the spreadsheet estimates the DSP total power for core and IO = 2.76 Watts.

6 Voltage Supply Reference List

Table 2. Power Pins

Group Name	Signal Name	Description
Cvdd-1.2/1.25	**CV_{DD}**	1.2-/1.25-V Core supply voltage
srio-1.2/1.25	**DV_{DDRM}**	1.2-/1.25-V I/O supply voltage (SRIO interface supply)
	DV_{DD12}	1.2-/1.25-V I/O supply voltage (main SRIO supply)
	AV_{DDT}	1.2-/1.25-V I/O supply voltage (SRIO termination supply)
	AV_{DDA}	1.2-/1.25-V I/O supply voltage (SRIO analog supply)
Dvdd-3.3	**DV_{DD33}**	3.3-V I/O supply voltage
ddr-1.8	**DV_{DD18}**	1.8-V I/O supply voltage (DDR2 Memory Controller)
	DV_{DDR} (1)	1.8-V I/O supply voltage (SRIO regulator supply)
Dvdd-1.5	**DV_{DD15}**	1.5-V I/O supply voltage for the RGMII function of the EMAC
	$V_{REFHSTL}$	(DVDD15/2)-V reference for HSTL buffer (EMAC RGMII)
pll-1.8	PLLV1	1.8-V I/O supply voltage for PLL1
	PLLV2	1.8-V I/O supply voltage for PLL2
	AV_{DLL1}	
	AV_{DLL2}	1.8-V I/O supply voltage

(1) The DV_{DDR} pin consumes negligible power (less than 10 mA). Therefore, the power impact of this pin is not reflected on the ddr-1.8 column of the spreadsheet.

7 References

- *TMS320TCI6482 Communications Infrastructure Digital Signal Processor Data Manual* (SPRS246)
- *Implementing DDR2 PCB Layout on the TMS320TCI6482* (SPRAAA9)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265