Application Note

High-Speed Interface Layout Guidelines

TEXAS INSTRUMENTS

ABSTRACT

As modern bus interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution.

Table of Contents

List of Figures

List of Tables

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1 Introduction

1.1 Scope

This application report can help system designers implement best practices and understand PCB layout options when designing platforms. This document is intended for audiences familiar with PCB manufacturing, layout, and design.

1.2 Critical Signals

A primary concern when designing a system is accommodating and isolating high-speed signals. As high-speed signals are most likely to impact or be impacted by other signals, they must be laid out early (preferably first) in the PCB design process to ensure that prescribed routing rules can be followed.

Table 1-1 outlines the high-speed interface signals requiring the most attention when laying out a PCB that incorporates a Texas Instruments™ System-on-Chip (SoC).

Table 1-1. Critical Signals

Signal Name	Description
DP	Universal Serial Bus (USB) 2.0 differential data pair, positive
DM	Universal Serial Bus (USB) 2.0 differential data pair, negative
SSTXP	SuperSpeed Universal Serial Bus (SSUSB) differential data pair, TX, positive
SSTXN	SuperSpeed Universal Serial Bus (SSUSB) differential data pair, TX, negative
SSRXP	SuperSpeed Universal Serial Bus (SSUSB) differential data pair, RX, positive
SSRXN	SuperSpeed Universal Serial Bus (SSUSB) differential data pair, RX, negative
SATA_RXP	Serial ATA (SATA) differential data pair, RX, positive
SATA_RXN	Serial ATA (SATA) differential data pair, RX, negative
SATA_TXP	Serial ATA (SATA) differential data pair, TX, positive
SATA_TXN	Serial ATA (SATA) differential data pair, TX, negative
PCIe_RXP	PCI-Express (PCIe) differential data pair, RX,positive
PCIE_RXN	PCI-Express (PCIe) differential data pair, RX,negative
PCIE_TXP	PCI-Express (PCIe) differential data pair, TX,positive
PCIE_TXN	PCI-Express (PCIe) differential data pair, TX,negative
HDMI_CLOCKx	High-Definition Multimedia Interface (HDMI) differential clock pair, positive or negative
HDMI_CLOCKy	High-Definition Multimedia Interface (HDMI) differential clock pair, positive or negative
HDMI_DATA2x	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
HDMI_DATA2y	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative

Table 1-1. Critical Signals (continued)

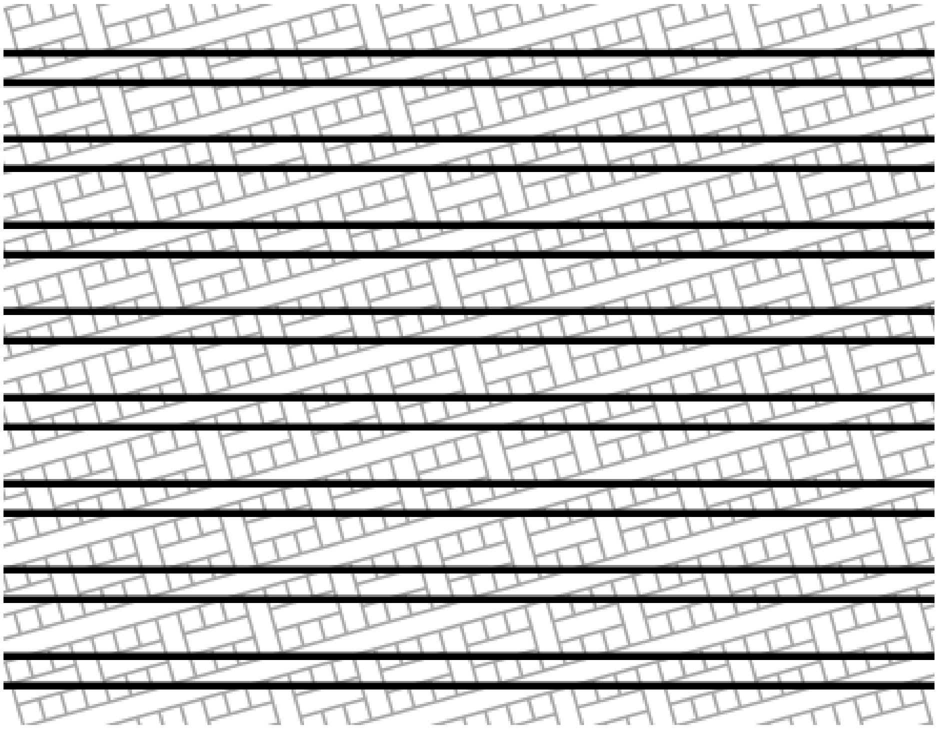
Signal Name	Description
HDMI_DATA1x	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
HDMI_DATA1y	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
HDMI_DATA0x	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
HDMI_DATA0y	High-Definition Multimedia Interface (HDMI) differential data pair, positive or negative
SGMII_TXP	Serial Gigabit Media Independant Interface (SGMII) differential data pair, TX, positive
SGMII_TXN	Serial Gigabit Media Independant Interface (SGMII) differential data pair, TX, negative
SGMII_RXP	Serial Gigabit Media Independant Interface (SGMII) differential data pair, RX, positive
SGMII_RXN	Serial-Gigabit Media Independant Interface (SGMII) differential data pair, RX, negative
CSI_RXCLKN	CSI Differential Receive Clock Input (negative)
CSI_RXCLKP	CSI Differential Receive Clock Input (positive)
CSI_RXN0	CSI Differential Receive Input (negative)
CSI_RXN1	CSI Differential Receive Input (negative)
CSI_RXN2	CSI Differential Receive Input (negative)
CSI_RXN3	CSI Differential Receive Input (negative)
CSI_RXP0	CSI Differential Receive Input (positive)
CSI_RXP1	CSI Differential Receive Input (positive)
CSI_RXP2	CSI Differential Receive Input (positive)
CSI_RXP3	CSI Differential Receive Input (positive)

2 General High-Speed Signal Routing

2.1 PCB Fiber Weave Mitigation

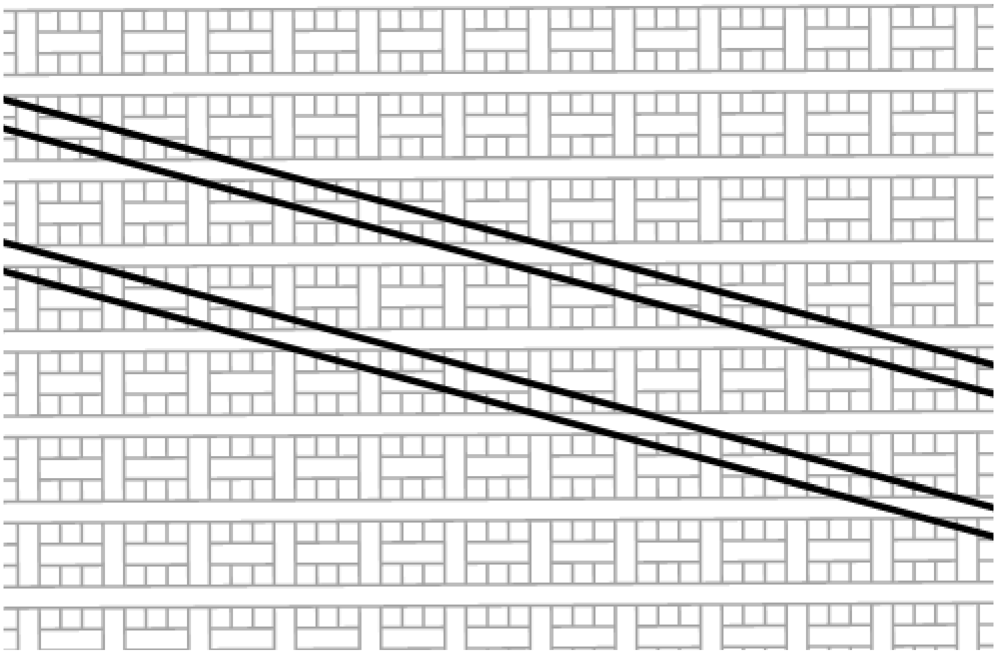
When routing differential signals across common PCB materials, each trace of the pair will experience different dielectric constants and corresponding signal velocities due to the differences in static permittivity (Ɛr) of the fiberglass weave (Ɛr is approximately 6) and epoxy (Ɛr is approximately 3) that comprise a PCB. As signals travel faster when Ɛr is lower, an interpair skew can develop if a signal in a differential pair travels over a higher ratio of fiberglass or epoxy than does its companion signal. This skew between the differential signals can significantly degrade the differential eye diagram as presented to the receiver, cause significant AC common-mode voltage noise, and cause EMI issues. The extent of this problem will depend on the bus speed, the length of the traces, the trace geometries, the type of fiberglass weave used, and the alignment of the traces to the weave pattern of a PCB. Problems from fiber weave alignment vary from board to board. This variance makes issues difficult to diagnose.

Figure 2-1, Figure 2-2, and Figure 2-3 show the three most common methods to minimize the impact of PCB fiber weave in a board design. The goal of each method is to ensure that both signals of the differential pair will share a relatively common Ɛr across the length of the pair routing.



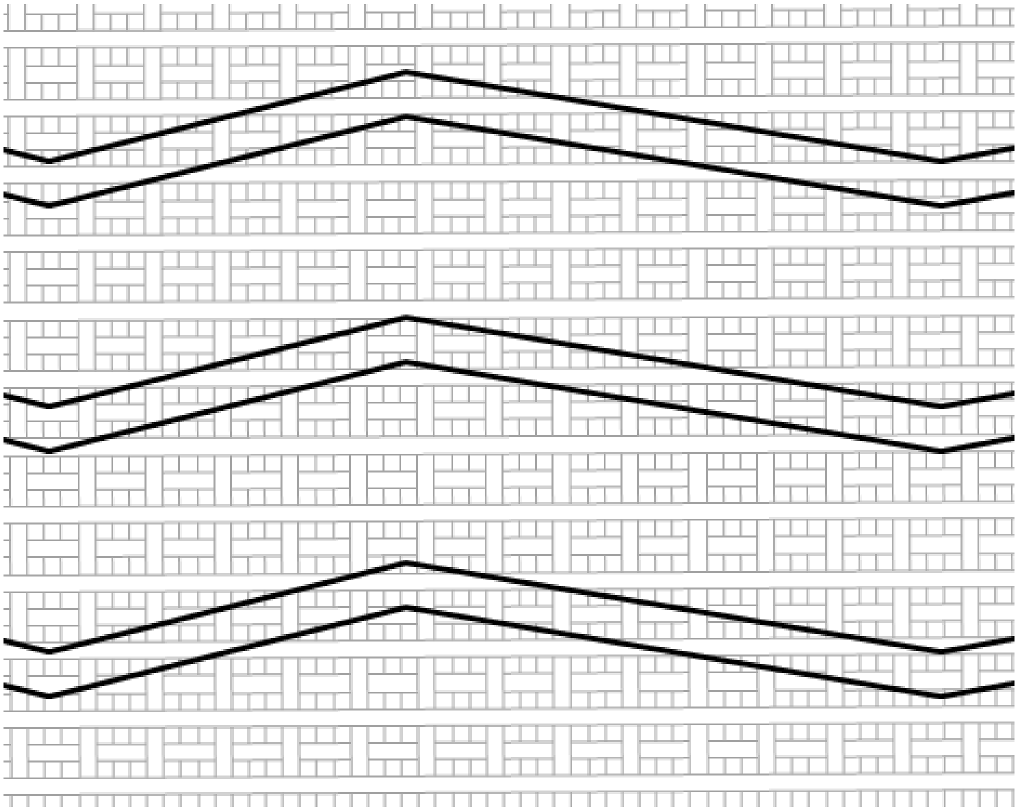
The entirety of the signaling image plane is rotated 10° to 35° in relation to the underlying PCB fiber weave. The PCB manufacturer can effect this rotation without making changes to the PCB layout database.

Figure 2-1. Rotation of the PCB Image



Only the high-speed differential signals are routed at a 10° to 35° angle in relation to the underlying PCB fiber weave.

Figure 2-2. Routing Angle Rotation



The high-speed differential signals are routed in a zig-zag fashion across the PCB.

Figure 2-3. Zig-Zag Routing

Because the ratio of fiberglass to epoxy is the primary contributor to the Ɛr disparity, choose a PCB style with a tighter weave, less epoxy, and greater Ɛr uniformity across longer trace lengths. Before sending your design out for fabrication, specify a PCB style that can best accommodate high-speed signals. For examples of common PCB styles, see Figure 2-4.

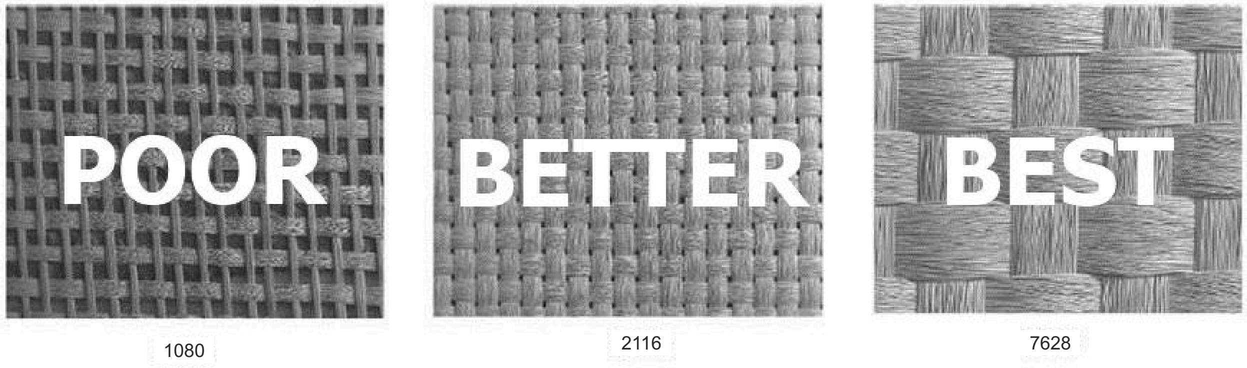


Figure 2-4. PCB Fiberglass Style Examples

2.2 High-Speed Signal Trace Lengths

As with all high-speed signals, keep total trace length for signal pairs to a minimum. For trace length requirements for each device, see Appendix A.

2.3 High-Speed Signal Trace Length Matching

Match the etch lengths of the relevant differential pair traces of each interface. The etch length of the differential pair groups do not need to match (that is, the length of the transmit pair does not need to match the length of the receive pair). When matching the intrapair length of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible. For more details, see Figure 2-5.

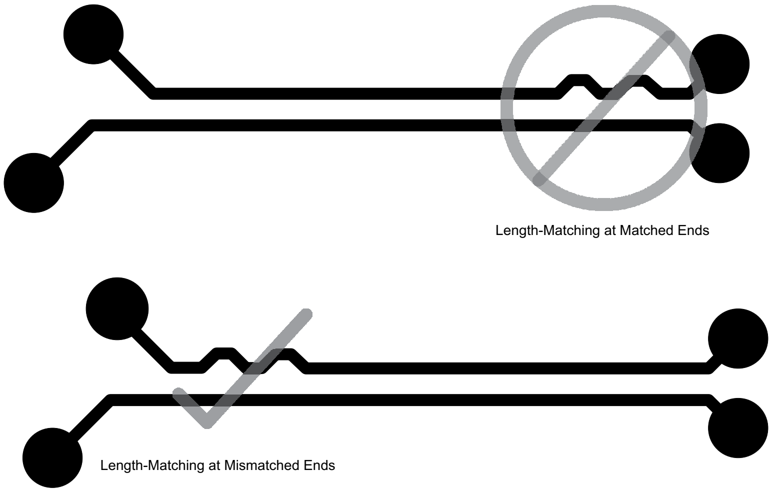


Figure 2-5. Length Matching

2.4 High-Speed Signal Reference Planes

High-speed signals should be routed over a solid GND reference plane and not across a plane split or a void in the reference plane unless absolutely necessary. TI does not recommend high-speed signal references to power planes.

Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void. This can result in the following conditions:

- Excess radiated emissions from an unbalanced current flow
- Delays in signal propagation delays due to increased series inductance
- Interference with adjacent signals
- Degraded signal integrity (that is, more jitter and reduced signal amplitude)

For examples of correct and incorrect plane void routing, see Figure 2-6 and Figure 2-7.

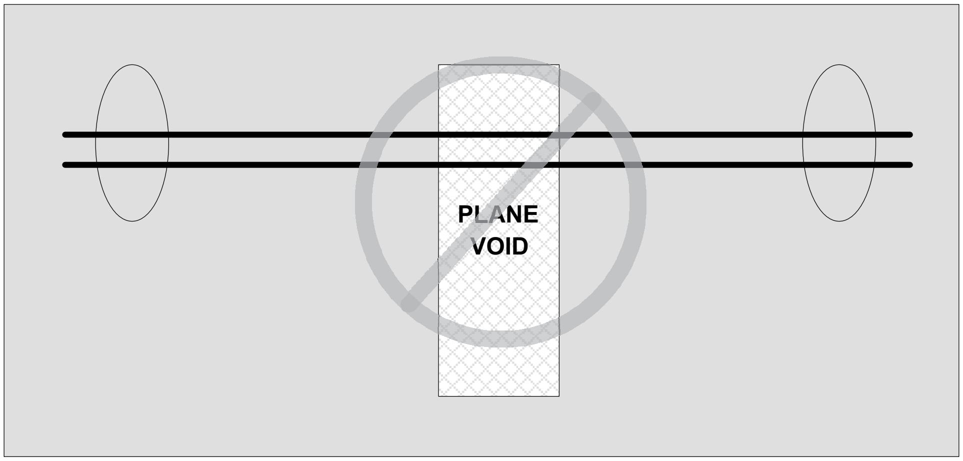


Figure 2-6. Incorrect Plane Void Routing

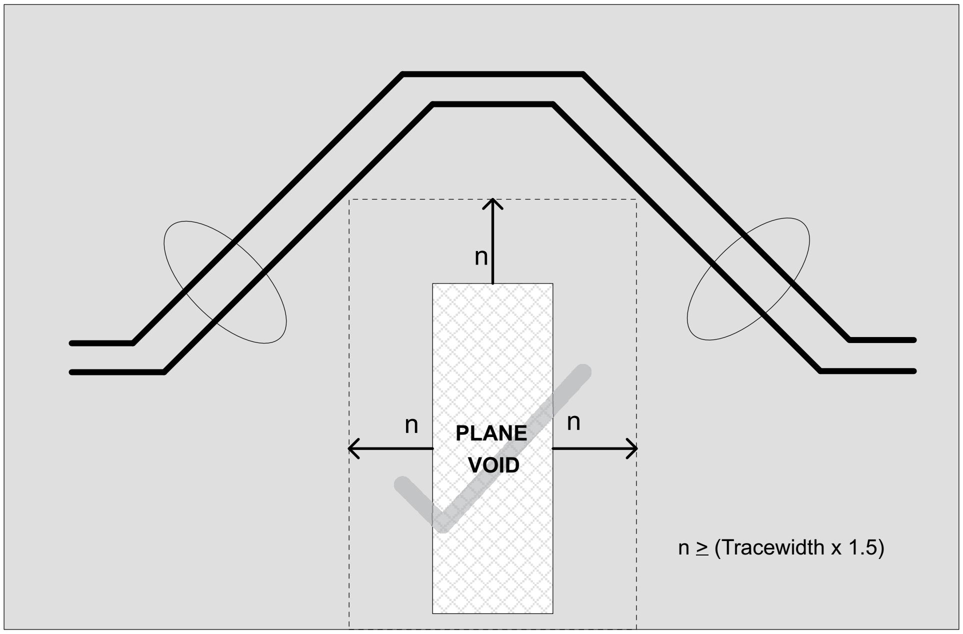


Figure 2-7. Correct Plane Void Routing

If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. These stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split. These capacitors should be 1 μF or lower and placed as close as possible to the plane crossing. For examples of incorrect plane-split routing and correct stitch capacitor placement, see Figure 2-8 and Figure 2-9.

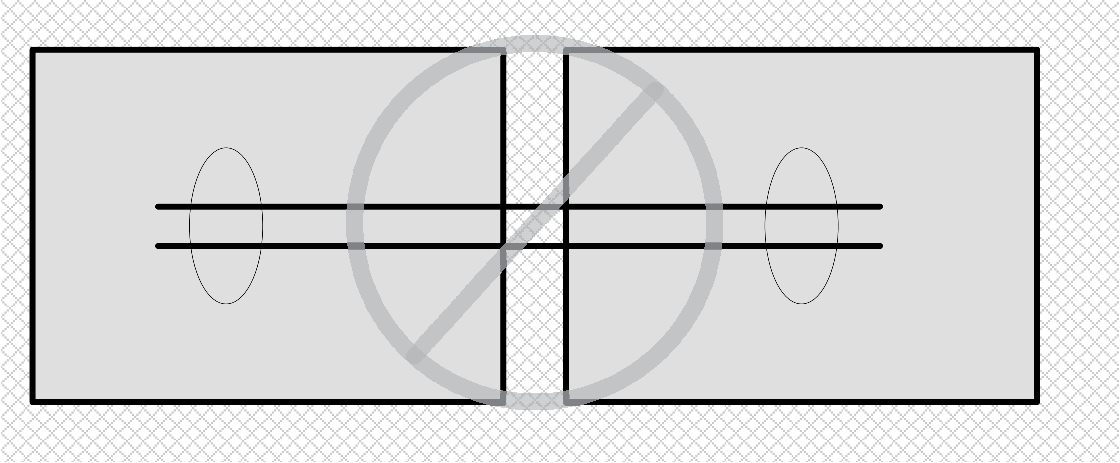


Figure 2-8. Incorrect Plane-Split Signal Routing

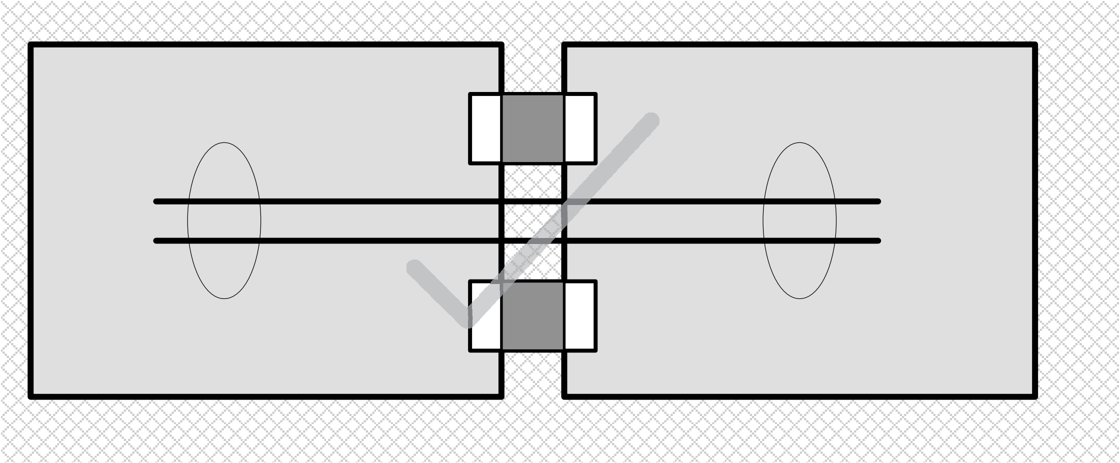


Figure 2-9. Stitching Capacitor Placement

When planning a PCB stackup, ensure that planes that do not reference each other are not overlapped because this produces unwanted capacitance between the overlapping areas. To see an example of how this capacitance could pass RF emissions from one plane to the other, see Figure 2-10.

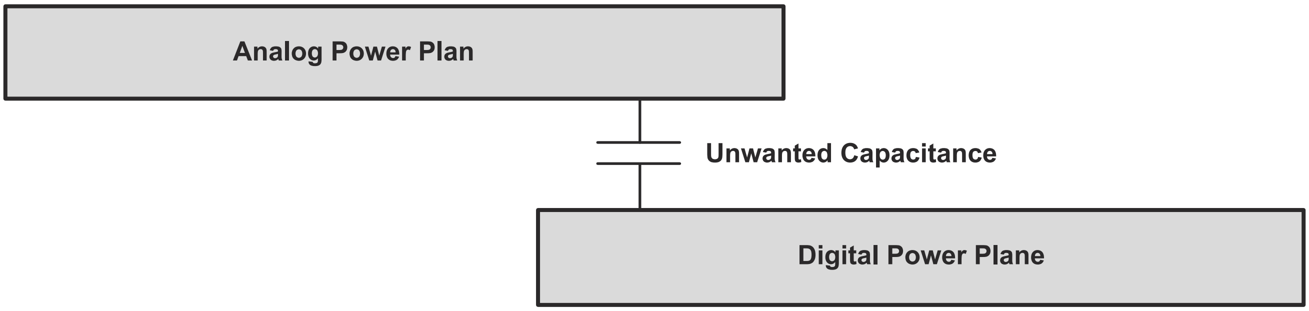


Figure 2-10. Overlapped Planes

The entirety of any high-speed signal trace should maintain the same GND reference from origination to termination. If unable to maintain the same GND reference, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (center-to-center, closer is better) of the signal transition vias. For an example of stitching vias, see Figure 2-11.

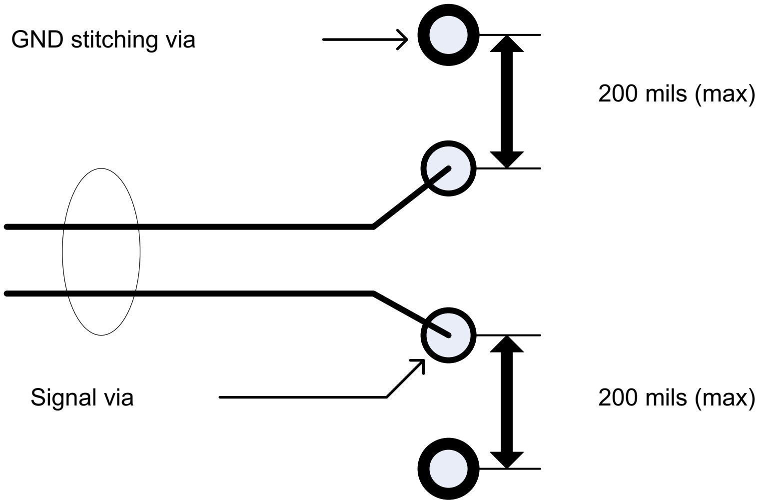


Figure 2-11. Stitching Vias

3 High-Speed Differential Signal Routing

3.1 Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of 5 times the width of the trace. This spacing is referred to as the 5W rule. A PCB design with a calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs abut a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to ensure proper isolation. For examples of high-speed differential signal spacing, see Figure 3-1 and Figure 3-2.

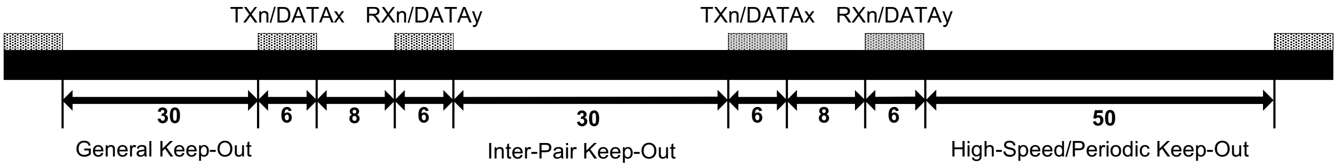


Figure 3-1. USB3/SATA/PCIe/HDMI/SGMII/CSI Differential Signal Spacing (mils)

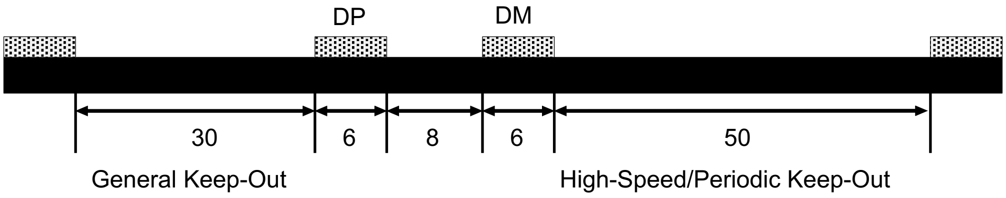


Figure 3-2. USB2 Differential Signal Spacing (mils)

3.2 High-Speed Differential Signal Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- After BGA breakout, keep high-speed differential signals clear of the SoC because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer. TI does not recommend stripline routing of the high-speed differential signals.
- Ensure that high-speed differential signals are routed ≥ 90 mils from the edge of the reference plane.
- Ensure that high-speed differential signals are routed at least 1.5 W (calculated trace-width × 1.5) away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the SoC BGA escape to avoid impedance mismatches in the transmission lines.
- Maximize differential pair-to-pair spacing when possible.

3.3 Symmetry in the Differential Pairs

Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short as possible and package break-out must occur within 0.25 inches of the package.

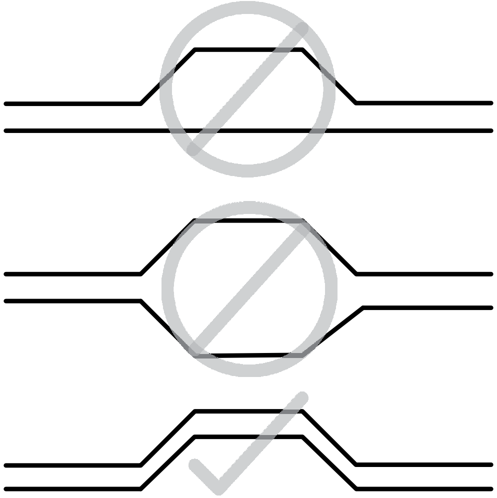


Figure 3-3. Differential Pair Symmetry

3.4 Crosstalk Between the Differential Signal Pairs

In devices that include multiple high-speed interfaces, avoiding crosstalk between these interfaces is important. To avoid crosstalk, ensure that each differential pair is not routed within 30 mils of another differential pair after package escape and before connector termination.

3.5 Connectors and Receptacles

When implementing a through-hole receptacle (like a USB Standard-A), TI recommends making high-speed differential signal connections to the receptacle on the bottom layer of the PCB. Making these connections on the bottom layer of the PCB prevents the through-hole pin from acting as a stub in the transmission path. For surface-mount receptacles such as USB Micro-B and Micro-AB, make high-speed differential signal connections on the top layer. Making these connections on the top layer eliminates the need for vias in the transmission path. For examples of USB through-hole receptacle connections, see Figure 3-4.

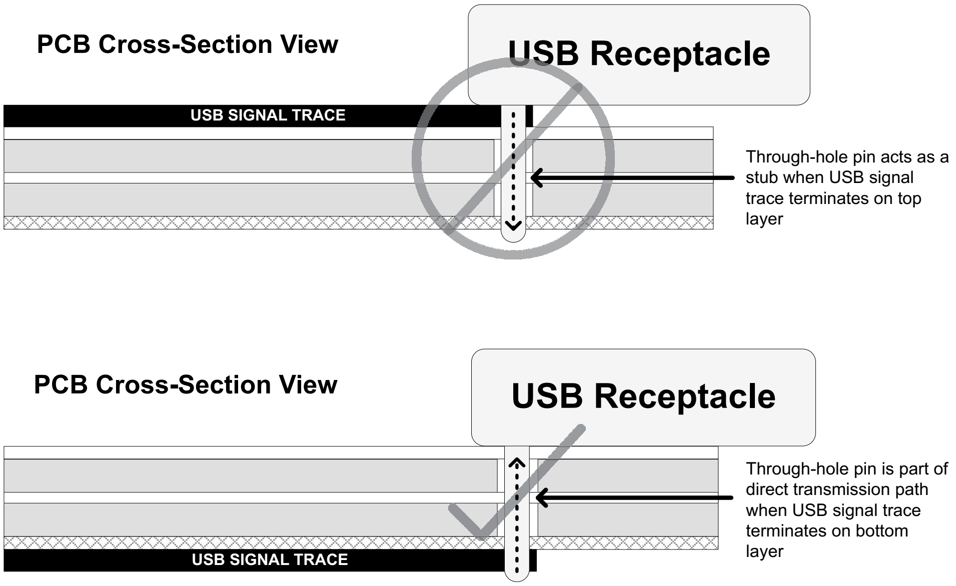


Figure 3-4. USB Through-Hole Receptacle Connection

3.6 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace and can appear as a capacitive and/or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as it travels through the via. Reduce the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. In most cases, the stub portion of the via present significantly more signal degradation than the signal portion of the via. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be back-drilled.

For examples of short and long via lengths, see Figure 3-5 and Figure 3-6.

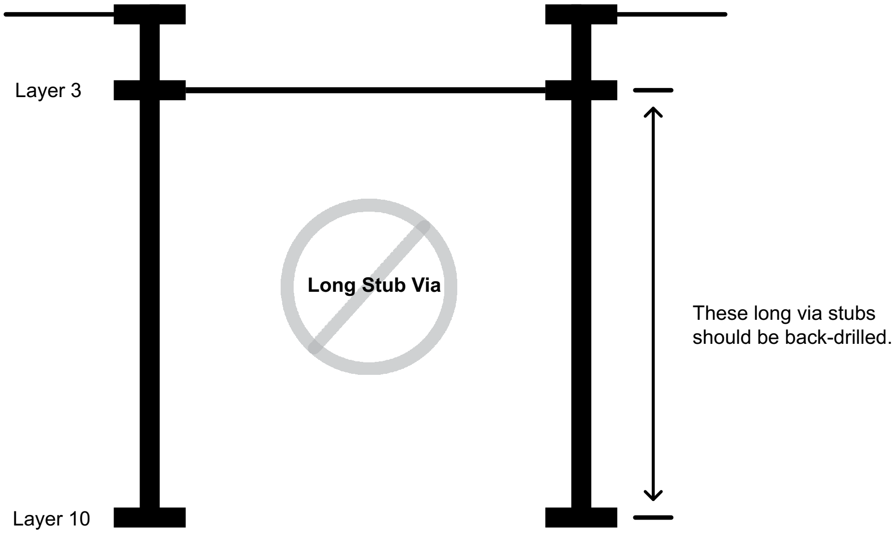


Figure 3-5. Via Length (Long Stub)

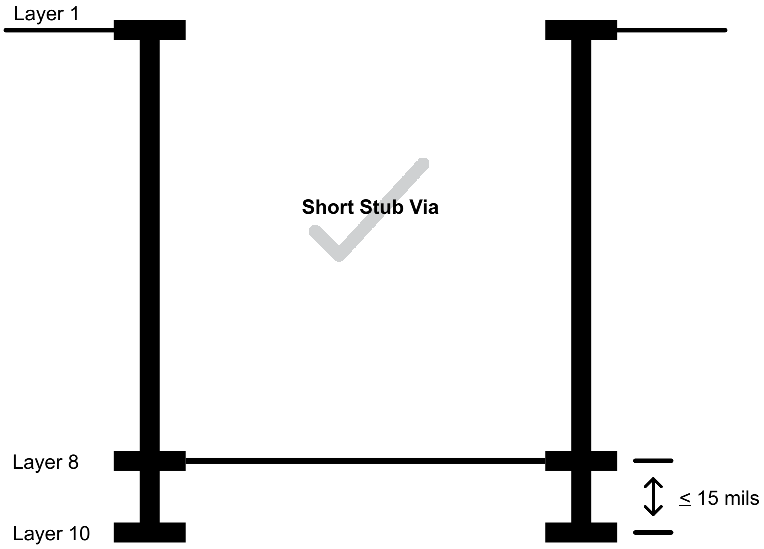


Figure 3-6. Via Length (Short Stub)

3.7 Back-Drill Stubs

Back-drilling is a PCB manufacturing process in which the undesired conductive plating in the stub section of a via is removed. To back-drill, use a drill bit slightly larger in diameter than the drill bit used to create the original via hole. When via transitions result in stubs longer than 15 mils, back-drill the resulting stubs to reduce insertion losses and to ensure that they do not resonate.

3.8 Increase Via Anti-Pad Diameter

Increasing the via anti-pad diameter reduces the capacitive effects of the via and the overall insertion loss. Ensure that anti-pad diameter for vias on any high-speed signal are as large as possible (30 mils provides significant benefits without imposing undue implementation hardship). The copper clearance, indicated by this anti-pad, must be met on all layers where the via exists, including both routing layer and plane layers. The traces connecting to the via barrel contain the only copper allowed in this area; non-functional or unconnected via pads are not permitted. For an example of a via anti-pad diameter, see Figure 3-7.

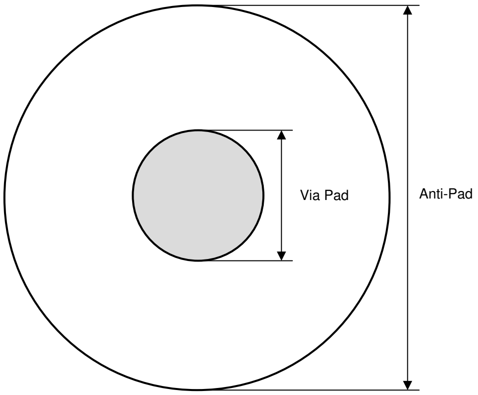


Figure 3-7. Anti-Pad Diameter

3.9 Equalize Via Count

If using vias is necessary on a high-speed differential signal trace, ensure that the via count on each member of the differential pair is equal and that the vias are as equally spaced as possible. TI recommends placing vias as close as possible to the SoC.

3.10 Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. TI strongly recommends using 0402 or smaller. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement, see Figure 3-8.

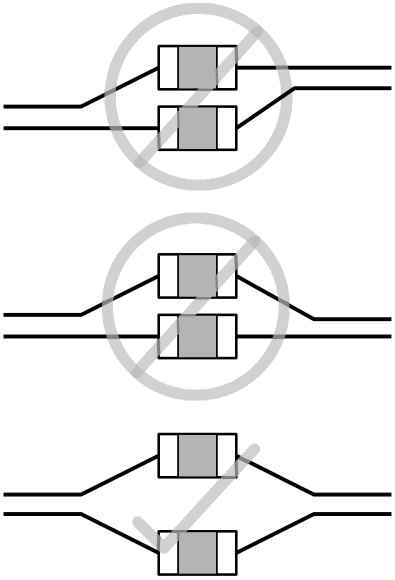


Figure 3-8. AC-Coupling Placement

To minimize the discontinuities associated with the placement of these components on the differential signal traces, TI recommends voiding the SMD mounting pads of the reference plane by 100%. This void should be at least two PCB layers deep. For an example of a reference plane voiding of surface mount devices, see Figure 3-9.

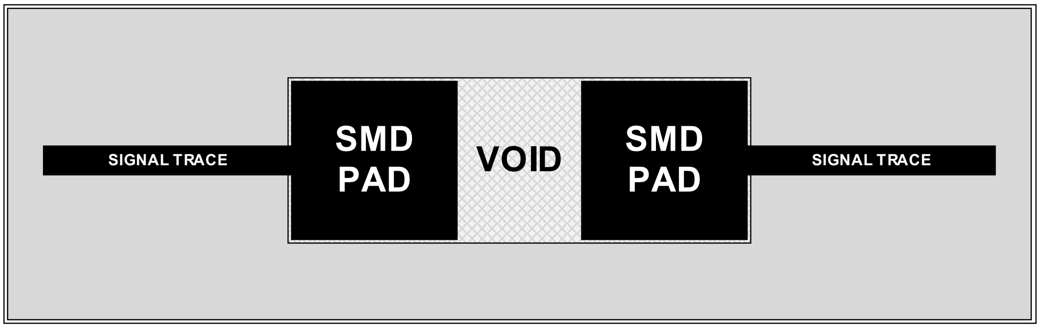


Figure 3-9. Reference Plane Voiding of Surface-Mount Devices

3.11 Signal Bending

Avoid the introduction of bends into high-speed differential signals. When bending is required, maintain a bend angle greater than 135° to ensure that the bend is as loose as a possible. For an example of high-speed signal bending rules, see Figure 3-10.

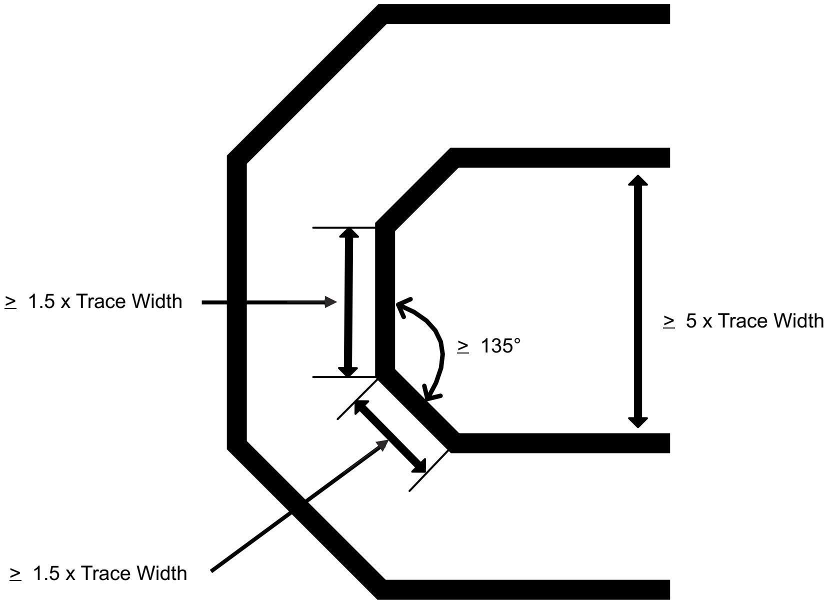


Figure 3-10. Signal Bending Rules

3.12 Suggested PCB Stackups

TI recommends a PCB of at least six layers. Table 3-1 provides example PCB stackups.

Table 3-1. Example PCB Stackups

6-LAYER	8-LAYER	10-LAYER
SIGNAL	SIGNAL	SIGNAL
GROUND	GROUND	GROUND
SIGNAL(1)	SIGNAL	SIGNAL(1)
SIGNAL(1)	SIGNAL	SIGNAL(1)
POWER/GROUND(2)	POWER/GROUND(2)	POWER
SIGNAL	SIGNAL	POWER/GROUND(2)
	GROUND	SIGNAL(1)
	SIGNAL	SIGNAL(1)
		GROUND
		SIGNAL

(1) Route directly adjacent signal layers at a 90° offset to each other
(2) Plane may be split depending on specific board considerations. Ensure that traces on adjacent planes do not cross splits.

3.13 ESD/EMI Considerations

When choosing ESD/EMI components, TI recommends selecting devices that permit flow-through routing of the USB differential signal pair because they provide the cleanest routing. For example, the TI TPD4EUSB30 can be combined with the TI TPD2EUSB30 to provide flow-through ESD protection for both USB2 and USB3 differential signals without the need for bends in the signal pairs. For an example of flow-through routing, see Figure 3-11.

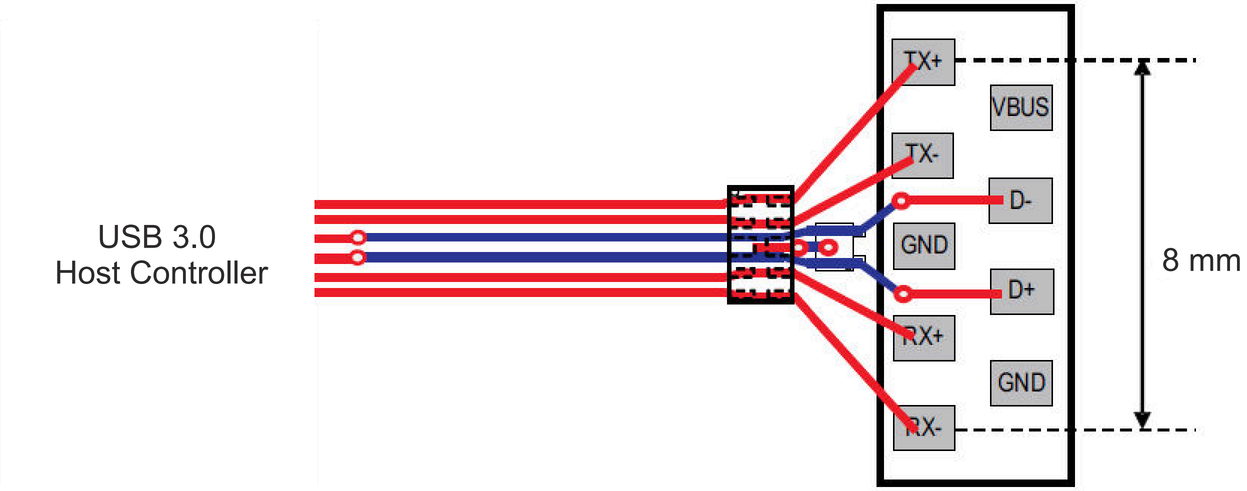


Figure 3-11. Flow-Through Routing

3.14 ESD/EMI Layout Rules

- Place ESD and EMI protection devices as close as possible to the connector.
- Keep any unprotected traces away from protected traces to minimize EMI coupling.
- Incorporate 60% voids under the ESD/EMI component signal pads to reduce losses.
- Use 0402 0-Ω resistors for common-mode filter (CMF) no-stuff options because larger components will typically introduce more loss that the CMF itself.
- Place any required signal pair AC coupling capacitors on the protected side of the CMF and as close as possible to the CMF.
- If vias are needed to transition to the CMF layer, ensure that the vias are as close as possible to the CMF.
- Keep the overall routing of AC coupling capacitors + CMF + ESD protection as short and as close as possible to the connector.

4 References

- Hall, Stephen H., and Garrett W. Hall. *High Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*. New York: Wiley, 2000.
- Johnson, Howard W., and Martin Graham. *High-speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ: Prentice Hall/PTR, 2003.
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- Johnson, Howard W., and Martin Graham. *High-Speed Digital Design: A Handbook of Black Magic*. Upper Saddle River, NJ: Prentice Hall/PTR, 1993. ISBN 0-13-395724-1

A Device Layout Parameters

Table A-1. AM335x/AM437x/AMIC1xx

Parameter	MIN	TYP	MAX	Unit
USB2.0 Tracelength (total)		4000	12000	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP/DM pair differential impedance	81	90	99	Ω
USB2.0 DP/DM pair common-mode impedance	40.5	45	49.5	Ω
Number of stubs allowed on any USB differential pair trace (total)			0	Stubs
Number of vias allowed on each USB2.0 differential trace (total)			4	Vias
Number of test points permitted on any USB differential pair trace (total)			0	Test Points
USB differential pair to clock or high-speed periodic signal trace spacing	50			Mils
USB differential pair to any other signal trace spacing	30			Mils

Table A-2. AM57xx/DRA7xx

Parameter	MIN	TYP	MAX	Unit
USB3.0 (SuperSpeed) Tracelength (Total)			3500	Mils
Serial-ATA (SATA) Tracelength (Total)			3500	Mils
PCI-Express (PCIe) Tracelength (Total)			4700	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
USB2.0 Tracelength (Total)		4000	12000	Mils
HDMI Tracelength (Total)			4000	Mils
Skew within any USB3/SATA/PCIe/HDMI differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			550	Mils
Skew between all PCIe TX pairs (Total)			550	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ω
USB2.0 DP or DM pair single-ended impedance	40.5	45	49.5	Ω
SuperSpeed SSRX or SSTX pair differential impedance	83.7	90	96.3	Ω
PCI-Express RX or TX pair differential impedance	90	100	110	Ω
PCI-Express RX or TX trace single-ended impedance	51	60	69	Ω
Serial-ATA RX or TX pair differential impedance	85	100	115	Ω
HDMI TMDS differential impedance	90	100	110	Ω
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3 differential trace (Total)			2	Vias
Number of vias allowed on any PCIe/SATA differential trace (Total)			0	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of vias allowed on each TMDS differential trace (HDMI)(Total)			0	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

Table A-3. KeyStone II - K2K, K2H, K2L, and K2E Devices

Parameter	MIN	TYP	MAX	Unit
USB3.0 (SuperSpeed) Tracelength (Total)			5500	Mils
Serial-ATA (SATA) Tracelength (Total)			5500	Mils
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
SuperSpeed Insertion Loss at 2.5 GHz (device to connector)	Refer to USB Specification			dB
USB2.0 Tracelength (Total)		4000	12000	Mils
Skew within any USB3/SATA/PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			550	Mils
Skew between all PCIe TX pairs (Total)			550	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ω
USB2.0 DP or DM pair common mode impedance	40.5	45	49.5	Ω
SuperSpeed SSRX or SSTX pair differential impedance	83.7	90	96.3	Ω
PCI-Express RX or TX pair differential impedance	90	100	110	Ω
PCI-Express RX or TX trace single-ended impedance	51	60	69	Ω
Serial-ATA RX or TX pair differential impedance	85	100	115	Ω
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on USB3 differential trace (Total)			2	Vias
Number of vias allowed on any PCIe/SATA differential trace (Total)			0	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

Table A-4. KeyStone II - K2G (66AK2G0x/66AK2G1x) Devices

Parameter	MIN	TYP	MAX	Unit
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
Skew within any PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			550	Mils
Skew between all PCIe TX pairs (Total)			550	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ω
USB2.0 DP or DM pair single-ended impedance	40.5	45	49.5	Ω
PCI-Express RX or TX pair differential impedance	90	100	110	Ω
PCI-Express RX or TX trace single-ended impedance	51	60	69	Ω
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any PCIe differential trace (Total)			0	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

Table A-5. AM65xx/DRA80xM

Parameter	MIN	TYP	MAX	Unit
USB3.1 GEN1 Tracelength (Total)			4000	Mils
PCI-Express (PCIe) Tracelength (Total)			4000	Mils
Serial Gigabit Media Independent Interface (SGMII) Tracelength (Total)			7500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
Skew within any USB3/PCIe/SGMII differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			6	ns
Skew between all PCIe TX pairs (Total)			1.5	ns
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ω
SuperSpeed SSRX or SSTX pair differential impedance	90.25	95	99.75	Ω
PCI-Express RX or TX pair differential impedance	90.25	95	99.75	Ω
SGMII RX/TX/RXCLK/TXCLK pair differential impedance	90.25	95	99.75	Ω
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3/PCIe/SGMII differential trace (Total)			2	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

Table A-6. AM64x

Parameter	MIN	TYP	MAX	Unit
USB3.1 GEN1 Tracelength (Total)			5500	Mils
PCI-Express (PCIe) Tracelength (Total)			5500	Mils
USB2.0 Tracelength (Total)		4000	12000	Mils
SuperSpeed Insertion Loss at 2.5GHz (device to connector)	Refer to USB Specification			dB
Skew within any USB3/PCIe differential pair			5	Mils
Skew between all PCIe RX pairs (Total)			6	ns
Skew between all PCIe TX pairs (Total)			1.5	ns
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
SuperSpeed SSRX or SSTX pair differential impedance	90.25	95	99.75	Ohms
PCI-Express RX or TX pair differential impedance	90.25	95	99.75	Ohms
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on any USB3/PCIe differential trace (Total)			2	Vias
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

Table A-7. AM62x (Preliminary Data)

Parameter	MIN	TYP	MAX	Unit
USB2.0 Tracelength (Total)		4000	12000	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
CSI Tracelength (Total)			10	Inches
CSI differential pair skew	Must satisfy mode-conversion S-parameters (1)			
CSI pair differential impedance	85	100	115	Ohms (2)
CSI single-ended impedance		50		Ohms
CSI lane skew			40	ps (3)
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of vias allowed on each CSI differential trace (Total)			2	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

1. Defined in MIPI D-PHY spec; includes sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22. General estimate is UI/50 (where UI = 400 ps for 1.25 GHz).
2. Because the MIPI signals are used for low-power, single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.
3. Defined by MIPI spec as 0.1 x UI (where UI = 400 ps for 1.25 GHz).

Table A-8. AM62Ax (Preliminary Data)

Parameter	MIN	TYP	MAX	Unit
USB2.0 Tracelength (Total)		4000	12000	Mils
Skew within any USB2.0 differential pair			50	Mils
USB2.0 DP or DM pair differential impedance	81	90	99	Ohms
CSI Tracelength (Total)			10	Inches
CSI differential pair skew	Must satisfy mode-conversion S-parameters (1)			
CSI pair differential impedance	85	100	115	Ohms (2)
CSI single-ended impedance		50		Ohms
CSI lane skew			40	ps (3)
Number of stubs allowed on any differential pair trace (Total)			0	Stubs
Number of vias allowed on each USB2.0 differential trace (Total)			4	Vias
Number of vias allowed on each CSI differential trace (Total)			2	Vias
Number of test points permitted on any differential pair trace (Total)			0	Test Points
Differential pair to clock or high-speed periodic signal trace spacing	50			Mils
Differential pair to any other signal trace spacing	30			Mils

1. Defined in MIPI D-PHY spec; includes sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22. General estimate is UI/50 (where UI = 400 ps for 1.25 GHz).
2. Because the MIPI signals are used for low-power, single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.
3. Defined by MIPI spec as 0.1 x UI (where UI = 400 ps for 1.25 GHz).

Revision History

Changes from Revision I (April 2022) to Revision J (February 2023) **Page**

- Removed (Preliminary Data) from AM64x. 16
- Added new AM62Ax (Preliminary Data).. 16

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