

OMAP35x 0.65mm Pitch Layout Methods

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ABSTRACT

It is easy to see from the unique look that the OMAP35x parts have a very unusual footprint. The OMAP35x ball grid array is designed with new technology called the Via Channel™ array, which makes significant printed circuit board (PCB) cost savings possible. If the PCB is routed correctly, this cost savings can be substantial. This application report explains how this is possible and shows several methods in which this can be done.

This document will explain methods to correctly route this BGA chip on a printed circuit board to take advantage of the features of the Via Channel array. It also shows how to route the entire OMAP35x chip in only two signal layers, using cheap PCB technology rules.

For more information regarding routing an OMAP35x system, see the *SDRAM Controller Subsystem (SDRC)* section in the device data sheet.

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1 OMAP35x PCB Layout Technology Summary

1.1 Via Channel Technology

Via Channel technology is a way of depopulating balls on the BGA chip package in a shape that makes it possible to have the vias concentrated in channels. This allows several advantages.

First, the via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the balls, since all the vias are placed in special areas called *via channels*. This makes PCB manufacturing less expensive because larger vias are possible.

Second, the vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of vias.

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Figure 1 shows the resulting OMAP35x footprint.

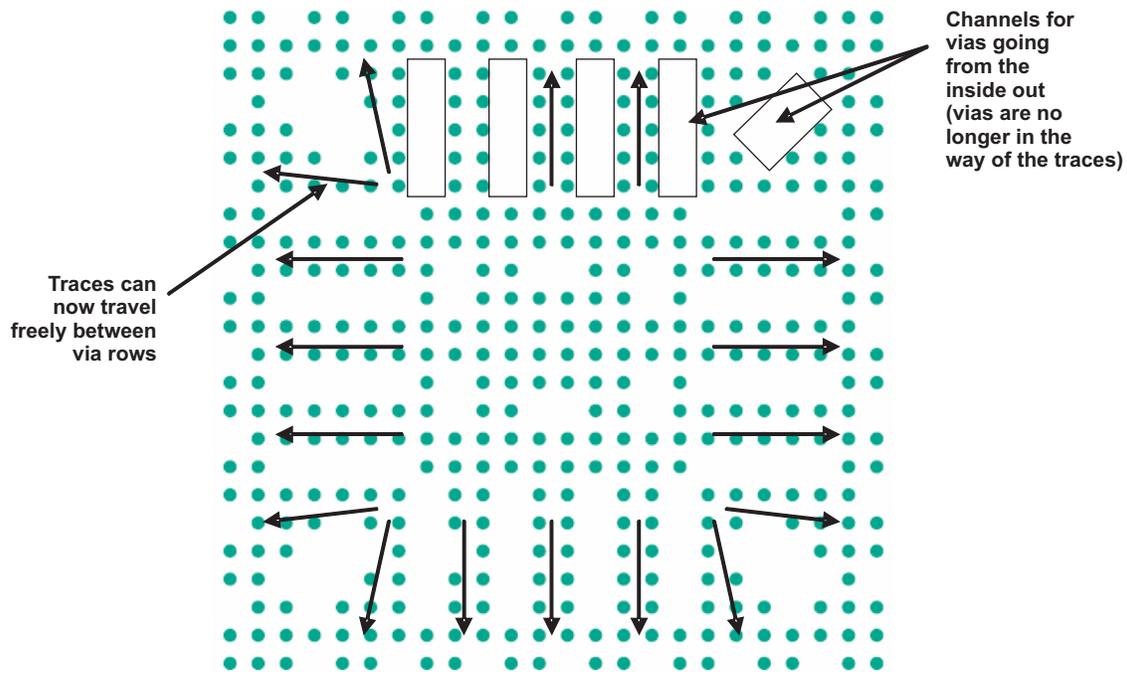


Figure 1. OMAP35x Footprint With Via Channel Array

The unique outer row routing and the via channel inner routing are two important parts of this technology on the OMAP35x.

1.2 Outer Row Routing

For the first two rows (from the outside in) of the BGA array, the balls have been arranged to allow wider traces than would otherwise be possible. The first row (the outside row) supports any size trace desired, since the trace simply comes from the PCB ball land and goes out on the PCB. Normally, the second row traces must be routed in between the first row of the PCB ball lands. On this package, the second row traces are routed through an open channel where the BGA ball has been removed to allow wider traces. The OMAP35x parts allow a 5 mil (0.125mm) trace/space in all areas, if routed correctly.

Figure 2 shows the first two rows of the OMAP35x package and how it is possible to route large 5 mil (0.125 mm) traces and spaces in the areas of removed balls.

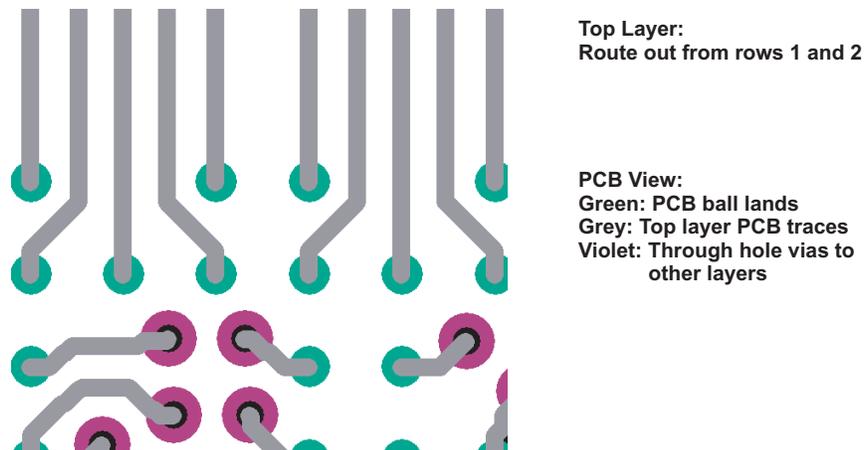


Figure 2. Outer Rows With Large Traces

1.3 Via Channel Inner Routing

Starting at the third row, as with any BGA package, vias are necessary. These vias are standard 18 mil (0.45mm) diameter vias with 8 mil (0.2mm) – 10 mil (0.25mm) finished hole sizes. The hole size is not important as long as the board can be built by your board shop with good yield.

As stated before, the vias are gathered in the via channels, so the only vias that need to be placed in between balls are some of the power vias in areas of ground or power copper pour. In this case, they have no regular via ring since they are located in an area of copper pour where all the surrounding balls share the same net. Since the via ring is larger than one that would normally fit in between these balls with the required clearance, the layout tool may flag a design rule check (DRC) error, however, this is a false warning since there is no risk of shorting to a nearby pad because they are all on the same net.

The rest of the vias need to be placed into the via channels as shown below. [Figure 3](#) shows how the vias are grouped in the via channels.

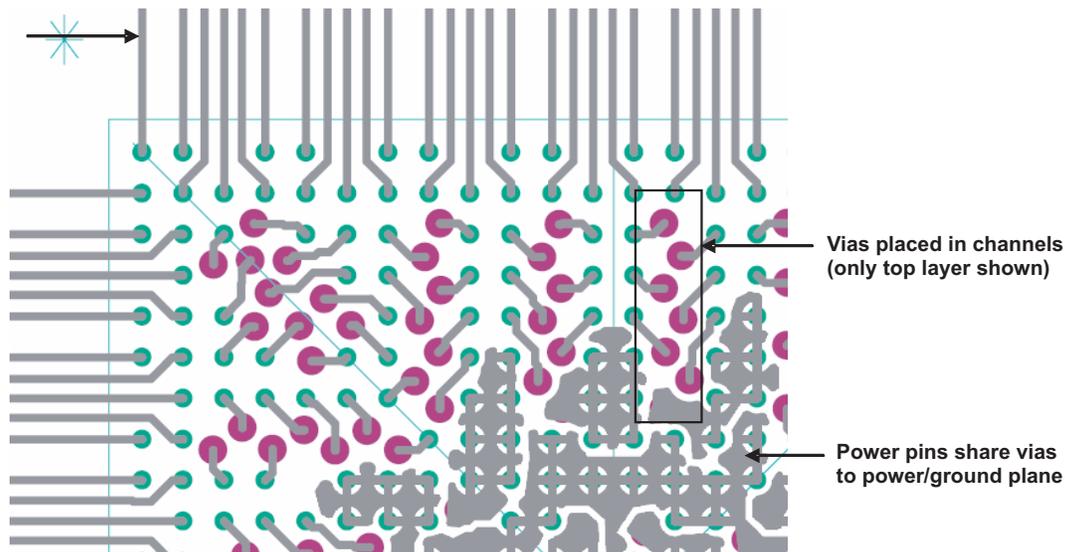


Figure 3. Vias in Via Channels

1.4 The Results

If done correctly, the PCB layout rules will be as follows:

- 5 mil (0.125mm) maximum trace/space
- 18 mil (0.45mm) maximum via diameter
- No blind, stacked, buried, or micro vias necessary
- Only two signal layers needed

These are the results of the BGA escape. This result in a PCB design should be even more cost effective than a 0.8mm pitch BGA part of equal pin count.

2 Methods

There are several easier methods to route the OMAP35x. They involve copying sections and repeating them to minimize effort.

Note that the gerbers and Allegro® files are available from your TI representative so that this work is already done for you.

2.1 Copy Channel Method

This method involves placing the vias in the channels, routing them, and copying each channel to other identical channels. If the largest PCB feature sizes (above) are used, trace placement is critical to allow copying from one to the other.

Here are the steps to successfully route a Via Channel array:

1. Build or download the footprint for this part from your PCB layout software. Note that there is a missing ball for orientation (at J5).
2. Use a metric grid. This allows the software layout tool to work more effectively with the metric defined footprint and will place traces on better defined locations.
3. Define the trace and space width to the maximum dimension (mentioned in [Section 1.4](#)) or smaller.
4. Route traces from the outside row out.
5. Route traces from the second row out through the missing ball areas in the first row as shown in [Figure 2](#). Three traces will fit through each opening. This allows wider traces and spaces than when routing in between balls.

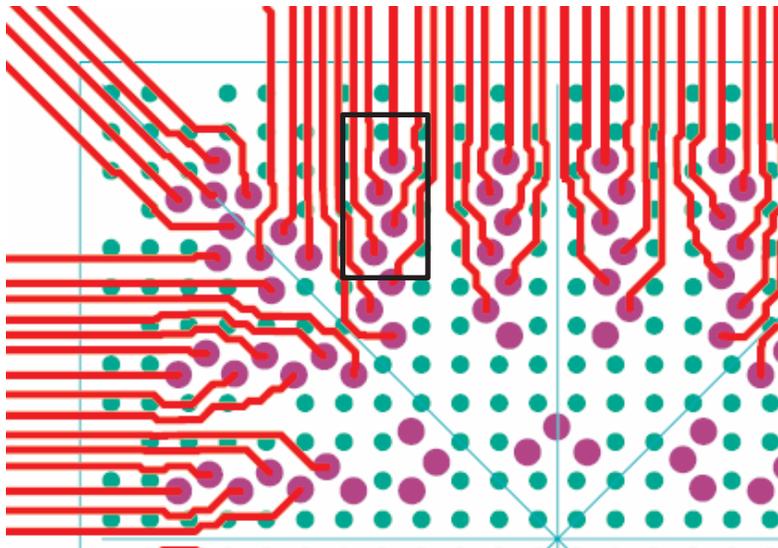
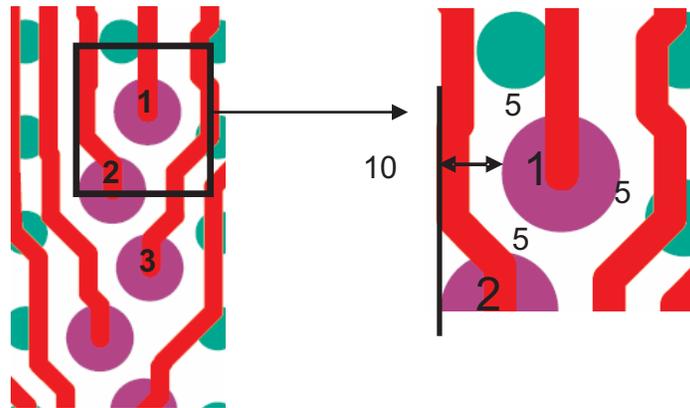


Figure 4. Area of the Exploded Drawings for [Figure 6](#) (top layer routing removed for clarity)

6. Create the vias to the diameter (mentioned in [Section 1.4](#)) or smaller and place them in the via channels. [Figure 5](#) shows how this is done.
 - a. Place the first outside via in one of the outside corners of the via channel.



- A This illustration shows an even closer look at the number 1 and 2 vias on the right of the illustration. The places where the number “5” appear show the distance from the number 1 via to the surrounding area in mils (5 mils = 0.125mm). It also shows how the number 2 via is placed as close as possible to the number 1 via, but offset by 10 mils (.250mm).

Figure 5. Expanded Area From [Figure 4](#)

- b. Place the next via adjacent to the first, as close as possible, but make sure the offset is only one space and one trace width wide (10 mils or .250mm). This enables the best routing for the traces going through the trace areas from vias 3-5.
 - c. The third via can go as close as possible to the second, and so on, until all the necessary vias are placed in a pattern like the one shown on [Figure 3](#), [Figure 4](#), and [Figure 5](#).
7. On an inner layer (or bottom), route from each via out to the outside of the package as shown making sure to put the traces as close as possible, as shown in [Figure 4](#). If you are using the maximum width trace/space dimension shown above, the placement will be tight. If this is done correctly, all but the outer two rows of the package will be routable in just one signal layer (except for the power and ground). If more than one layer is desired, feel free to switch any traces to another layer. [Figure 4](#) shows one routing example.
8. Connect the vias to the BGA ball pads on the top layer as shown in [Figure 3](#).
9. Copy this trace/via pattern to other identical via channels in a rotating copy method (going clockwise, for example, instead of mirroring from side to side).
10. Place the vias for the corners as shown in [Figure 3](#) and [Figure 4](#).
11. Route the traces out on the inner or bottom layer as shown in [Figure 4](#).
12. Connect the vias to the BGA ball pads on the top layer as shown in [Figure 3](#).
13. Copy this corner trace/via pattern to the other corners in a rotating copy method.
14. Place the power/ground vias as shown, both in between BGA ball pads and in the via channels. Placing one via for every 3-4 power/ground balls is ideal. Since the power/ground vias are placed only in locations in between four BGA ball pads that are on the same net, the warnings that the software layout tool may flag are not valid. The via becomes a hole in a copper pour area with no outside via diameter since the via would be completely engulfed in the copper pour. Since it is only adjacent to BGA ball pads in the same net, there is no possibility of shorting the via to the BGA ball pad; it is already shorted, being on the same net.

15. Form a copper pour area around the power/ground nets being sure to provide thermal reliefs around the BGA ball pads. These are not for thermal issues, but to ensure that the ball solder does not get wicked away (spread too thin) by the copper during reflow. This is a top layer copper pour. The lower power planes should match the same shape somewhat (if not solid) and be routed with heavy traces on the power plane. For signal integrity, it is essential to make the ground layer solid with no cuts. Cut the power plane only in a radial pattern (from the center out) once the pins are grouped. This improves signal integrity as most trace's return currents will not have to cross the gap in the power plane like they would if the cuts were perpendicular to the routing direction, which is typically from the inside of the chip out.

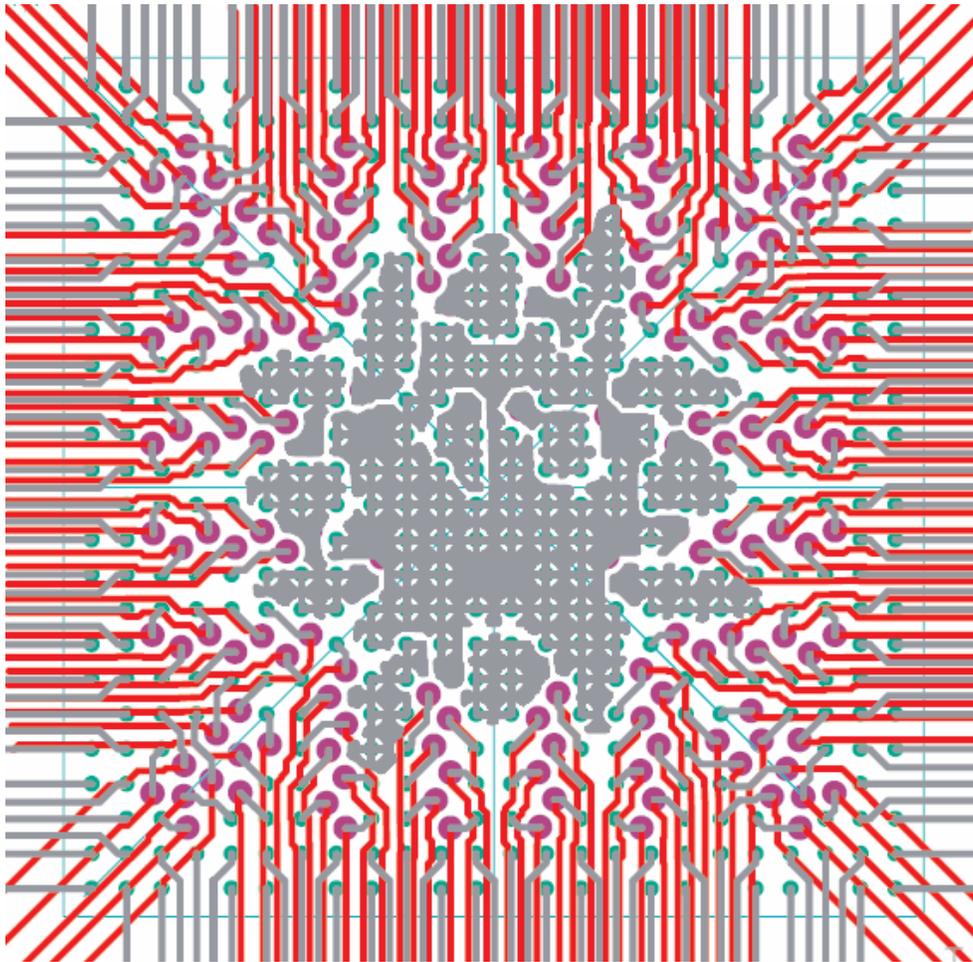


Figure 6. Completed Layout in Two Signal Layers (four overall layers)

It is easier to copy channels in a rotating fashion around the part than it is to copy them symmetrically. For example, when you finish routing the upper left via channel area, copy it to the area immediately to the right, and so on. Then rotate it 90° and continue down the right side, rotate it again, and continue around the bottom, etc. This tends to work better than trying to copy the upper sections and mirror them to the bottom sections.

2.2 *Quadrant Method*

This method is similar except that the first quadrant is routed by hand and then rotated/copied to the rest of the quadrants. Then proceed from step 14 in [Section 2.1](#).

3 References

- *SDRAM Controller Subsystem (SDRC)* section of the OMAP35x datasheet

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