

TMS320TCI6482 EMAC Performance Data

High-Performance and Multicore Processors

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Abstract

The TMS320TCI6482 integrates an EMAC module, which can be used to move data between the devices on the same Ethernet network. It supports 10/100/1000Mbps, and four types of interfaces to the physical layer device (PHY): MII, RMII, GMII and RGMII.

This document provides EMAC bandwidth data measured under various operating conditions. The CPU load relevant to the Ethernet packet transfer is also provided.

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1 Introduction

The TMS320TCI6842 integrates an EMAC (Ethernet Media Access Control) module, which can be used to move data between the device and another host connected to the same Ethernet network. It supports 10/100/1000 Mbps operation, and supports four types of interfaces to the physical layer device (PHY): standard media independent interface (MII), reduced pin count media independent interface (RMII), standard gigabit media independent interface (GMII) and reduced pin count gigabit media independent interface (RGMII). For more details about EMAC of TCI6482 please refer to [TMS320TCI648x DSP EMAC MDIO Module Reference Guide \(SPRUE12\)](#).

This document provides measured bandwidth data achieved on 1GHz TMS320TCI6482 EVM board.

There are two TCI6482 DSPs on the EVM. One of them connects to an MII PHY, which is used to measure 100Mbps operation performance; and the other connects to an RGMII PHY, which is used to measure 1000Mbps operation performance. 10Mbps operation is not measured, because it is rarely used.

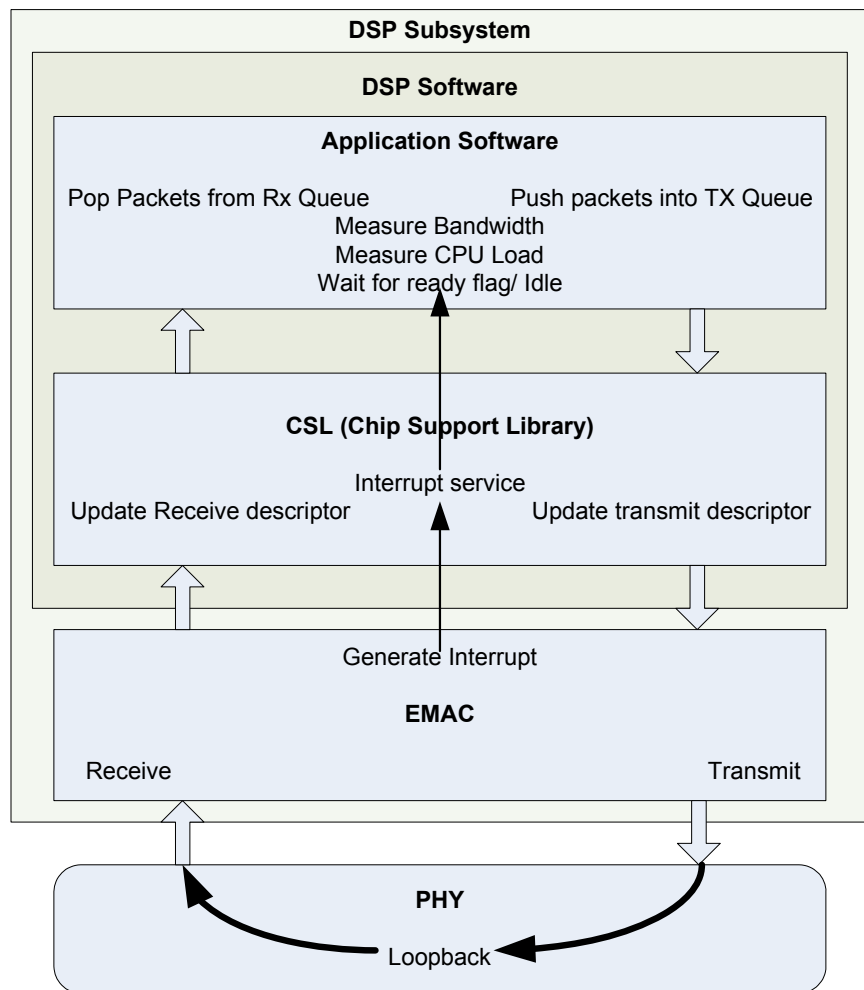
The CPU load relevant to the Ethernet packet transfer is also measured, which mainly includes:

- Filling transmit descriptor and starting transfer
- Filling receive descriptor and starting receiver
- Interrupt service for transmit, receive and status update

2 Measurement Methodology and Assumptions

Figure 1 describes the measurement system.

Figure 1 Block Diagram of the EMAC Performance Measurement System



The application software pushes the transmit packet into a Tx Queue; the CSL library is used to control the EMAC to transmit the packet from the TX Queue to PHY. The Ethernet packets are looped back in the PHY to the Rx port of the EMAC.

When the EMAC receives packets, it generates an interrupt to the CSL. Then, the CSL moves the received packet into the Rx Queue. The application software pops the Ethernet packet from the Rx Queue.

After packets are transmitted, the EMAC generates another interrupt, which triggers the CSL interrupt service routine to continuously transmit additional packets in the Tx Queue.

The bandwidth measured is only for the payload, the formula for calculating bandwidth is:

$$\text{Bandwidth} = (\text{packet payload}) * (\text{total packets transferred}) / (\text{total time used})$$

Generally, DSP core is faster than EMAC, so after DSP software finishes transmitting or receiving, it waits for next transfer. This period is the idle state. The idle time under this situation is measured; the CPU load is calculated based on the idle time.

$$(\text{CPU Load for EMAC}) = 100\% - (\text{idle time between transfer}) / (\text{total time used})$$

This test performs receive and transmit in parallel, so the bandwidth and CPU load measured is full duplex.

Other assumptions for the performance measurement include:

- 1GHz CPU clock is used.
- 64 Rx and 64 Tx descriptors buffer are used.
- The software is optimized with -o3 option.
- All data and code are in internal memory.
- 32KB L1D and 32KB L1P cache are used.

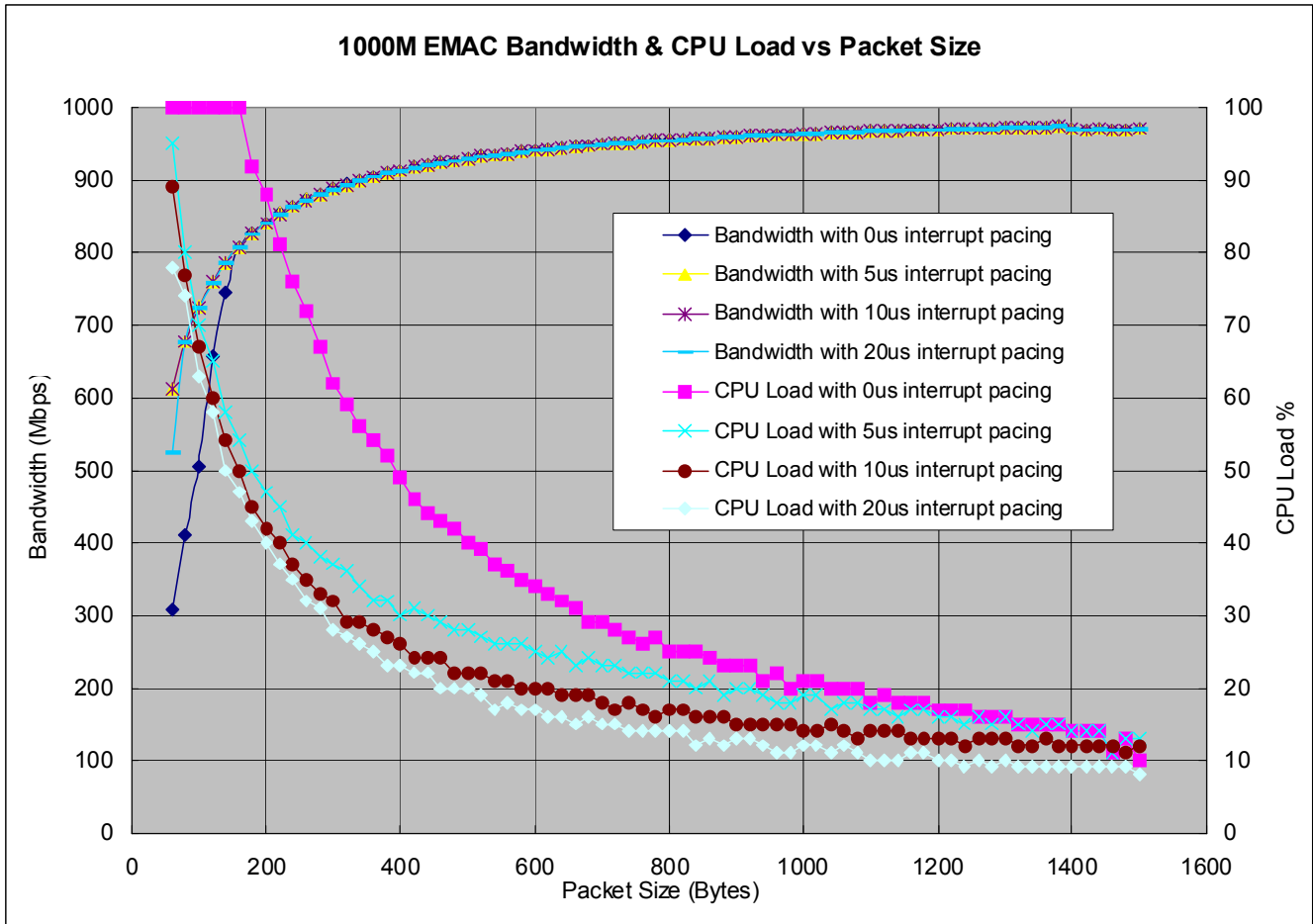
3 EMAC performance data

The actual payload bandwidth is primarily affected by packet size. The CPU load for EMAC transfer is affected by packet size and interrupt pacing. This section provides performance data for different packet size and interrupt pacing.

3.1 1000Mbps bandwidth

The curves on the top of Figure 2 show the actual payload bandwidth achieved under different conditions. The X axis is packet size (payload size); the Y axis is bandwidth.

Figure 2 1000M EMAC Bandwidth & CPU Load vs Packet Size



The actual bandwidth increases with packet size. For packets larger than 200 bytes, the actual bandwidth is higher than 800Mbps; for packets smaller than 200 bytes, the actual bandwidth decreases.

The interrupt pacing has no noticeable effect on bandwidth when the packets are larger than 200 bytes, while it does have a noticeable effect on bandwidth when the packets are smaller than 200 bytes. Longer interrupt pacing increases bandwidth. However, interrupt pacing longer than 10us does not increase bandwidth.

3.2 CPU Load for EMAC

The curves on the bottom of [Figure 2](#) show the CPU load for EMAC packet transfer under different conditions. The X axis is packet size (payload size); the right Y axis is CPU load.

The CPU load for the EMAC decreases with increased packet size. The CPU load for the smallest packet size is close to 100%, while it is only about 10% for the largest packet size.

The interrupt pacing also affects the CPU load for the EMAC though the effect is more obvious for small packet sizes. Longer interrupt pacing decreases CPU load.

Longer interrupt pacing decreases the CPU load, while also increasing the transfer delay. Additionally, longer interrupt pacing results in a larger data buffer and more packet descriptors.

$$(\text{Minimum Data Buffer Size}) = (\text{Bandwidth}) * (\text{interrupt pacing})$$

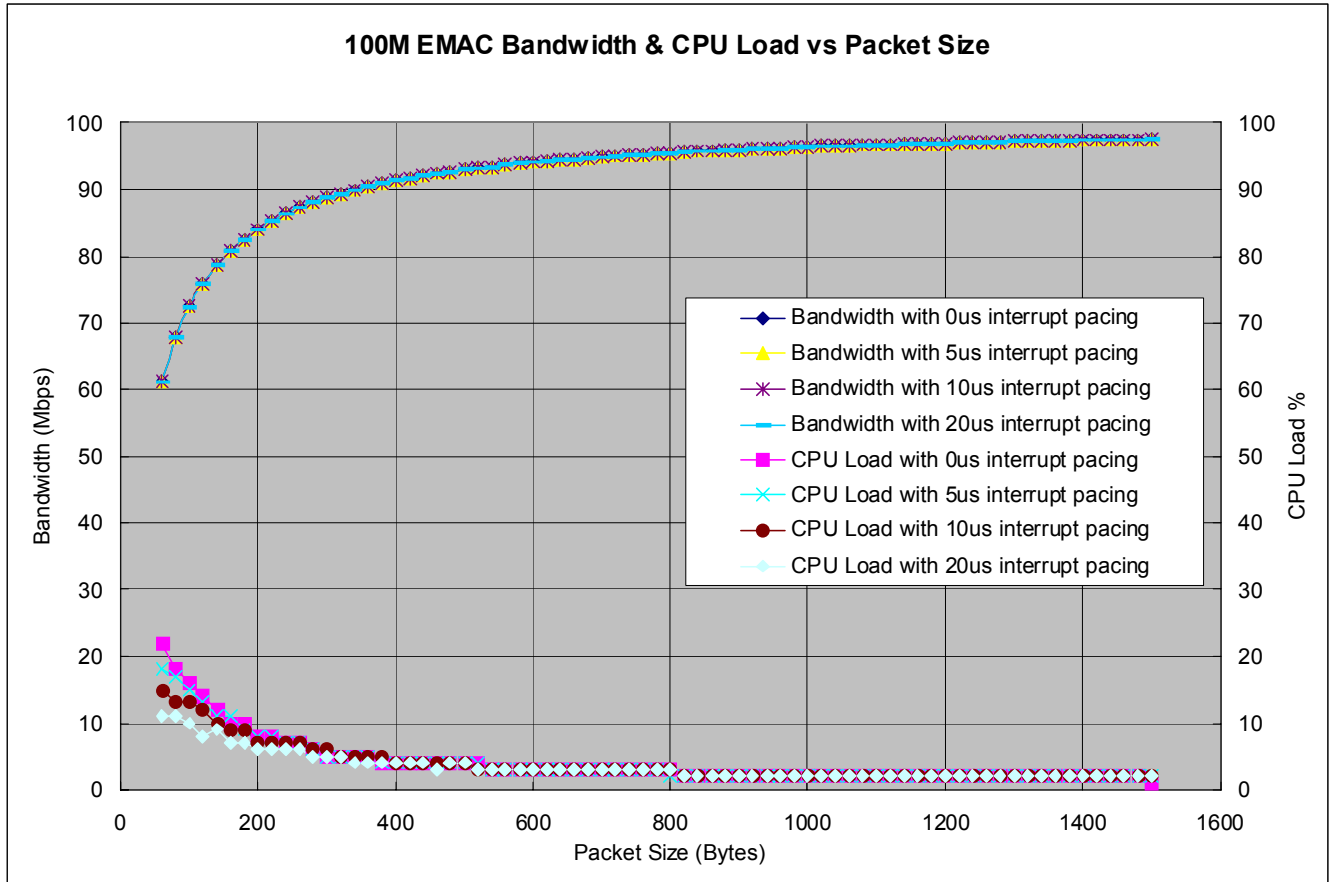
$$(\text{Descriptor number}) = \text{packets transferred during interrupt pacing} = (\text{Interrupt pacing}) / (\text{transfer time for one packet})$$

So, interrupt pacing should be a trade-off that the system designer can control. The figures above show that interrupt pacing longer than 10us can not obviously decrease CPU load further, so interrupt pacing longer than 10us is not necessary.

3.3 100Mbps performance data

Figure 3 shows the 100Mbps operation performance achieved under different conditions. The X axis is packet size (payload size); the left Y axis is payload bandwidth; the right Y axis is relevant CPU Load for EMAC.

Figure 3 100M EMAC Bandwidth & CPU Load vs Packet Size



These results are similar to 1000Mbps operation; to achieve more than 80% theoretical bandwidth, packets should be larger than 200 bytes. The charts don't show noticeable effect of interrupt pacing on the bandwidth of 100Mbps operation.

CPU load is relatively low for 100Mbps operation; it is just about 1/10 of 1000Mbps operation. Longer interrupt pacing decreases CPU load, while interrupt pacing longer than 10us is not necessary.

4 Summary

The TCI6482 EMAC performance is dramatically affected by packet size. Packets larger than 200 bytes are recommended to achieve more than 80% of theoretical bandwidth.

For 1000Mbps operation, interrupt pacing affects the CPU load for the EMAC. Longer interrupt pacing can reduce CPU load, while increasing transfer latency. Interrupt pacing longer than 10us does not improve EMAC performance, so it is not recommended.

5 References

1. [TMS320TCI648x DSP EMAC MDIO Module Reference Guide \(SPRUE12\)](#)

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