Application Report
SPRABL9A—November 2011

TMS320TCI6616-to-TMS320TCI6618 Migration Guide

High-Performance and Multicore Processors

Abstract

This document describes the main differences between the TMS320TCI6616 and TMS320TCI6618 devices and how to migrate the TMS320TCI6616-based system design to the TMS320TCI6618 design.

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Abbreviations

Term	Definition
BCP	Bit Rate Coprocessor
CDMA	CPPI DMA (submodule) (now called Packet DMA (PKTDMA))
CorePac	A specific DSP core
CRC	Cyclic Redundancy Check
DDR	Dual Data Rate memory
DL	Downlink
DMA	Direct Memory Access
DSP	Digital Signal Processor
EDMA	Enhanced Direct Memory Access
FDD	Frequency Division Duplex
FFTC	Fast Fourier Transform Coprocessor
INTC	Interrupt Controller
L2	CorePac DSP Level 2 SRAM
LLR	Log Likelihood Ratio
LTE	Long Term Evolution
MMR	Memory Mapped Register
MPU	Memory Protection Unit
PBGA	Plastic Ball Grid Array
PSC	Power Sleep Controller
RAM	Random Access Memory
TCP3d	Turbo Decoder Coprocessor
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TI	Texas Instruments
UL	Uplink
WCDMA	Wideband Code Division Multiple Access
WiMax	Worldwide Interoperability for Microwave Access

1 Introduction

The TMS320TCI6616 (TCI6616) fixed/floating-point system on a chip (SoC) and the TMS320TCI6618 (TCI6618) SoC are two Texas Instruments high-performance multicore SoC processors. Both are pin-compatible, each offering high-speed DSP processing, large internal memories, a rich set of coprocessors, accelerators, peripherals, and other support functions useful in a system environment.

This application report describes device considerations for migrating a design based on the TCI6616 to one based on the TCI6618. These two devices have many similarities; they both contain four TMS320C66x DSP CorePacs, and feature a similar mixture of memory and other peripherals. This document describes the considerations of concern for performing this migration.

Note—Since this document describes migration from a TCI6616 device to a TCI6618, familiarity with the TMS320TCI6616 device and its documentation including the errata document is assumed.

All of the documentation for the TCI6616 and the TCI6618 referenced in this migration guide can be found on the TI website located in the respective product folders. The device product folders are found at the following two web pages:

- **http://www.ti.com/product/tms320tci6616**
- **http://www.ti.com/product/tms320tci6618**

2 Basic Feature Comparison

Table 1 shows a comparison of the basic features of the TCI6616 and the TCI6618, with the differences highlighted. The remainder of this document presents a comparison of these features in greater detail, and also provides references to the appropriate documentation for further information.

Table 1 Basic TCI6616/ TCI6618 Feature Comparison (Part 1 of 2)

Hardware Features		TMS320TCI6616	TMS320TCI6618
DSP Cores		4 × C66x	4 × C66x
Speed		1000Mhz/1200Mhz	1200Mhz
Endianness		Big/Little	Big/Little
Voltage	Core (V)	SmartReflex variable supply	SmartReflex variable supply
	IO (V)	1.0 V, 1.5 V, and 1.8 V	1.0 V, 1.5 V, and 1.8 V
Package		841-Pin Flip-Chip Plastic BGA (CYP)	841-Pin Flip-Chip Plastic BGA (CYP)
Peripherals	DDR3 memory controller	1 - Capable of 1333MTS	1 - Capable of 1333MTS
	EDMA3 (16 independent channels) [CPU/2 clock rate]	1	1
	EDMA3 (64 independent channels) [CPU/3 clock rate]	2	2
	High-speed 1×/2×/4× Serial RapidIO port (4 lanes)	1	1
	Second-generation Antenna Interface (AIF2)	1	1
	I^2C	1	1
	SPI	1	1
	PCIe (2 lanes)	1	1
	UART	1	1
	10/100/1000 Ethernet	1	1
	Management Data Input/Output (MDIO)	1	1
	64-Bit Timers (configurable)(internal clock source = CPU/6 clock frequency)	Eight 64-bit or Sixteen 32-bit	Eight 64-bit or Sixteen 32-bit
	General-Purpose Input/Output Port (GPIO)	16	16
Encoder/Decoder Coprocessors	VCP2 (clock source = CPU/3 clock frequency)	4	4
	TCP3d (clock source = CPU/2 clock frequency)	2	3
	TCP3e (clock source = CPU/3 clock frequency)	1	1
	FFTC (clock source = CPU/3 clock frequency)	2	3
	BCP (clock source = CPU/3 clock frequency)	None	1
Accelerators	Receive Accelerator (RAC)	2	2
	Transmit Accelerator (TAC)	1	1
	Rake/Search Accelerator (RSA)	4	4
	Packet Accelerator (PA)	1	1
	Security Accelerator (SA)	1	1

Table 1 Basic TCI6616/ TCI6618 Feature Comparison (Part 2 of 2)

Hardware Features		TMS320TCI6616	TMS320TCI6618
Memory	Cache: L1P Cache: L1D Cache: L2 Multicore Shared Memory RAM ROM	32K bytes per core 32K bytes per core 1M bytes per core 2M bytes 128K bytes per core	32K bytes per core 32K bytes per core 1M bytes per core 2M bytes 128K bytes per core
C66x CorePac Revision ID	CorePac Revision ID Register (address location: 0181 2000h)	xxxx_xxxx_xxxx_xxxx_ 0000_0000_0000_0000b	xxxx_xxxx_xxxx_xxxx_ 0000_0000_0000_0000b
JTAG BSDL_ID	JTAGID register (address location: 0x02620018)- bits 27-12	0000_0000_1001_1101 (Rev1.0) 1011_1001_0100_0001 (Rev1.0A)	1011_1001_0100_0001
Product Status	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD	PD
End of Table 1			

3 Overall Device Considerations

The TCI6616 and the TCI6618 utilize the same TMS320C66x DSP CorePac. Code written for the DSP on the TCI6616 generally functions the same on the TCI6618. However, when executing applications on the four DSP CorePacs on the TCI6616 and TCI6618, additional considerations sometimes are needed for additional coprocessors (BCP, TCP3d, and FFTC), shared memory and resources, algorithm partitioning, and interprocessor communications. The TCI6616 and TCI6618 implement mechanisms that facilitate these functions to support execution of an application on this multi-core device.

There also are differences in other aspects of these devices that affect how code operates, including functionality of peripheral modules and differences in memory map. These differences must be addressed when migrating applications and are discussed in detail in the remainder of this document.

4 Internal Memory Comparison

Both the TCI6616 and the TCI6618 feature on-chip internal memories, allowing efficient handling of varied partitions of internal program and data information. Both devices feature several different types of cache memory, allowing significant flexibility in using this memory to enhance algorithm performance. Both devices also provide an on-chip ROM, which contains the bootloader program. Since there are some differences between the memory architectures on the two devices, such as the additional MPU5, BCP, FFT_C and TCP3d_C memory mapped registers on the TCI6618 shown in Table 2, some software modifications may be required when migrating applications from the TCI6616 to the TCI6618.

Table 2 Memory Map Comparison

Memory Map					TMS320TCI6616	TMS320TCI6618
Logical 32-Bit Address		Physical 36-Bit Address		Bytes	Description	Description
Start	End	Start	End			
3500 0000	3500 03FF	0 3500 0000	0 3500 03FF	1K	Reserved	Memory Protection Unit (MPU) 5
3500 0400	3500 7FFF	0 3500 0400	0 3500 7FFF	31K	Reserved	Reserved
3500 8000	3500 81FF	0 3500 8000	0 3500 81FF	512	Reserved	Reserved
3500 8200	3501 FFFF	0 3500 8200	0 3501 FFFF	95K	Reserved	Reserved
3502 0000	3502 03FF	0 3502 0000	0 3502 03FF	1K	Reserved	TCP3d_C config
3502 0400	3503 FFFF	0 3502 0400	0 3503 FFFF	127K	Reserved	Reserved
3504 0000	3504 07FF	0 3504 0000	0 3504 07FF	2K	Reserved	FFTC_C config[1]
3504 0800	350F FFFF	0 3504 0800	0 350F FFFF	766K	Reserved	Reserved
3510 0000	351F FFFF	0 3510 0000	0 351F FFFF	1M	Reserved	Reserved
3520 0000	3521 FFFF	0 3520 0000	0 3521 FFFF	128K	Reserved	BCP config
3522 0000	355F FFFF	0 3522 0000	0 355F FFFF	3968K	Reserved	Reserved
3560 0000	356F FFFF	0 3560 0000	0 356F FFFF	1M	Reserved	TCP3d_C data
3570 0000	37FF FFFF	0 3570 0000	0 37FF FFFF	41M	Reserved	Reserved
End of Table 2						

1. The "_C" nomenclature indicates the third instance of a peripheral or coprocessor, with _A being the first instance and _B being the second instance.

5 Peripherals

In addition to the new Bit Rate Coprocessor (BCP), which did not exist on the TCI6616, the TCI6618 has an extra Fast Fourier Transform Coprocessor (FFTC_C) and an extra Enhanced Coprocessor for Turbo Decoding (TCP3d_C).

- The FFTC_C on the TCI6618 is identical to the other two FFTCs on both devices. The FFTCs can process 2048 point FFT in 4.8µs.
- The TCP3d_C on the TCI6618 is identical to the other two TCP3ds on both devices. The TCP3d can support up to 548 Mbps for LTE and up to 353 Mbps for WCDMA.

Note—The designation "_C" indicates the third instance of a coprocessor, with _A being the first instance and _B being the second.

5.1 Bit Rate Coprocessor (BCP)

The BCP is a hardware accelerator for wireless infrastructure. It performs most of the uplink and downlink layer 1 bit processing for 3G and 4G wireless standards. It supports LTE, FDD WCDMA, TD-SCDMA, and WiMAX 802.16-2009 standards. It supports various downlink processing blocks like CRC attachment, turbo encoding, rate matching, code block concatenation, scrambling, and modulation. It supports various uplink processing blocks like soft slicer, de-scrambler, de-concatenation, rate de-matching and LLR combining. For more information, see the TMS320TCI6618 Bit Rate Coprocessor User Guide (SPRUGZ1).

5.2 Power Domains

The device has several power domains that can be turned on for operation or turned off to minimize power dissipation. The Global Power Sleep Controller (GPSC) is used to control the power gating of various power domains. Table 3 shows that the additional power domain 18 is dedicated for the BCP, FFTC_C, and TCP3d_C coprocessors on the TCI6618 device.

Table 3 Power Domain Comparison

Domain	TMS320TCI6616	TMS320TCI6618	Note	Power Connection
18	NA	BCP, FFTC_C, and TCP3d_C	Logic can be powered down for BCP, FFTC_C, and RAMs can be powered down for TCP3d_C	Software control
End of Table 3				

5.3 Clock Domains

Clock gating to each logic block is managed by the Local Power Sleep Controllers (LPSCs) of each module. For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock(s) at the source. For modules that share a clock with other modules, the LPSC controls the clock gating. Table 4 shows that the additional clock domain 30 is dedicated for the BCP, FFTC_C, and TCP3d_C coprocessors on the TCI6618 device.

Table 4 Clock Domain Comparison

Domain	TMS320TCI6616 Modules	TMS320TCI6618 Modules	Note
30	NA	BCP, FFTC_C, and TCP3d_C	Software control
End of Table 4			

5.4 PSC Register Memory Map

Table 5 shows that the additional memory mapped registers are dedicated for the PSC of BCP, FFTC_C, and TCP3d_C coprocessors on the TCI6618 device.

Table 5 PSC Register Memory Map Comparison

Offset	Register	TMS320TCI6616 Description	TMS320TCI6618 Description
0x248	PDSTAT18	Reserved	Power Domain Status Register 18 (BCP, FFTC_C and TCP3d_C)
0x348	PDCTL18	Reserved	Power Domain Control Register 18 (BCP, FFTC_C and TCP3d_C)
0x878	MDSTAT30	Reserved	Module Status Register 30 (BCP, FFTC_C and TCP3d_C)
0xA78	MDCTL30	Reserved	Module Control Register 30 (BCP, FFTC_C and TCP3d_C)
End of Table 5			

5.5 EDMA3 Channel Synchronization Events

The Enhanced Direct Memory Access 3 (EDMA3) supports up to 16 DMA channels for EDMA3CC0, 64 each for EDMA3CC1 and EDMA3CC2, that can be used to service system peripherals and to move data between system memories. For more detailed information on the EDMA3 module and how EDMA3 events are enabled, captured, processed, prioritized, linked, chained, and cleared, etc., see the Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide (SPRUGS5).

Table 6 shows EDMA3CC0 events dedicated for TCP3d_C and FFTC_C coprocessors on the TCI6618. They are reserved on the TCI6616.

Table 6 EDMA3CC0 Events Comparison

Event Number	Event	TMS320TCI6616 Event Description	TMS320TCI6618 Event Description
0	TCP3D_C_REVT0	Reserved	TCP3d_C Receive event0
1	TCP3D_C_REVT1	Reserved	TCP3d_C Receive event1
2	FFTC_C_ERROR0	Reserved	FFTC_C Error0 event and FFTC_C debug event
3	FFTC_C_ERROR1	Reserved	FFTC_C Error1 event and FFTC_C debug event
4	FFTC_C_ERROR2	Reserved	FFTC_C Error2 event and FFTC_C debug event
5	FFTC_C_ERROR3	Reserved	FFTC_C Error3 event and FFTC_C debug event
End of Table 6			

Similarly, Table 7 shows EDMA3CC2 events dedicated for TCP3d_C and FFTC_C coprocessors on the TCI6618 and reserved on the TCI6616.

Table 7 EDMA3CC2 Events Comparison

Event Number	Event	TMS320TCI6616 Event Description	TMS320TCI6618 Event Description
58	TCP3D_C_REVT0	Reserved	TCP3d_C Receive event0
59	TCP3D_C_REVT1	Reserved	TCP3d_C Receive event1
60	FFTC_C_ERROR0	Reserved	FFTC_C Error0 event and FFTC_C debug event
61	FFTC_C_ERROR1	Reserved	FFTC_C Error1 event and FFTC_C debug event
62	FFTC_C_ERROR2	Reserved	FFTC_C Error2 event and FFTC_C debug event
63	FFTC_C_ERROR3	Reserved	FFTC_C Error3 event and FFTC_C debug event
End of Table 7			

Table 8 shows INTC0 event inputs dedicated for BCP, TCP3d_C, and FFTC_C coprocessors on the TCI6618 and reserved on the TCI6616.

Table 8 INTC0 Event Inputs — C66x CorePac Secondary Interrupts Comparison

Input Event Number on INTC0	System Interrupt	TMS320TCI6616 System Interrupt Description	TMS320TCI6618 System Interrupt Description
91	BCP_ERROR0	Reserved	BCP error 0
92	MPU1_INTD (MPU1_ADDR_ERR_INT and MPU1_PROT_ERR_INT combined	MPU1 addressing violation interrupt and protection violation interrupt.	MPU1 addressing violation interrupt and protection violation interrupt.
93	BCP_ERROR1	Reserved	BCP error 1
94	MPU2_INTD (MPU2_ADDR_ERR_INT and MPU2_PROT_ERR_INT combined	MPU2 addressing violation interrupt and protection violation interrupt.	MPU2 addressing violation interrupt and protection violation interrupt.
95	BCP_ERROR2	Reserved	BCP error 2
96	MPU3_INTD (MPU3_ADDR_ERR_INT and MPU3_PROT_ERR_INT combined	MPU3 addressing violation interrupt and protection violation interrupt.	MPU2 addressing violation interrupt and protection violation interrupt.
97	BCP_ERROR3	Reserved	BCP error 3
180	TCP3D_C_ERROR MPU5_INTD (MPU5_ADDR_ERR_INT and MPU5_PROT_ERR_INT combined)	Reserved	TCP3D_C_Error event MPU5 Addressing violation interrupt and Protection violation interrupt.
202	TCP3D_C_REVT0	Reserved	TCP3d_C receive event0
203	TCP3D_C_REVT1	Reserved	TCP3d_C receive event1
204	FFTC_C_ERROR0	Reserved	FFTC_C Error0 event and FFTC_C debug event
205	FFTC_C_ERROR1	Reserved	FFTC_C Error1 event and FFTC_C debug event
206	FFTC_C_ERROR2	Reserved	FFTC_C Error2 event and FFTC_C debug event
207	FFTC_C_ERROR3	Reserved	FFTC_C Error3 event and FFTC_C debug event
End of Table 8			

Similarly Table 9 shows INTC2 event input dedicated for TCP3d_C coprocessor on the TCI6618. It is reserved on the TCI6616.

Table 9 INTC2 Event Inputs — C66x EDMA3CC0 Secondary Interrupts Comparison

Input Event Number on INTC2	System Interrupt	TMS320TCI6616 System Interrupt Description	TMS320TCI6618 System Interrupt Description
48	TCP3D_C_ERROR MPU5_INTD (MPU5_ADDR_ERR_INT and MPU5_PROT_ERR_INT combined)	Reserved	TCP3D_C Error Event MPU5 Addressing violation interrupt and Protection violation interrupt.
End of Table 9			

5.6 Memory Protection Unit (MPU)

The TCI6618 supports six MPUs while the TCI6616 supports only five MPUs. The MPU5 on the TCI6618 is used to protect the main CFG TeraNet of the TE_SCR_3M.

5.6.1 MPU5 Memory Region

Table 10 shows MPU5 Memory Region for TE_SCR_3M on the TCI6618 and reserved on the TCI6616.

Table 10 MPU Memory Region Comparison

	Memory Protection	Start Address	End Address	TMS320TCI6616 Memory Protection	TMS320TCI6618 Memory Protection
MPU5	TE_SCR_3M	3502 0000	3521 FFFF	Reserved	TE_SCR_3M
End of Table 10					

5.6.2 MPU5 Configuration Register (CONFIG)

The Configuration Register (CONFIG), Figure 1-1, contains the configuration value of the MPU5 on the TCI6618. See the Data Manual (SPRS688) for the MPU5 register's memory map and details.

Figure 1-1 MPU5 Configuration Register (CONFIG)

31 24	23 20	19 16	15 12	11 1	0
ADDR_WIDTH	NUM_FIXED	NUM_PROG	NUM_AIDS	Reserved	ASSUME_ALLOWED
R-0	R-0	R-3	R-16	R-0	R-1

Legend: R = Read only; -*n* = value after reset

5.7 Master ID

Table 11 shows the Master IDs assigned to PA_SS, QM_SS, and TE_SS peripherals on the TCI6616 and TCI6618.

Table 11 Master ID Setting Comparison

Master ID	TMS320TCI6616 Master ID	TMS320TCI6618 Master ID
56 to 59	PA_SS (Rev 1.0) QM_SS (Rev 1.0A)	QM_SS
92 to 93	QM_second (Rev 1.0) PA_SS (Rev 1.0A)	PA_SS
96	Reserved	FFTC_C
97	Reserved	Reserved
98 to 100	Reserved	BCP
End of Table 11		

5.8 Privilege ID

Table 12 shows, on TCI6616, Priviledge ID 8 assigned to either PA_SS or QM_second (depending on silicon revision) while Priviledge ID 10 is assigned to either QM_CDMA/QM_second or QM_CDMA/PA_SS. The Privilege ID 15 is assigned to TE_SCR_3M peripheral on the TCI6618.

Table 12 Privilege ID Setting Comparison

Privilege ID	TMS320TCI6616			TMS320TCI6618		
	Master	Privilege Level	Security Level/Access Type	Master	Privilege Level	Security Level/Access Type
8	PA_SS (Rev1.0) QM_second (Rev1.0A)	User	Non-secure/DMA	QM_second	User	Non-secure/DMA
10	QM_CDMA/QM_second (Rev 1.0) QM_CDMA/PA_SS (Rev 1.0A)	User	Non-secure/DMA	QM_CDMA/PA_SS	User	Non-secure/DMA
15	Reserved	Reserved	Reserved	TE_SCR_3M	User	Non-secure/DMA
End of Table 12						

6 Thermal Data Differences

There are small differences in the thermal data figures between the TCI6616 and TCI6618. See the Data Manual for the details for your specific part.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265